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Freezing Grid-Forming Converter Virtual Angular Speed to Enhance Transient Stability Under Current Reference Limiting

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Abstract—Grid-forming voltage source converters have been envisioned to play a major role in future power systems, but they have limited overcurrent capability. Therefore, it is important to investigate their ability to ride through faults and maintain system stability under strict overcurrent limits. Different current priority limiting controls based on conditional anti-windup integration are formulated, and transient stability is analyzed using voltage phasor diagrams. Subsequently, a practical solution is proposed which enhances transient stability, by freezing the virtual angular speed to the pre-fault value during faults, once current saturation occurs. Additionally, temporarily freezing the post-fault angular speed to a value slightly less than pre-fault value ensures recovery from the saturated current state. Simulation results, based on a modified IEEE 39-bus system validate the efficacy of the proposed solution.

Keywords—Grid-forming converter, current limiting, transient stability, anti-windup integration, fault analysis.

I. INTRODUCTION

Power systems are undergoing a period of unprecedented change, with conventional generation, based around synchronous generators, being displaced by converter-based renewable energy sources, along with increased HVDC interconnection to neighboring systems [1]-[4]. At present, most power converters are “grid-following”, and employ a phase-locked loop to synchronize with the grid frequency, based on the converter terminal voltage. Moving forward with higher converter shares, “grid-forming” converters, with the ability to regulate voltage and frequency, are envisioned to displace synchronous-based generation. However, they have much smaller overload capability, and, so, it is important to investigate how grid-forming converters can maintain system transient stability under stringent overcurrent limits.

Although various grid-forming converter current limiting strategies have been proposed [7]-[13], a range of aspects are not always addressed. Firstly, the modulated voltage angle of the converter should be limited when current limiting is active, but then part, or all, of the grid forming capability is lost. The resulting impact on converter synchronization is confirmed by analysis of grid-forming converters with only a (soft) virtual impedance current limit in [5][8]. Secondly, since cascading voltage and current controllers [6] are typically employed in grid-forming converters, windup integration of the voltage proportional-integral (PI) controllers must be avoided, with consequences for dynamic stability support. It is also highly desirable that grid-forming

capability should be maintained for as long as possible during fault conditions, and that current saturation should end as soon as possible after the fault is cleared, when the grid voltage is within normal bounds.

Existing grid-forming converter current limiting strategies can be divided into two groups: without [7]-[9], and with [10]-[13] current reference limiters. The former approach offers the advantage of remaining sensitive to changes in grid voltage, and being able to re-schedule active and reactive current within current limits. However, there are also some disadvantages: the virtual impedance (VI) control in [7][8] cannot strictly limit the current; additionally, since the VI gains are normally obtained through offline studies for particular conditions, sub-optimal performance can be experienced for other conditions; finally, synchronization stability remains a concern, although an adaptive droop coefficient [8] may be helpful. The projected control in [9] introduces current constraints into the droop design optimization problem, to strictly limit the current, but it is assumed that all grid-forming converters adopt the same control algorithm with no other regulators present, which, of course, restricts method applicability.

For the latter group using current reference limiters, two issues have been targeted in existing methods [10]-[13]: integrator windup for the outer PI loop, and synchronization instability due to an increase in the modulated voltage angle when the current reference limiters are active. Anti-windup integration is applied in [10][11], while the q-axis voltage across the LCL capacitor is fed into the virtual angular speed control loop (i.e. P/f droop loop) in [11], to address synchronization instability. Stability is improved but is not guaranteed here, depending on the sign of the measured q-axis voltage and the proportional gain. In [12][13], anti-windup is not used in the outer voltage PI loop, but instead, in [12], the voltage reference is modified using adaptive virtual impedance control. However, the voltage integrator anti-windup can't be guaranteed, depending on the adaptive virtual impedance gain, and the voltage reference can't be modified further when current limiting is active (since the current is fixed). In contrast, in [13], the active and reactive power references are switched to levels based on low-voltage ride-through (LVRT) grid code requirements. The references can only be followed when the active power is PI/I controlled, which is not suitable for a P/f droop-controlled grid-forming converter. Moreover, only active current prioritization is considered. It should also be noted that none of methods [10]-[13] investigate how a grid-forming converter will post-fault exit the current saturation state [14], as they tend to rely upon

a change in grid voltage.

In this paper, it is proposed that a current reference limiting technique is applied, together with conditional anti-windup integration, and freezing of the virtual angular speed input once the converter is in current saturation. Using this simple method, the converter current can be strictly limited, and the modulated voltage angle is also frozen, so that converter transient stability is enhanced. Meanwhile, maximum voltage support is obtained automatically, since the converter is attempting to maintain the voltage at its target value before saturation occurs. The main contributions of this paper are summarized as follows:

- Freezing the virtual angular speed under current reference limiting control, with modified conditional anti-windup integration, is proposed here for a “grid-forming” converter (or converter based on virtual synchronous machine, power synchronization, or other control concepts without using a PLL, and can independently regulate voltage magnitude and frequency), which is straightforward to implement, but can also ensure strict current limits, contribute to active and reactive power regulation, and enhance transient stability.
- It is shown that freezing the virtual angular speed to its pre-fault value doesn't ensure that a grid-forming converter exits current saturation and recovers voltage controllability after fault clearance and grid voltage phase shifts. Hence, freezing the post-fault angular speed to a slightly reduced value is proposed.
- It is found that active and reactive current prioritization limiting mode can easily excite high-frequency oscillations, but such problem doesn't occur with scaling current limiting, which generates smooth current references.

The remainder of the paper is organized as follows: Section II introduces some grid-forming control principles, along with formulations of three current prioritization limiting strategies, including conditional anti-windup integration. Section III then presents the proposed freezing of virtual angular speed technique, supported by simulation results in Section IV, and Section V concludes the paper.

II. GRID-FORMING CONVERTER WITH CURRENT REFERENCE LIMITING AND CONDITIONAL ANTI-WINDUP INTEGRATION

Typical grid-forming control, with cascaded voltage and current PI controllers, is first introduced, and then current reference limiting with conditional anti-windup integration based on different current priorities is presented. Subsequently, high-frequency oscillation phenomena for active and reactive current priority limiting is revealed through simulation studies. Finally, grid-forming converter synchronization stability is analyzed under fault conditions using voltage phasor diagrams.

A. Typical Grid-Forming Control with Cascaded Voltage and Current PI Controllers

A grid-forming converter, connected via an LCL filter to an equivalent AC grid, is shown in Fig. 1. The converter consists of a 3-phase, 2-level voltage source converter (VSC) supplied by a DC voltage, V_{dc} (assumed constant, so transient stability issues relate only to AC-side controls, with DC-side dynamics ignored). In Fig. 1, v_c is the converter modulated

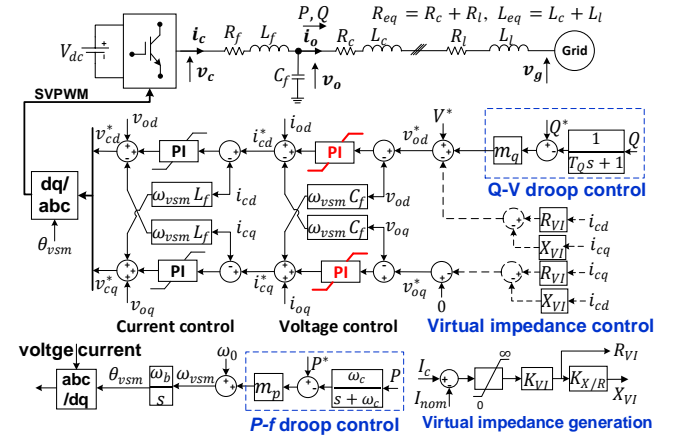


Fig. 1. Grid-forming converter connected to AC system via LCL filter.

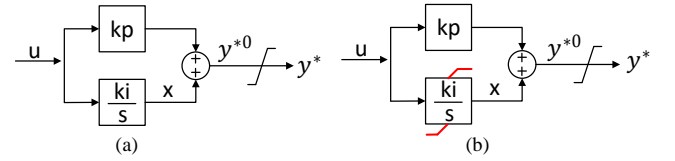


Fig. 2. (a) Windup integration, (b) conditional anti-windup integration.

voltage, i_c , the current through filter L_f , v_o , output voltage across capacitor C_f , and, i , output current through grid-side inductance, L_c . The AC system is formed as an ideal AC voltage source, v_g , in series with L_l , R_l , with $V_g = 1$ pu. Equivalent output impedance seen by the converter is L_{eq} , R_{eq} , with $L_{eq} = 10R_{eq} = 0.25$ pu, based on rated voltage and converter capacity.

Fig. 1 also presents a typical grid-forming cascaded control structure, which includes cascaded AC voltage and current loops represented in synchronous frame, and P/f and Q/V droop control loops. The cascaded voltage and current loops consist of two cascaded PI controllers, feedforward decoupling terms and compensation. The current references are determined by the outer AC voltage control loop, while the AC current control loop generates the modulated voltage, which will be further modulated as switching signals through a linearization stage. The reference voltage phase angle, θ_{vsm} , which is used to transform voltage and current signals between the stationary abc and dq coordinates, and the reference voltage magnitude ($v_{dq}^* = V_{ref} + j0$), are provided by P/f and Q/V droop control respectively. The P/f and Q/V droop controls are expressed by

$$\theta_{vsm} = \frac{\omega_b \omega_{vsm}}{s}, \quad (1)$$

$$\omega_{vsm} = \omega_0 + m_p \left(P^* - \frac{\omega_c}{s + \omega_c} P \right), \quad (2)$$

$$V_{ref} = V^* + m_q \left(Q^* - \frac{1}{T_Q s + 1} Q \right), \quad (3)$$

where, ω_b , ω_0 , and ω_{vsm} represent the nominal frequency in rad/s and per unit, and the virtual angular speed, while m_p and m_q are the active and reactive droop gains. ω_c and T_Q are the cut-off frequency and time constant of the low-pass filters, associated with filtering the active and reactive output power P and Q signals. Finally, $V_{ref} \approx V^*$ since $m_q \approx 0$.

The virtual impedance control shown in Fig. 1 will be applied in Section IV.

B. Current Reference Limiting with Anti-windup Integration

In order to strictly limit the converter current and simplify control design, current reference limiting is adopted here. Since integrator windup in the outer voltage PI controllers will affect converter stability characteristics, conditional anti-windup integration, shown in Fig. 2(b), is adopted here. The approach follows IEEE Standard 421.5-2016 [15], offering faster post-fault convergence over other anti-windup techniques [16]. For clarity, windup integration is shown in Fig. 2(a).

For the application at hand, three types of current reference limiting strategies are now formulated based upon different current prioritization principles:

- Active (d-axis) current priority limit:

$$i_{c,d}^* = \begin{cases} i_{c,d}^{*0}, & \text{if } |i_{c,d}^{*0}| < I_{max} \\ \pm I_{max}, & \text{if } |i_{c,d}^{*0}| \geq I_{max} \end{cases}, \quad (4)$$

$$i_{c,q}^* = \begin{cases} i_{c,q}^{*0}, \dot{x}_{dq} = k_{iv} \mathbf{u}_{dq}, & \text{if } |i_{c,q}^{*0}| < \sqrt{I_{max}^2 - i_{c,d}^{*2}} \\ \pm \sqrt{I_{max}^2 - i_{c,d}^{*2}}, \dot{x}_{dq} = \mathbf{0}, & \text{if } |i_{c,q}^{*0}| \geq \sqrt{I_{max}^2 - i_{c,d}^{*2}} \end{cases} \quad (5)$$

- Reactive (q-axis) current priority limit: the same as (4)(5), but with d and q subscripts exchanged.
- Scaling down limit:

$$i_{c,dq}^* = \begin{cases} i_{c,dq}^{*0}, \dot{x}_{dq} = k_{iv} \mathbf{u}_{dq}, & \text{if } \|i_{c,dq}^{*0}\| < I_{max} \\ \gamma i_{c,dq}^{*0}, \dot{x}_{dq} = \mathbf{0}, & \text{if } \|i_{c,dq}^{*0}\| \geq I_{max} \end{cases}. \quad (6)$$

where $\mathbf{u}_{dq} = u_d + ju_q$, $\mathbf{x}_{dq} = x_d + jx_q$, while u_d and x_d , and u_q and x_q , are the inputs and outputs of the d-axis and q-axis integrators, while $\gamma = I_{max} / \|i_{c,dq}^{*0}\|$. I_{max} is the maximum current, and variables with, and without, superscript 0 represent values before, and after, the limiter in Fig. 2(b). It should be noted from (4)(5), $\dot{x}_d = 0$ when $|i_{c,d}^{*0}| \geq \sqrt{I_{max}^2 - i_{c,d}^{*2}}$ instead of $|i_{c,d}^{*0}| \geq I_{max}$. Hence, $\dot{x}_d = 0$ once $I_c^0 \geq I_{max}$, instead of waiting until $|i_{c,d}^{*0}| \geq I_{max}$ becomes true. Similarly $\dot{x}_q = 0$ when $|i_{c,q}^{*0}| \geq \sqrt{I_{max}^2 - i_{c,q}^{*2}}$ instead of $|i_{c,q}^{*0}| \geq I_{max}$ for the reactive current prioritization limit.

The modulated voltage can be limited using scaling anti-windup limiting, but the voltage limit is rarely reached, and the modulated voltage can be physically limited by the DC voltage.

C. Oscillation Phenomenon under Active and Reactive Current Prioritization Limiting Control

For the test system of Fig. 1, a 250 m fault is applied at 2 s such that V_g falls to 0.1 pu, as shown in Fig. 3. Under active, reactive current prioritization and scaling-down limiting control, the active power reference, P^* , is set at the experimentally observed stability limit, namely 0.6 pu, 0.15 pu and 0.4 pu. Two scenarios are simulated: without, and with, adding an extra resistor 0.2 pu and 2 pu in series with C_f for active and reactive current priority limiting respectively. All other parameters are summarised in the Appendix, Table I.

The simulation results of Fig. 3 show that the currents are strictly limited to 1.1 pu in all cases. However, under active and reactive current priority limiting there are obvious oscillations, with a frequency of 250 ~ 400 Hz (which is

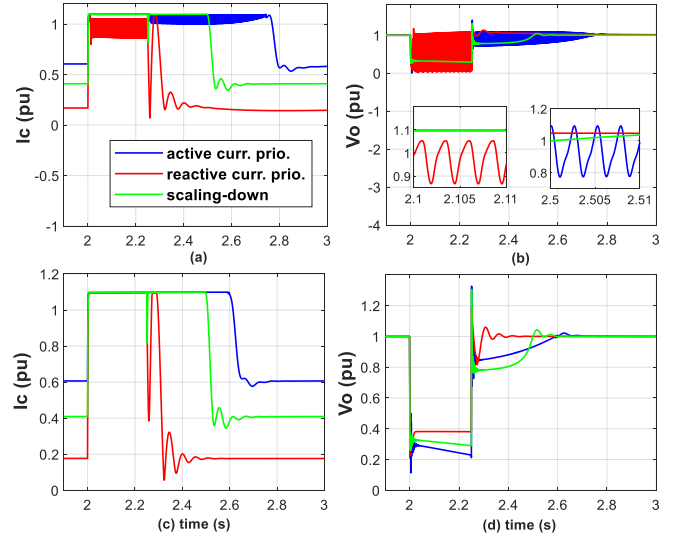


Fig. 3. 250 ms 3-phase fault ($V_g = 0.1$ pu during fault) under active & reactive current priority and scaling limiting controls: (a)(b) without adding an extra damping resistor, (c)(d) adding an extra resistor 0.2 pu and 2 pu in series with C_f under active and reactive priority limiting controls.

above the $L_f C_f L_{eq}$ resonant frequency $\sqrt{(L_f + L_{eq}) / (4\pi^2 L_f C_f L_{eq})} = 101$ Hz), due to sudden changes in the d- and q-axis current references exciting $L_f C_f L_{eq}$ resonance. Such oscillations can be avoided by using scaling current limiting (which provides smooth d- and q-axis current references), or using passive or active damping techniques. Fig. 3(c)(d) shows that the oscillations are almost eliminated with an additional resistor.

Based on the above results, active and reactive current priority limiting are not preferred (especially the latter, as the required resistor is large), considering (1) the importance of simultaneous active and reactive power (in other words voltage angle and amplitude) regulation for a grid-forming converter, (2) the oscillating frequency varies with operating conditions. Hence, these options are not discussed further, although the freezing of virtual angular speed technique, as proposed here, can also enhance their grid-forming transient stability, similar to that for current scaling limiting control.

III. GRID-FORMING CONVERTER TRANSIENT STABILITY ENHANCEMENT UNDER CURRENT REFERENCE LIMITING

A. Freezing of Virtual Angular Speed to Pre-fault Value

Using reference limiting with conditional anti-windup integration, the converter current can be strictly limited. However, the converter can easily lose transient stability, since the modulated voltage angle continues to increase when the converter is already in current saturation and has no voltage frequency (or voltage angle) regulation capability. However, the problem can be readily solved by freezing the virtual angular speed ω_{vsm} to the pre-fault value ω_{vsm}^0 or ω_0 , when the converter hits the current limit to prevent the dq coordinates rotating, as below

$$\omega_{vsm} = \begin{cases} \omega_0 + m_p(P^* - p_m), & I_c^* < I_{max} - \epsilon_{db} \\ \omega_{vsm}^0 \text{ or } \omega_0, & I_c^* \geq I_{max} \end{cases}, \quad (7)$$

where ϵ_{db} is a small deadband to avoid frequent switching and ensure numerical solvability in simulation software. It is noted that freezing the virtual angular speed is equivalent to

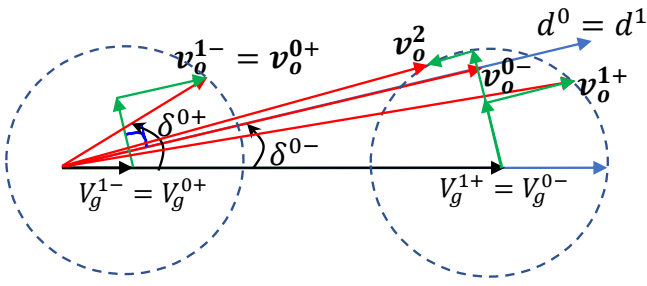


Fig. 4. Voltage phasor diagram of system in Fig. 1 with grid-forming converter under scaling limiting and freezing the virtual angular speed control (eqn. 7) under situation (a), where green lines represent d- and q-axis voltage drops across L_{eq} , red lines are the converter output voltage, and dark blue lines are the converter dq coordinate (q axis not shown). Subscripts 0, 1 and 2 represent variables at the time of fault occurrence, clearance and a short period after fault clearance, while - and + represent the instants before and after an event occurs.

switching the active power reference to $P^* = p_m$, or reducing the droop coefficient, m_p , to zero when the current hits the limit.

B. Enhanced Virtual Angular Speed Freezing

After a fault is cleared, the sudden change in grid voltage will normally cause the converter to exit current saturation, based on the control principles of the outer voltage loop. However, it is also possible for the grid-forming converter to remain in current saturation after fault clearance. This usually happens with high pre-fault current under the following two situations:

Situation (a): the virtual angular speed is immediately frozen during a fault, but grid stability is retained after fault clearance, as represented by the phasor diagram of Fig. 4. When the fault occurs, v_o^{0-} changes to v_o^{0+} , and due to immediate current saturation and freezing of ω_{vsm} , the dq coordinates do not rotate during the fault, and so just prior to fault clearance $v_o^{1-} = v_o^{0+}$. Then, with the voltage drops (in green) being moved right along with V_g^{1+} , v_o^{1+} is obtained immediately after the fault clears. It is seen that since $v_{oq}^{1+} < 0 < v_{oq}^{1-}$ and $0 < v_{od}^{1-} < v_{od}^{1+}$, then i_{cq}^{1+} increases (from negative) and i_{cd}^{1+} decreases (from positive) such that the converter exits current saturation, but only for a short period, before entering current saturation again, whereupon V_o^{2+} is lower than V_o^{0-} . Then, since the converter is in current saturation, but grid conditions are stable, both the dq coordinates and v_o^2 are unchanged. It is seen that if P^* is small, then the current will be less likely to be saturated again after the fault clears.

Situation (b): the virtual angular speed is increased (so dq coordinates rotate anticlockwise) during the fault, due to the converter current not hitting its limit. Then after the fault clears, the converter may well be in current saturation with a low voltage (and probably active power) output. If local devices are not available to restore the equivalent grid voltage amplitude or frequency, the grid-forming converter will remain in current saturation.

To break the saturation deadlock, two approaches can be considered: (i) modifying the voltage and/or power references, (ii) rotating the dq coordinates clockwise after fault clearance. The principle behind the latter method can be

explained as follows: from Fig. 4, with the dq coordinates rotating clockwise, i_{cd} and i_{cq} will change, and v_o^2 and P will increase slowly, until, after some time, the current exits saturation. The second method is easier to implement, and, hence, is considered here, given by (8).

$$\omega_{vsm} = \begin{cases} \omega_0 + m_p(P^* - p_m), & I_c^{*0} < I_{max} - \epsilon_{ab}, \\ (\omega_{vsm}^0 - \epsilon) \text{ or } (\omega_0 - \epsilon), & I_c^{*0} \geq I_{max} \end{cases}, (8)$$

where ϵ is a small positive constant if $P^* > 0$, and a negative one if $P^* < 0$. The proposed freezing technique is summarized as ω_{vsm} is given by (7) during the fault, and by (8) after fault clearance. The angular speed freezing technique, together with the current reference limiting and conditional anti-windup integration, can be understood as:

- Freezing the virtual angular speed of a grid-forming converter to ω_{vsm}^0 or ω_0 during faults provides maximum inertial support. Being a “grid-forming” converter, there is no need to maintain synchronism during faults, otherwise inertial and frequency regulation could not be provided automatically and independently, which is also a major reason for not recommending active or reactive current priority limiting modes;
- Reactive power/voltage support is automatically maximized during faults, as seen from Fig. 1, where the converter aims to maintain the output voltage at V^* ;
- Precisely “following” a reactive power reference is not possible for a P/f droop grid-forming converter, unless integral control is employed, or the virtual angular speed is obtained from a PLL, which obviously violates the intention of being “grid-forming”;
- The main drawback, however, is that although post-fault signal freezing can recover a grid-forming converter from being current saturated, the approach is not optimal from a power system global stability perspective.

For Situation (a), the effectiveness of the proposed freezing technique is now demonstrated for the system of Fig. 1, under a 250 ms fault (created by $V_g = 0.1$ pu), and with the grid-forming converter operating under scaling current limiting control (6). Two cases are simulated. In Case 1, two control modes are considered: (i) freezing ω_{vsm} to ω_0 (*Simple freezing*), and (ii) freezing it to ω_0 during the fault and to $\omega_0 - 0.005$ pu after fault clearance, if the current is saturated (*Enhanced freezing*). In (7)(8) $\epsilon_{ab} = 0.01$ pu.

For the *Simple* mode, $P^* = 0.7$ and 0.9 pu, while for the *Enhanced* mode, $P^* = 1$ pu. Fig. 5 demonstrates that 0.9 pu is the minimum active power which leads to current saturation after clearing a 250 ms fault under *Simple freezing*, a value much larger than 0.4 pu in Fig. 3, demonstrating the achieved improvement in transient stability. Under high load conditions, *Simple freezing* ($P^* = 0.9$ pu) results in the converter remaining in current saturation, with the output voltage and power not controllable after fault clearance, while for *Enhanced freezing* ($P^* = 1$ pu), the converter quickly exits current saturation and regains “grid-forming” functionality within 0.1 s.

In Case 2, shown in Fig. 6, the settings are the same as Case 1, except that $P^* = -1.02$ pu, and under *Enhanced freezing*, ω_{vsm} is frozen to $\omega_0 + 0.005$ pu after fault clearance if the current is saturated. Under *Simple freezing* the converter remains in current saturation, while under

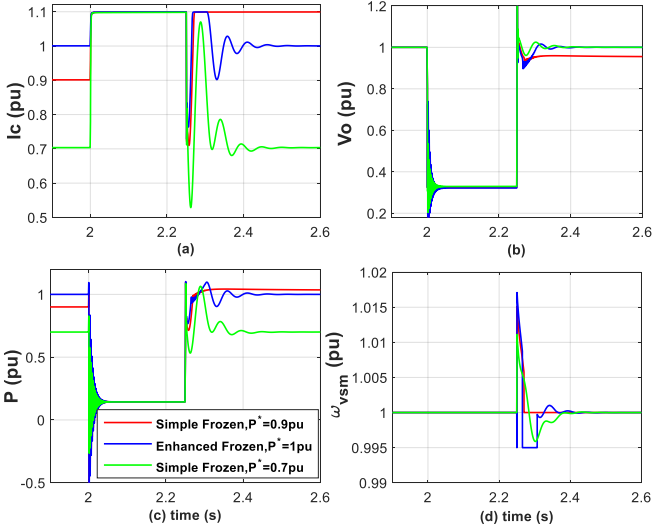


Fig. 5. Application of 250 ms 3-phase fault ($V_g = 0.1$ pu during the fault) with *Simple* and *Enhanced* freezing of virtual angular speed controls with $P^* > 0$.

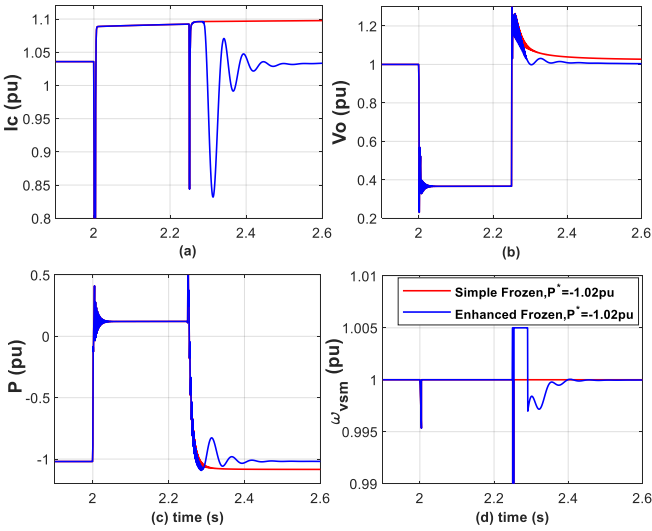


Fig. 6. Application of 250 ms 3-phase fault ($V_g = 0.1$ pu during the fault) with *Simple* and *Enhanced* freezing of virtual angular speed controls with $P^* < 0$.

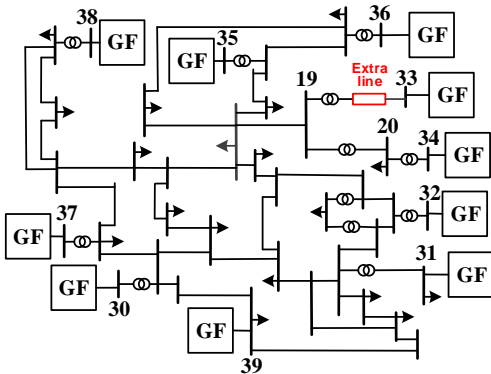


Fig. 7. 39-bus system with grid-forming converters replacing generators.

Enhanced freezing the converter exits current saturation within 0.1 s. Note that the high frequency oscillations will normally be eliminated in practice, since for the $L_f C_f L_{eq}$ circuit structure additional harmonic damping capability will be introduced.

IV. VALIDATION ON NEW ENGLAND TEST SYSTEM

The New England 39-bus system [17] with all synchronous generators replaced by grid-forming converters, Fig. 7, is used to validate the dynamic performance of the proposed current limiting control. Adopting a 100% grid-forming approach, with all synchronous generation displaced, represents a transient stability worst case, considering the much smaller overload capability of VSCs compared to synchronous units. The grid-forming converter LCL filter and control parameters are unchanged from before (Table I in Appendix), with the cascaded voltage and current controllers parameters based on [18], to guarantee robust stable behavior for different operating conditions. The system loads and generation are unchanged. Constant impedance loads and equivalent π electrical lines are modelled. The converter capacity is 1000 MVA, except at buses 33 and 34, which are modified as 702 and 564 MVA respectively (so that their active power setpoints reach 0.9 and 0.7 pu). In order to weaken the connection to the converter at bus 33, an extra line ($R = 0.56$ pu and $L = 0.14$ pu, under the converter capacity base) is inserted between buses 19 and 33. Simulations are performed within the Dymola environment, enabling the differential equations for the transmission lines and converters to be easily and transparently formulated.

Case 1: The effectiveness of the proposed approach of freezing the virtual angular speed is assessed by comparing against a few alternative options: (1) typical virtual impedance (*Typical VI*) control (Fig. 1); (2) *Adaptive VI* control, based on the approach [8], with a reduced droop

coefficient of $m_p \sqrt{(1 - \Delta v_{VI,d})^2 + \Delta v_{VI,q}^2}$ when the virtual impedance is active; (3) scaling current limiting (*Scaling Only*); (4) as previous, but with freezing of the virtual angular speed input using equ. 7 (*Simple Frozen + Scaling*). For options (3) and (4) $I_{max} = 1.1$ pu.

A 250 ms 3-phase bolted fault is applied at bus 19 at 2 s under the above 4 options, with Fig. 8 showing results for grid-forming converters at buses 33 and 34. Fig. 8(a)(b) shows that under *VI* and *Adaptive VI* the converter currents can exceed 1.1 pu with high spikes lasting $\approx 7\sim 10$ ms, but under the other two approaches the current is strictly limited to 1.1 pu. Fig. 8(c)(d) show that under *Frozen + Scaling* the grid-forming converter is stable and quickly recovers to its pre-fault state after the fault is cleared, while under the other three controls the converter is not stable and the active power output P goes negative and the voltage output falls low. It is seen that under *Adaptive VI*, at the instant of fault clearance, P is higher than that under *Typical VI*, which indicates improved transient stability, but the initial P is still less than P^* , and therefore the converter can't avoid losing stability, while the reduced droop coefficient only retards the evolution of P vs. $\theta_{vsm} - \theta_g$, leading to an extended recovery period.

Case 2: In Case 1, none of the grid-forming converters are in current saturation after the fault is cleared under *Simple Frozen + Scaling*. To create Situation (b) in Section III.B, the current limit is set to $I_{max} = 1.2$ pu. Two options are considered: (i) *Simple Frozen + Scaling*, (ii) freezing the virtual speed input to ω_{vsm}^0 during the fault, and to $\omega_{vsm}^0 - 0.005$ pu after the fault clears if the current is saturated (*Enhanced Frozen + Scaling*). A 250 ms 3-phase bolted fault is again applied at bus 19 at 2 s under the above 2 options, with Fig. 9 showing results for the grid-forming converter at

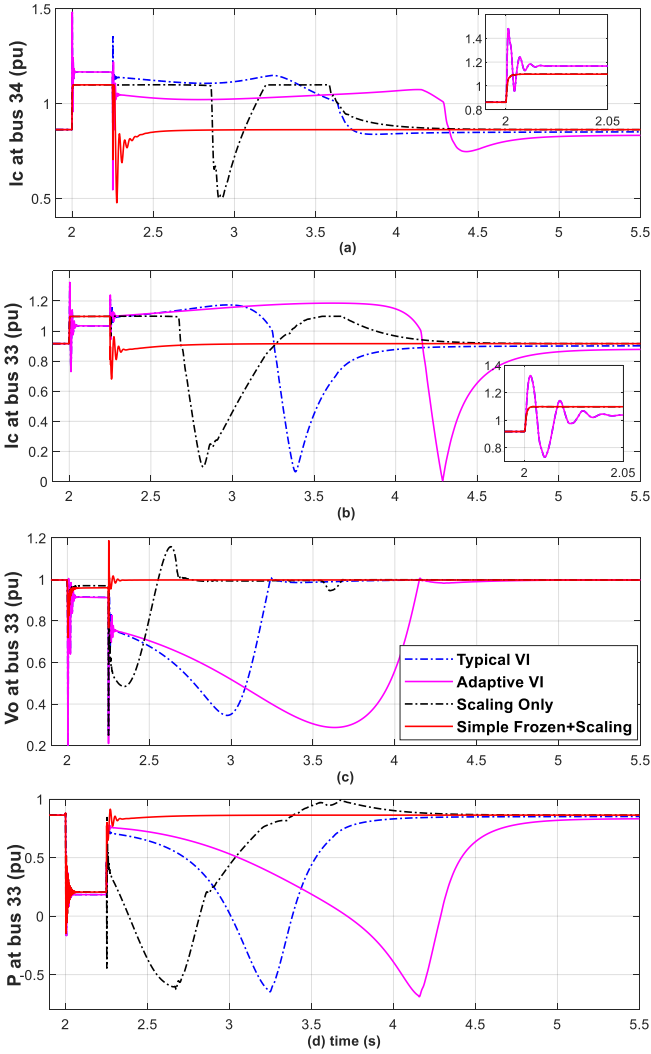


Fig. 8. Performance of grid-forming converter at bus 33 and 34, subject to a 250 ms 3-phase fault at bus 19, for different *scaling* current limiting options.

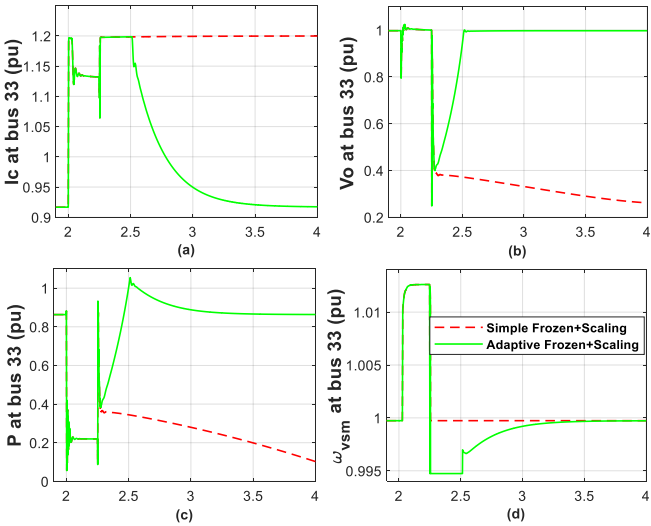


Fig. 9. Performance of grid-forming converter at bus 33, subject to a 250 ms 3-phase fault at bus 19, for different *Frozen* virtual angular speed options.

bus 33. It is seen from Fig. 9(a) that under *Simple Frozen + Scaling* the current of the converter at bus 33 is not saturated for most of the duration of the fault, so ω_{vsm} increases, Fig. 9(d), causing the converter *dq* coordinate to rotate

anticlockwise. Hence, after the fault is cleared the converter becomes current saturated, and the voltage and active power do not recover to pre-fault levels, but remain low, Fig. 9(b)(c). However, under *Enhanced Frozen + Scaling*, due to ω_{vsm} being frozen to a smaller value after the fault clears, Fig. 9(a) shows that the current begins to exit saturation ≈ 0.25 s after the fault is cleared, during which the voltage and active power output increase, Fig. 9(b)(c).

V. CONCLUSION

Under fault conditions, grid-forming converters will not always exit current saturation after a fault clears by simply freezing the virtual angular speed to pre-fault value or ω_0 when the converter is in current saturation, mainly due to the rotation of the converter *dq* coordinates from their pre-fault position. Consequently, the “grid-forming” functionality of the converter is affected. A readily implementable solution has been proposed here to freeze the virtual angular speed to a slightly reduced value after fault clearance, to return the *dq* coordinates to their original position. Freezing the virtual angular speed, in conjunction with current reference limiting and anti-windup integration, is straightforward to implement, and can strictly limit the converter current while enhancing transient stability. The effectiveness of the proposed solution has been verified on a modified simulation of the IEEE 39-bus power system, and future work is planned to further confirm the benefits of the approach on an Opal-RT system.

APPENDIX

TABLE I GRID-FORMING CONVERTER LCL FILTER AND CONTROL PARAMETERS

Parameter	Value (pu)	Parameter	Value (pu)
$R_f, L_f, C_f,$ R_c, L_c	0.005, 0.15, 0.066, 0.005, 0.15	$k_{pv}, k_{iv}, k_{pi}, k_{ii}$	0.52, 1.161022, 0.7388, 1.19
m_p, m_q, ω_0	0.02, 0.0001, 1	$I_{nom}, I_{max}, \epsilon_{db}$	1, 1.1 or 1.2, 0.01
ω_c, T_Q	62.8 rad/s, 1/31.4 s	$K_{VI}, K_{X/R}, \epsilon$	0.67, 5, ± 0.005

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