Dual-Band Three-Way Doherty Power Amplifier Employing Dual-Mode Gate Bias and Load Compensation Network

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***Abstract*—This article presents a new method to design dual-band three-way Doherty power amplifiers (DPAs). A novel modified load modulation network (LMN) is constructed for enabling dual-mode Doherty operation with three-way configuration, providing enhanced high efficiency range in both modes. Moreover, a parallel load compensation network (LCN) is employed in the proposed three-way DPA to provide wideband performance in each operation band. A three-way dual-mode DPA using commercial GaN HEMTs is then designed and manufactured to verify the proposed architecture. Frequency bands of 1.45-1.9 GHz in Mode I and 0.75-1.0 GHz in Mode II are achieved by the DPA, respectively. The fabricated DPA has a 9-dB output back-off (OBO) efficiency of 42.8%-57.7% and a saturated efficiency of 55.4%-70.1%. When driven by a 20-MHz long term evolution (LTE) modulated signal with 8-dB peak-to-average ratio (PAPR), the adjacent channel power ratio (ACPR) of the fabricated DPA is better than -49.9 dBc after digital predistortion at 0.9 GHz and 1.7 GHz with average efficiency of 45.7% and 54.6%.**

***Index Terms*—5G, broadband, Doherty power amplifier (DPA), dual-mode, dual-band, load compensation, three-way.**

I. Introduction

With increasing demands for high-speed and large-scale data transmission, more complex modulation schemes and wide transmission bandwidth are required in modern wireless communication systems, which poses significant challenges in designing radio frequency (RF) power amplifiers (PAs) with stringent average efficiency requirement. The Doherty power amplifier (DPA) [1] architecture provides an effective solution to improve the efficiency at output back off (OBO) point, so that the PA can maintain high efficiency performance when amplifying signals with high peak to average power ratio (PAPR). Thanks to its simple structure and high reliability, the DPA architecture has become one of the most widely used PA architectures in wireless systems during the past decades [2]–[15].

With the rapid development of wireless communication systems, more and more frequency bands are deployed for different standards, and the related frequency distribution is complex and diverse [16], [17]. Therefore, PAs, including DPAs, are expected to cover multiple frequency bands for saving costs and reducing complexity of the entire wireless transmitters. In recent years, many scholars have conducted research on expanding the bandwidth of DPAs. By introducing techniques such as continuous-mode operations [5], [6], post-matching architectures [7]–[9], integrated compensating reactance [10], [11], complex combing loads [18], [19] and dual-input method [12]–[14], the bandwidth of DPA has been greatly expanded. Other PA architectures, such as load modulated balanced amplifiers (LMBAs), have also been proposed recently [20]–[25]. Although the reported LMBAs can achieve high performance cross wide bandwidth, the circuit structure of LMBA becomes complex if more frequency bands need be covered. In summary, despite recent efforts to extend the PA bandwidth while maintaining large high efficiency ranges, it is still difficult to design a PA with operation bands separated by more than one octave and with enhanced back-off efficiency at the same time. To meet this challenge, the dual-band/multi-band DPA architectures have been used as an option to support different wireless communication standards. Techniques such as frequency-dependent design [26]–[28], direct-matching transformer [29] and multi-band coupled networks [30] have been applied and successfully make the DPA work in multiple frequency bands. Unfortunately, these designs are usually narrowband in each operation band.

Recently, a new architecture, named reciprocal gate bias DPA, has been proposed in [31]–[33], and it shows excellent bandwidth expansion capability and multi-band functions by changing the bias conditions for the carrier and peaking PAs. However, in order to achieve the dual-mode gate bias switching configuration, a strict symmetrical structure with same carrier and peaking devices and drain supply voltages has to be adopted. This symmetrical configuration limits the high efficiency range of the reciprocal gate bias based DPAs to 6 dB at most of the operation frequencies, which limits the application of the architecture since signals with 8-12 dB PAPR are more widely used in the practical systems. It is conceivable that the dual-mode gate bias approach can not

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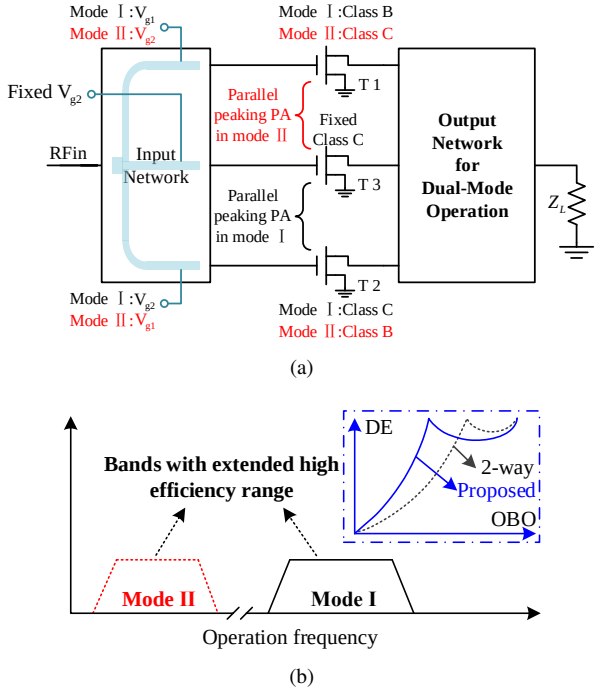


Fig. 1. Proposed three-way DPA architecture: (a) Block diagram; (b) Frequency bands coverage.

be directly deployed in the common design of DPAs with high-efficiency range enhancement, such as asymmetrical [34] and multi-way DPA architectures [35]–[38]. It is thus worth to explore how to improve the high efficiency range of dual-mode gate bias based DPAs while maintaining wide bandwidth performance in each mode.

In this article, we propose a novel dual-band three-way DPA architecture with an enhanced high efficiency range. A modified load modulation network (LMN) is created to enable wideband three-way Doherty operation with the reciprocal gate bias configuration, so that a new dual-mode dual-band DPA architecture can be constructed. Moreover, a load compensation network (LCN) is further employed to improve the wideband performance in each operation mode. It is illustrated that, the proposed three-way DPA can realize two wideband working modes corresponding to different operating frequencies with a large high efficiency range. To verify the proposed architecture, a three-way dual-mode DPA is designed and implemented using commercial GaN-HEMTs. The PA can operate at 1.45-1.9 GHz in Mode I and 0.75-1.0 GHz in Mode II, respectively. A 9 dB high efficiency range and more than 25% fractional bandwidth in each mode have been achieved.

The remaining part of this article is organized as follows. Section II introduces the theoretical analysis of the proposed DPA. Section III presents the detailed procedures for designing the DPA using commercial GaN transistors. The measurement results is given in Section IV with a conclusion in Section V.

II. Theoretical Analysis

The three-way DPA can achieve high efficiency at a large output power back-off, but bandwidth extension for three-way DPAs has always been a difficult problem due to the relatively more complex architecture. Designing broadband or multi-band three-way LMNs is undoubtedly more challenging compared to that for the two-way DPAs. Moreover, to effectively utilize the reciprocal gate bias approach [31]–[33] to extend bandwidth, the LMN must be compatible with the dual-mode gate bias configuration. To enable dual-mode operation while achieving wideband performance and high efficiency, the system architecture of the DPA must be carefully chosen and the output network needs to adopt a new design strategy.

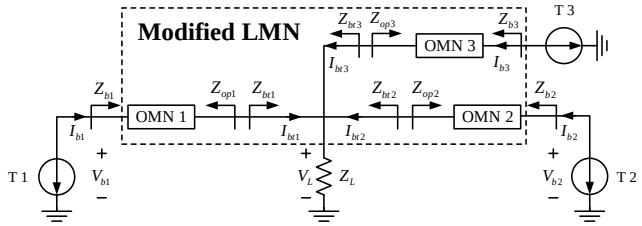


Fig. 2. Theoretical block diagram of the proposed three-way dual-mode DPA.

Fig. 1(a) presents the block diagram of the proposed three-way dual-mode DPA. Three identical transistors (T1, T2 and T3) are combined through an specific output network. For the proposed architecture, Doherty operation in different modes is expected to be achieved at different frequency bands by switching the gate biases of T1 and T2. In Mode I, transistor T1 is biased in Class-B as carrier active device with a gate bias voltage of V_{g1}, transistors T2 and T3 have the same gate bias voltage of V_{g2} and are working in Class-C mode as parallel peaking active devices. In Mode II, the output network is the same, but the transistor T2 is biased in Class-B as carrier active device with a gate bias voltage of V_{g1}, transistors T1 and T3 have the same gate bias voltage of V_{g2} and are working in Class-C mode as parallel peaking active devices. The frequency responses of the employed output network are different at different frequency bands. With proper design, a higher frequency band in Mode I and a lower frequency band in Mode II can be achieved as shown in Fig. 1(b). Meanwhile, the high efficiency range in each mode can be greatly improved because of the three-way structure. To realize the proposed operation, the output network in Fig. 1(a) has to be specially designed, providing three-way Doherty operation in both the two modes. In the following analysis, we will first explain how to build the output network to meet dual-mode operation, and then introduce a load compensation network (LCN) to further improve wideband performance of the proposed DPA.

A. Dual-Mode Three-Way DPA With Dual-Band Performance

To implement the proposed idea, we propose a symmetric three-way configuration shown in Fig. 2, where generalized output matching networks (OMNs) are employed for all the three amplifier branches to form a modified LMN and the transistors are represented by current generators (CGs). The package and parasitic parameters of transistors are assumed to be absorbed in the OMNs and all these OMNs are matched to Z_0 at their individual port. The dual-mode operation is achieved by switching the gate biases of T1 and T2. This

means that the carrier PA and the back-off impedance at OBO in Mode I are different from those in Mode II. In Mode I, T2 and T3 can be regarded as open-circuits at OBO, and the back-off impedance is Z_{b1}, while in Mode II, T1 and T3 can be regarded as open circuits at OBO, and the back-off impedance is Z_{b2}. Since Mode I and Model II use the same networks, the three OMNs must be properly designed to support the dual-mode DPA operation.

Let us assume the OMNs are lossless and the related phase shift is θ_M, the ABCD matrix of a single OMN can thus be expressed as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta_M & j Z_0 \sin\theta_M \\ j\dfrac{\sin\theta_M}{Z_0} & \cos\theta_M \end{bmatrix} \tag{1}$$

In the proposed configuration, Z_0 is set to the optimal impedance (R_{opt}) for running Class-B operation.

It is obvious that the voltage at the combining node can be calculated as,

$$V_L = (I_{bt1} + I_{bt2} + I_{bt3}) \times Z_L \tag{2}$$

where I_{bt1}, I_{bt2} and I_{bt3} are the currents flowing through the OMNs to the combining point and Z_L is the combining load. To meet the impedance condition of load modulation, the value of Z_L should be set to $Z_0/3$, and the current condition of $I_{bt1,sat} = I_{bt2,sat} = I_{bt3,sat}$ should be satisfied at saturation.

According to the characteristics of the ABCD matrix, the following voltage and current relationship can be obtained,

$$\begin{bmatrix} V_b \\ I_b \end{bmatrix} = \begin{bmatrix} \cos\theta_M & j Z_0 \sin\theta_M \\ j\dfrac{\sin\theta_M}{Z_0} & \cos\theta_M \end{bmatrix} \begin{bmatrix} V_L \\ I_{bt} \end{bmatrix} \tag{3}$$

where V_b and I_b represent the voltage and current at the CG plane for each transistors. Therefore, I_b can be calculated as,

$$I_b = j\frac{\sin\theta_M}{Z_0} \times V_L + \cos\theta_M \times I_{bt} \tag{4}$$

Substituting (2) into (4), the relationship between I_b and I_{bt} at saturation can be expressed as,

$$I_{b,sat} = I_{bt,sat} \times (j\,\sin\theta_M + \cos\theta_M) = I_{bt,sat}\, e^{j\theta_M} \tag{5}$$

In order to ensure the phase balance when the current is combined, the current needs to meet the following condition,

$$I_{b1,sat} = I_{b2,sat} e^{j(\theta_{M1} - \theta_{M2})} = I_{b3,sat} e^{j(\theta_{M1} - \theta_{M3})} \tag{6}$$

This phase condition can be satisfied by adding a phase compensation network in the input network, and is only related to the phase shift of the OMNs, which means, it can be applied in both Mode I and Mode II. When the condition (6) is met at saturation, the equivalent impedance for each branch at the combining point can be calculated as,

$$Z_{bt,sat} = \frac{V_{L,sat}}{I_{bt,sat}} = Z_0 \tag{7}$$

Since the equivalent characteristic impedance of the OMNs is set to Z_0, all the impedances matched to the CG planes at saturation, $Z_{b1,sat}$, $Z_{b2,sat}$ and $Z_{b3,sat}$, are equal to Z_0. Therefore, all the three branches can be matched to R_{opt} at saturation, no matter what working mode they are operated on.

In Mode I, the transistor T1 is turned on as the carrier device, the other transistors are all in off-state and appear an open circuits at the CG planes at OBO. Therefore, the output impedance Z_{op} of branch 2 and 3 can be calculated as $Z_{op2} = -jZ_0 \cot\theta_{M2}$ and $Z_{op3} = -jZ_0 \cot\theta_{M3}$. Then, the impedance of branch 1 at the combining load at OBO, $Z_{bt1,OBO}$ can be calculated as,

$$Z_{bt1,OBO} = \frac{Z_0}{3 + j(\tan\theta_{M2} + \tan\theta_{M3})} \tag{8}$$

For OMN1, the impedance relationship at its two ports can be described as,

$$Z_{b1,OBO} = Z_0 \frac{Z_{bt1,OBO} + jZ_0 \tan\theta_{M1}}{Z_0 + jZ_{bt1,OBO} \tan\theta_{M1}} \tag{9}$$

Substituting (8) into (9) we can obtain,

$$Z_{b1,OBO} = jZ_0 \frac{\tan\theta_{M1}(\alpha - \tan\theta_{M1}) - 1}{\alpha} \tag{10}$$

where parameter α is only related to the phase shift of OMNs, and is defined as follows to simplify the analysis,

$$\alpha = \tan\theta_{M1} + \tan\theta_{M2} + \tan\theta_{M3} - 3\,j \tag{11}$$

For conventional single-mode DPAs, θ_{M1} should be set to 90° at center frequency to realize the impedance inversion function. θ_{M2} is usually set to 180° to ensure that Z_{op2} behaves as an open circuit when transistor T2 is off. These two settings are retained in the proposed DPA configuration. For θ_{M3}, since it is still necessary to ensure that Z_{op3} remains open when transistor T3 is off at the center frequency in Mode I, θ_{M3} can thus be considered as an integer multiple of 180°. Moreover, it can be assumed that the OMN phase shift is a linear function of frequency as written in equation (12),

$$\theta = \frac{\theta_{f_0}}{f_0} f \tag{12}$$

where θ_{f_0} is the phase shift of the network at f_0. This assumption can greatly reduce the complexity of analysis while preserving the phase-frequency characteristics of the network composed of transmission lines (TLs). By using TLs, it is easy to design a network that approximates the above assumptions. However, under normal circumstances, the phase characteristics of the TLs composed network will present a larger slope, which will make the bandwidth of the actual designed network smaller than the theoretical analysis [31], [33]. After the phase shift at f_0 of OMNs is determined, $Z_{b1,OBO}$ at any frequency can be then determined according to (10), (12).

θ_{M1} and θ_{M2} at f_0 have been selected to 90° and 180°, and θ_{M3} is expected to be an integer multiple of 180°. If θ_{M3} is selected with different values, $Z_{b1,OBO}$ will have different frequency responses. Based on (10) and (12), Fig. 3 presents how the resistance of $Z_{b1,OBO}$ varies with frequency when θ_{M3} is set to 180°, 360°, 540° and 720° at f_0. As θ_{M3} increases, $Z_{b1,OBO}$ changes more and more drastically with frequency, so it can be easily inferred that the larger the θ_{M3}, the smaller the bandwidth that can support the normal operation of the DPA. Therefore, only for Mode I, setting θ_{M3} to 180° maybe

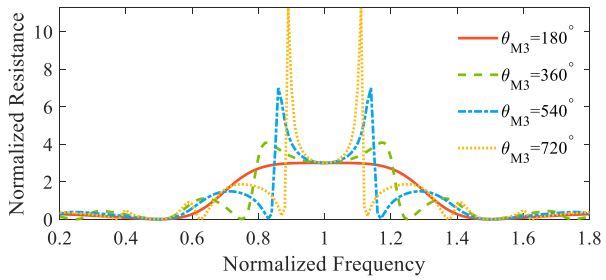


Fig. 3. Normalized OBO resistance versus normalized frequency in Mode I when θ_{M3} takes 180°, 360°, 540° and 720° respectively.

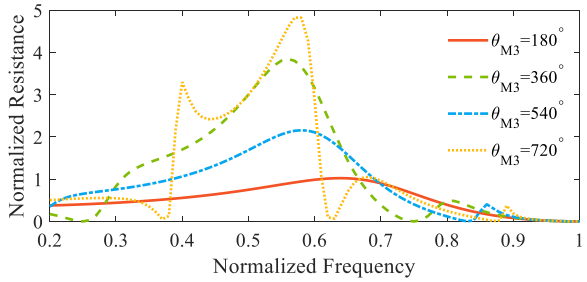


Fig. 4. Normalized OBO resistance versus normalized frequency in Mode II when θ_{M3} takes 180°, 360°, 540° and 720° respectively.

the best choice, but for a dual-mode DPA, it is also necessary to consider the performance of the DPA in Mode II.

In Mode II, the transistor T2 is turned on as the carrier device at OBO, while the other transistors are off and appear as open circuits at the CG planes. Therefore, the back-off impedance in Mode II can be calculated as,

$$Z_{b2,OBO} = jZ_0 \frac{\tan\theta_{M2}\,(\alpha - \tan\theta_{M2}) - 1}{\alpha} \tag{13}$$

Similar to the analysis in Mode I, $Z_{b2,OBO}$ will have different frequency responses if θ_{M3} is selected with different values. Fig. 4 shows how the resistance of $Z_{b2,OBO}$ varies with frequency when θ_{M3} is set to 180°, 360°, 540° and 720° at f_0. The best solution of θ_{M3,f_0} = 180° in Mode I is not suitable for Mode II, because the resistance at OBO in Mode II is very low, which will greatly reduce the OBO range. In contrast, when θ_{M3,f_0} = 360° or θ_{M3,f_0} = 720°, there is a relatively reasonable OBO resistance, which can provide enough OBO range. Combining the impedance frequency response of the two working modes at OBO in Fig. 3 and Fig. 4, the final value of θ_{M3} is selected as 360° at the center frequency in Mode I to provide the best dual-band performance.

Once the values of θ_{M1}, θ_{M2} and θ_{M3} at f_0 have been determined, the phase shift of the three OMNs can then be calculated according to (10) and (12). Fig. 5(a) shows how the real and imaginary part of $Z_{b1,OBO}$ vary with frequency in Mode I. It can be seen that the impedance condition of the DPA at OBO can be well satisfied in a wide bandwidth near f_0 in Mode I. Fig. 5(b) shows how the real and imaginary part of $Z_{b2,OBO}$ vary with frequency in Mode II. Different from Mode I, in Mode II, there is a frequency band below f_0 that can meet the impedance requirement of the DPA at OBO.

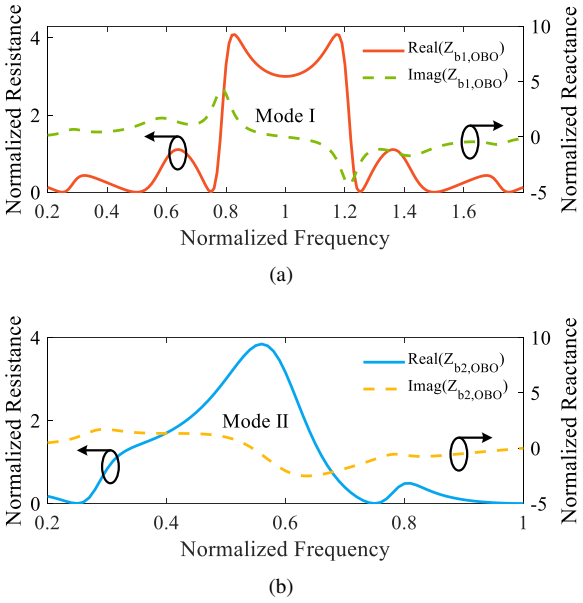


Fig. 5. Normalized OBO impedance versus normalized frequency without LCN in (a) Mode I and (b) Mode II.

Therefore, the proposed DPA architecture can indeed achieve the dual-mode dual-band operation. However, in Mode II, the real part of $Z_{b2,OBO}$ presents a sharper peak within the working band. This means that the resistance changes drastically, which will deteriorate the broadband performance in Mode II. In the following analysis, we will discuss the possibility to further improve the broadband performance in Mode II by introducing an added compensation network to the combining load.

B. Bandwidth Extension in Mode II Using Load Compensation Network

In order to extend the bandwidth in Mode II, a feasible solution of connecting a compensation network in parallel to the combining load is proposed in this article. Fig. 6 shows the OBO state of the modified LMN in Mode I and Mode II after adding LCN. The resistance change of $Z_{b2,OBO}$ in the working frequency band in Mode II is expected to be flattened, so that the broadband performance of the PA in Mode II could be improved.

Suppose that the equivalent characteristic impedance of the LCN in Fig. 6 is Z_p, the LCN phase shift is θ_p, the LCN can also be represented by a transmission matrix as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta_p & jZ_p\sin\theta_p \\ j\dfrac{\sin\theta_p}{Z_p} & \cos\theta_p \end{bmatrix} \tag{14}$$

The combining load will thus be replaced by Z_{LC}, which is equal to the parallel of Z_L and LCN impedance as,

$$Z_{LC} = \frac{Z_0 Z_p}{3Z_p - jZ_0\cot\theta_p} \tag{15}$$

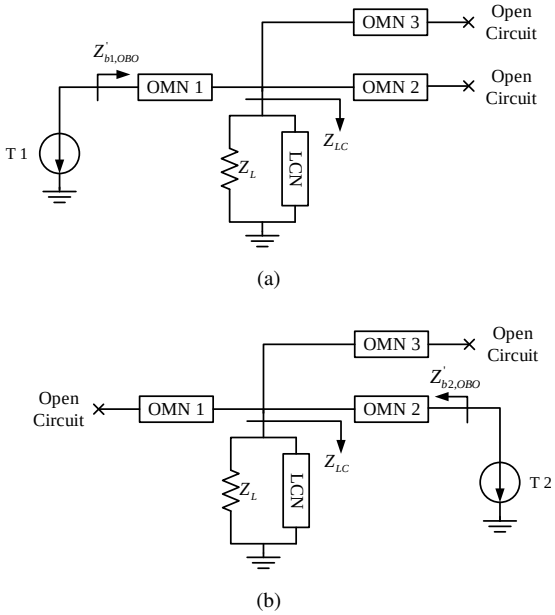


Fig. 6. The OBO state of the modified LMN in Mode I (a) and Mode II (b) after adding LCN.

Therefore, the impedance at OBO in Mode I and Mode II after adding LCN can be calculated as,

$$Z'_{b1,OBO} = \frac{jZ_0\left\{Z_p + \tan\theta_{M1}\left[Z_0\cot\theta_p - Z_p\left(\alpha - \tan\theta_{M1}\right)\right]\right\}}{Z_0\cot\theta_p - Z_p\alpha} \tag{16}$$

$$Z'_{b2,OBO} = \frac{jZ_0\left\{Z_p + \tan\theta_{M2}\left[Z_0\cot\theta_p - Z_p\left(\alpha - \tan\theta_{M2}\right)\right]\right\}}{Z_0\cot\theta_p - Z_p\alpha} \tag{17}$$

The phase shift of LCN can also be set as a function of frequency according to (12), so that the impedance frequency response of LCN can be obtained. Different impedance frequency responses can also be obtained based on different values of Z_p and θ_p. Fig. 7 shows the frequency responses of $Z'_{b1,OBO}$ and $Z'_{b2,OBO}$ corresponding to different values of θ_p when Z_p is fixed to Z_0. With the change of θ_p, the frequency response of the impedance has changed significantly, which means that if the values of Z_p and θ_p are appropriately selected, the broadband performance of the proposed DPA can be greatly improved.

In order to analyze the broadband characteristics more intuitively for selecting the appropriate values of Z_p and θ_p, the concept of "Power Bandwidth (PB) " [31], [39], [40] is introduced here, and the impedance value is used as the criterion to quantitatively calculate the bandwidth. To ensure that the output power of the PA falls within the range of δ dB compared to the situation when it is matched to the optimal OBO impedance, the matching impedance and admittance at the CG plane should meet the following two conditions at the same time,

$$\mathrm{Re}(Z_{OBO}) \geq nR_{opt}10^{-\delta/10} \tag{18}$$

$$\mathrm{Re}(Y_{OBO}) \leq \frac{10^{-\delta/10}}{nR_{opt}} \tag{19}$$

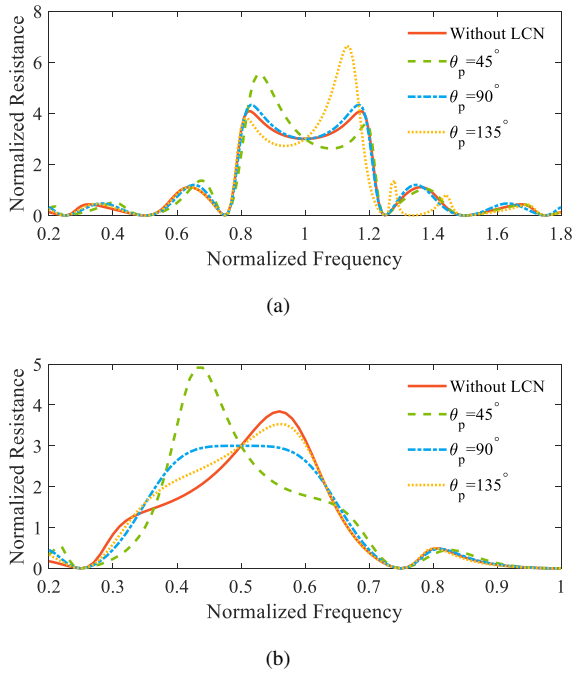


Fig. 7. Normalized OBO resistance versus normalized frequency of Mode I (a) and Mode II (b) with fixed $Z_p = Z_0$ compared with when there is no LCN.

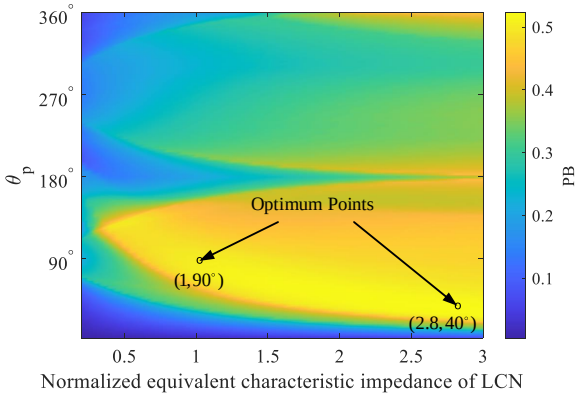
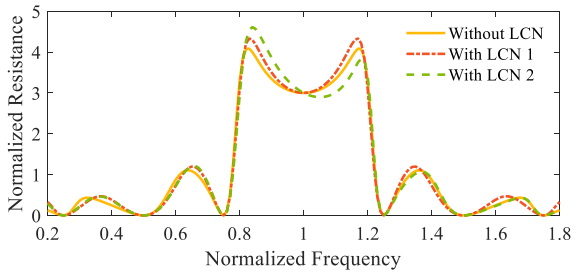


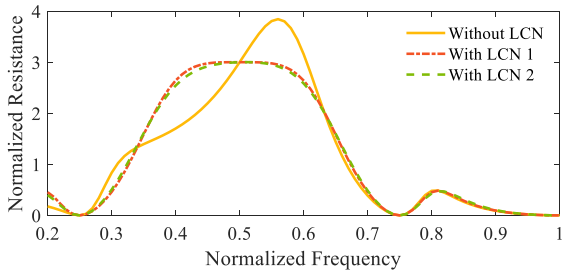
Fig. 8. The relationship between Z_p, θ_p and PB.

where n represents the ratio of R_{opt} to the impedance that should be matched at OBO. This means when both (18) and (19) are satisfied, the output power of the PA will drop no more than δ dB. We set the value of n to 3 and the value of δ to 1. Therefore, the set of all frequency points that meet the impedance and admittance condition is regarded as the PB of this network. By setting different values of the LCN parameters Z_p and θ_p, a series of impedance values can be obtained, and the related PB will also change. Scan Z_p and θ_p, record the PB in both Mode I and Mode II, sum them up and we can record the total bandwidth. Fig. 8 shows the scan results of Z_p from 0.2 to 3, θ_p from 2° to 360°, where Z_p is normalized to Z_0.

Fig. 8 is a very intuitive display of the relationship between the total PB, Z_p and θ_p. By observing the calculation results, it can be found that the total PB is more sensitive to the change



(a)



(b)

Fig. 9. Normalized OBO resistance versus normalized frequency of Mode I (a) and Mode II (b) with and without LCN.

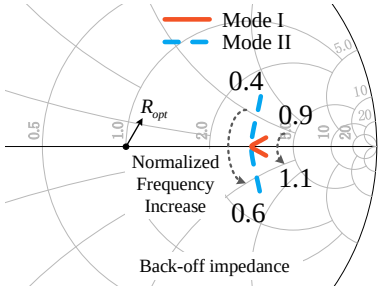


Fig. 10. Back-off impedance of Mode I and Mode II after adding LCN on the Smith chart.

of θ_p, and the values of Z_p and θ_p can be selected in a large area, which provides great flexibility for circuit design and implementation. Two "best solutions" with almost the same PB were found in the calculation results, namely solution 1: $Z_p = 1$, $\theta_p = 90°$ and solution 2: $Z_p = 2.8$, $\theta_p = 40°$. For these two special cases, the results of the achieved OBO resistance is shown in the Fig. 9, where LCN1 is corresponding to solution 1 and LCN2 corresponding to solution 2. Both LCN 1 and LCN 2 have brought significant improvements in the bandwidth in Mode II and did not have much impact on Mode I. In the following analysis and design verification, the LCN 1 is adopted and verified.

Fig. 10 shows the back-off impedance in Mode I and Mode II after adding LCN on the Smith chart. In Mode I, the working frequency band is centered on f_0, and in Mode II, the working frequency band is centered on $0.5f_0$. It is manifested in Fig. 9 that after adding the LCN, the change in Mode I is very small, while in Mode II, the impedance change is significantly smoother.

After connecting to the selected LCN, the normalized OBO impedance at center frequency f_0 and $0.5f_0$ can be calculated by formulas (16) and (17) as 3, and the relationship between the output power at the OBO point P_{OBO} and the output power at the saturation point P_{SAT} can be written as $P_{OBO} = 1/9P_{SAT}$. The OBO range at the center frequency in Mode I and Mode II can be calculated as,

$$\mathrm{OBO} = 10\log\frac{\mathrm{P_{SAT}}}{\mathrm{P_{OBO}}} = 9.54 \tag{20}$$

Because of the use of parallel peak PAs, the OBO range of the proposed DPA can be greatly increased. It should be noted that the OBO range of the proposed DPA is slightly different at different operating frequencies. We use 9 dB for OBO performance validation in the following designs.

III. Circuit Design

To verify the theory proposed in the previous section, commercial GaN HEMTs CGH40010F form Wolfspeed are used to manufacture a three-way dual-mode DPA on 20 mil thick Rogers 4350 substrate with a dielectric constant of 3.66. In this design, the drain supply voltage is set to 28 V, and the gate bias is $V_{g1} = -3$ V, $V_{g2} = -5.5$ V. The knee voltage of CGH40010F is about 4.5 V, and the maximum current is about 1.6 A. It can be calculated that R_{opt} is about 30 Ω. In Mode I, the gate bias of transistor T1 is set to −3 V to make it work in class B mode, and the gate biases of transistors T2 and T3 are set to −5.5 V, make them work in class C mode. The target working frequency band is 1.45−1.9 GHz. In Mode II, the gate voltages of transistors T1 and T2 are swapped and T3 maintains working in class C state. The target working frequency band is 0.75-1 GHz.

A broadband three-way power divider is designed firstly to distribute the input power to three ways. A third-order three-way planar Wilkinson power divider is adopted to ensure good power distribution in a wide frequency band of 0.7-2.0 GHz, covering Mode I and Mode II. Because three same transistors were used, the same input matching networks (IMNs) were deployed to simplify the design process. The use of same IMNs also made the design of phase compensation network become easier. A bias resistor is added to increase the stability of the circuit. The phase compensation network can be composed of TLs of different lengths with a characteristic impedance of 50 Ω. In order to satisfy the condition of formula (6), while taking into account the needs of layout, the lengths of the three microstrip lines that make up the phase compensation network were selected as 25.31 mm, 75.71 mm, and 104.85 mm.

After designing the input networks, the OMNs of the proposed DPA were build. Due to the impact from non-linearity of the transistor, the parasitic and package parameters, the transistors cannot be directly equivalent to an ideal CG as shown in Fig. 2. An equivalent parasitic and package network should be added between the CG plane and the package plane. Fig. 11 shows the equivalent parasitic and package network of CGH40010F. When designing the OMNs, this network should be absorbed into the OMNs. From the calculation in the previous section, we can see that the phase shifts at f_0 of OMN1, OMN2, and OMN3 are 90°, 180°, 360°, and the phase characteristic versus frequency is determined by (12).

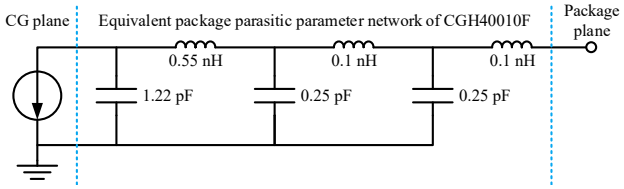


Fig. 11. Equivalent parasitic and package network of CGH40010F.

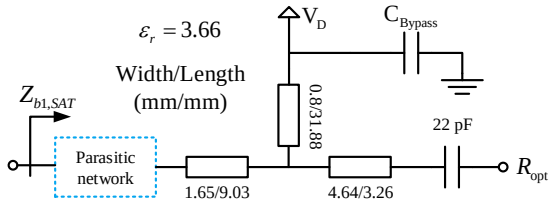
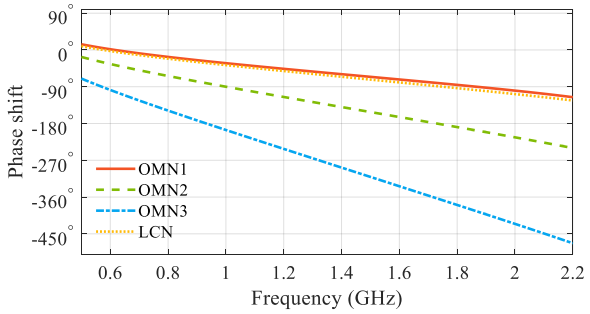
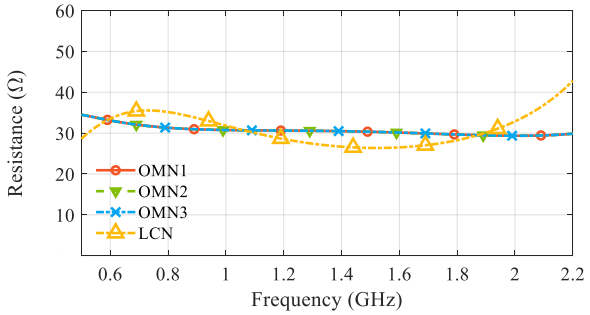


Fig. 12. Circuit of the designed EQWN.



(a)



(b)

Fig. 13. Parameters of the designed output network: (a) Phase shift of designed OMNs and LCN. (b) Matching resistance of designed OMNs and LCN when their loads equal to Z_0.

The equivalent characteristic impedance of the three OMNs are all R_{opt}. To implement the circuit more conveniently and maintain the consistency of the characteristic impedance of the three OMNs, an equivalent quarter wavelength network (EQWN) shown in Fig. 12 was designed based on a T-shape TL structure and used as OMN1. When the EQWN is loaded with R_{opt}, the input impedance of this network should also be R_{opt}, and the phase shift at f_0 should be 90°. After completing the design of EQWN, the OMN2 and OMN3 can be realized by adding a tuning TL with characteristic impedance of R_{opt}

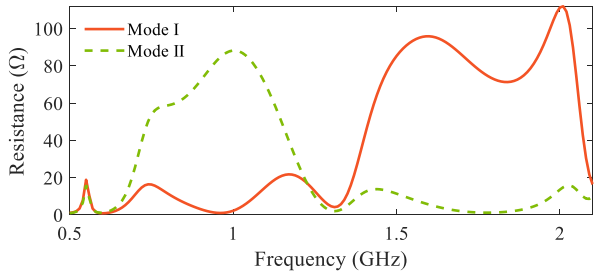


Fig. 14. OBO resistance of the designed DPA.

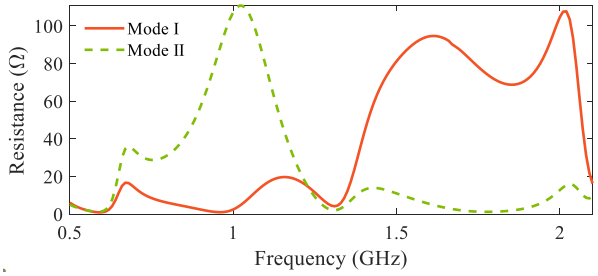
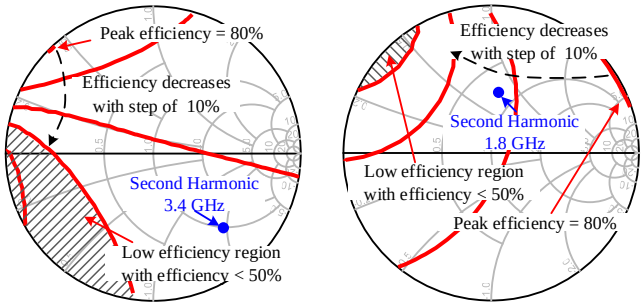


Fig. 15. OBO resistance of the designed DPA without LCN.



(a) (b)

Fig. 16. Second-harmonic impedance of the designed DPA and back-off efficiency contours of the second-harmonic load-pull simulation at (a) 1.7 GHz in Mode I and (b) 0.9 GHz in Mode II.

to the EQWN. The phase shift of the TLs at f_0 should be 90° and 270° respectively. In the actual design, due to the discontinuity caused by the bending of the TLs, the length of the TLs has been optimized to achieve better performance.

The LCN and the post-matching network can be designed together, however, in order to observe the impact of LCN, the LCN and the post-matching network are designed separately in this work. According to the required impedance and phase characteristics of the LCN, the LCN can be designed using a grounded quarter-wavelength TL with characteristic impedance of Z_0. However, the phase of OMNs do not strictly change linearly with frequency, which would have great influence on the phase characteristics of the OMNs. Therefore, it is not suitable to use a section of grounded TL to realize the LCN. In this work, the LCN adopts the same structure as the OMN1, and has achieved the consistency of phase characteristics with OMN1. Fig. 13(a) shows the phase

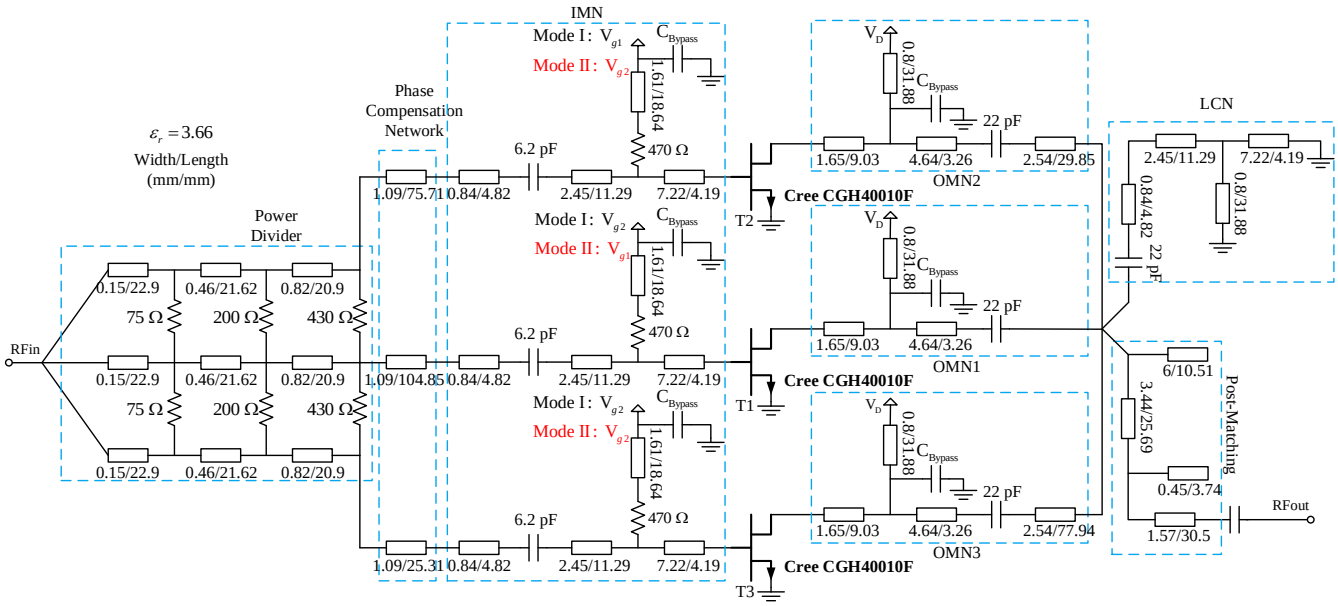
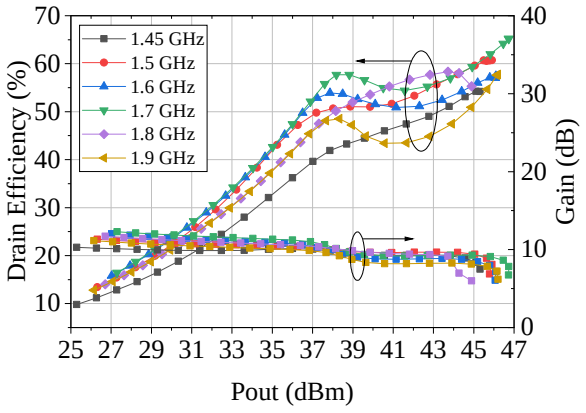
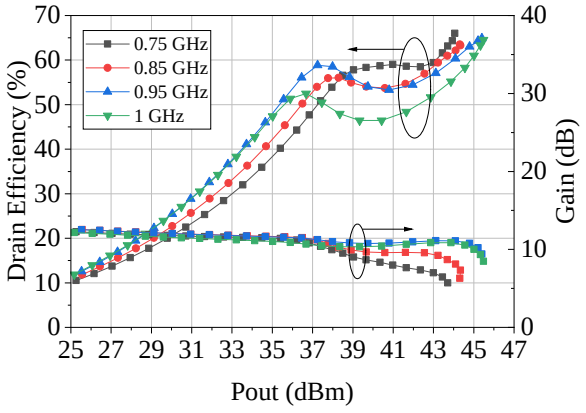


Fig. 17. Complete schematic of the proposed DPA.



(a)



(b)

Fig. 18. Simulated drain efficiencies and gains of the designed DPA versus output power at different frequencies of (a) Mode I carrier and (b) Mode II.

shift of designed OMNs and LCN and Fig. 13(b) shows the matching resistance when OMNs and LCN are loaded with Z_0. Finally, a post-matching network is needed to achieve impedance matching of Z_L to 50 Ω. In order to ensure a good matching within 0.7-2.0 GHz, a high-order low-pass TL topology were used.

Fig. 14 shows the back-off resistance of the designed DPA in Mode I and Mode II. It should be emphasized that it is impractical to completely eliminate the influence of parasitic networks in such a wide frequency range. Therefore, the designed network is slightly different from the theory, while the impact on the performance of the designed DPA is within the acceptable range. For comparison, Fig. 15 shows the back-off resistance when the LCN is disconnected. It can be clearly seen that adding LCN has greatly improved the bandwidth of Mode II and has almost no effect on Mode I. Fig. 16 shows the second-harmonic impedance and back-off efficiency contours of the second-harmonic load-pull simulation at 1.7 GHz in Mode I and 0.9 GHz in Mode II. In these figures, areas with efficiency below 50% on the Smith chart are defined as low efficiency region. It can be seen that, despite the second harmonic impedance is not in the optimal value, it is away from the low efficiency region and thus the level of efficiency reduction is acceptable for such a wideband DPA.

The schematic diagram of the entire design is shown in Fig. 17. All the size of the used TLs and lumped components are also given. The simulation results of drain efficiency and gain in Mode I and Mode II are shown in Fig. 18(a) and Fig. 18(b), respectively. In Mode I, the saturated drain efficiency achieves 54.3%-65.3% with a saturated output power of 44.9 dBm to 46.7 dBm, and a drain efficiency of 37%-55.9% is obtained at 9 dB OBO. In Mode II, the saturated drain efficiency achieves 62.2%-66% with a saturated output power of 43.7 dBm to 45.5 dBm, and a drain efficiency of 40.2%-56.1% is obtained at 9 dB OBO. To better observe the operation of the designed

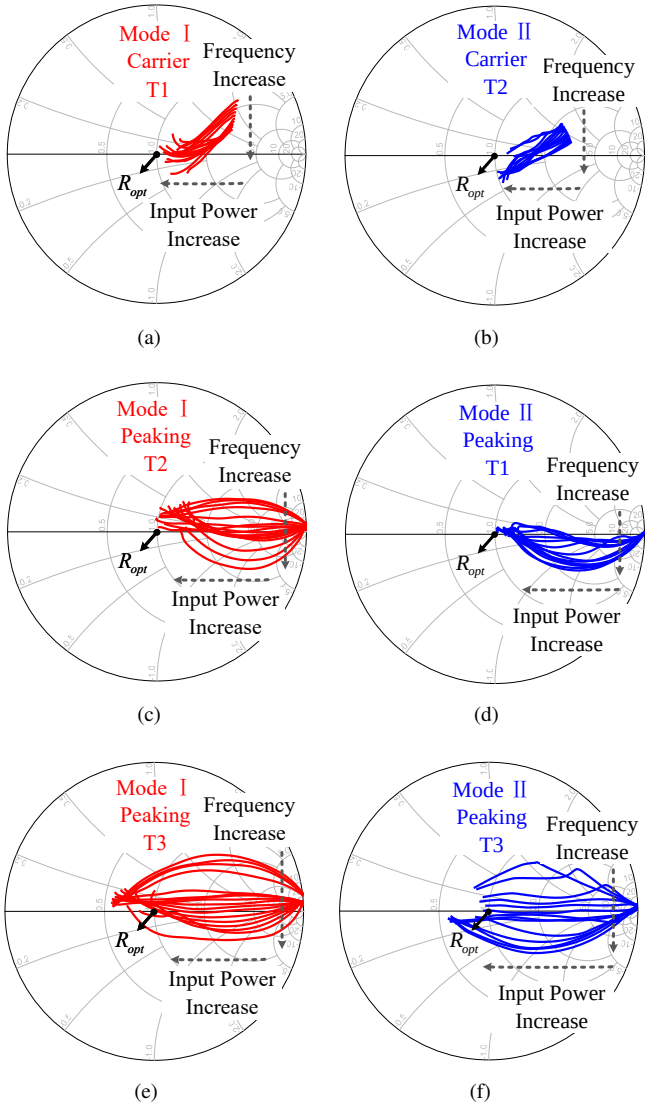


Fig. 19. Simulated load modulation trajectories at CG plane of (a) carrier T1 in Mode I, (b) carrier T2 in Mode II, (c) peaking T2 in Mode I (d) peaking T1 in Mode II, (e) peaking T3 in Mode I and (f) peaking T3 in Mode II.

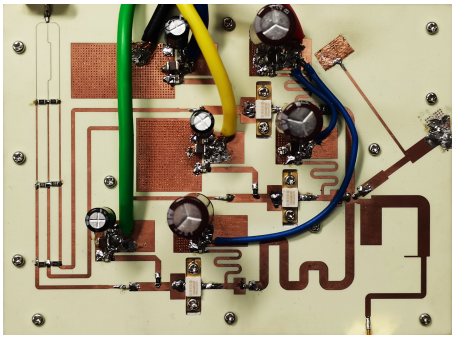


Fig. 20. Photo of the fabricated DPA.

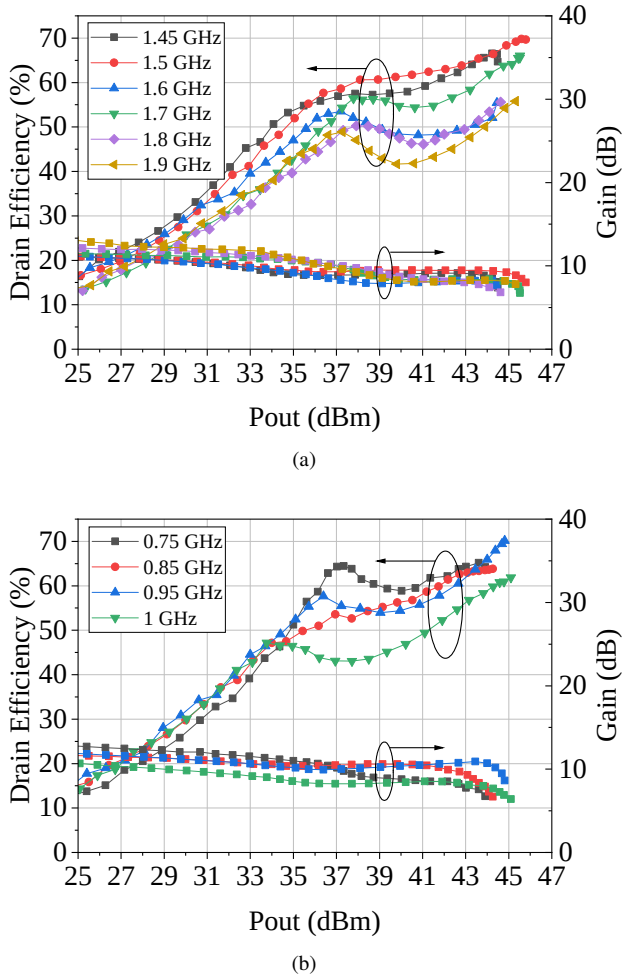


Fig. 21. Measured drain efficiencies and gains of the fabricated DPA versus output power at different frequencies of (a) Mode I and (b) Mode II.

DPA at different frequencies and power levels, we plotted the simulated load modulation trajectories at CG plane of the devices in Fig. 19, where we can see that the designed DPA successfully realizes the load modulation Doherty function in both Mode I and Model II.

IV. Measurements Results

Fig. 20 shows the photo of the fabricated DPA. Measurements of the fabricated DPA have been carried out under continuous-wave (CW) signal and modulated signal in both modes. The measurement results are basically consistent with the simulation, except for some inevitable differences in some data because of the fabrication variations and inaccuracy of simulation. The working bandwidths under Mode I and Mode II obtained from the measurement are 1.45-1.9 GHz and 0.75-1.0 GHz, respectively. During all the measurements, the quiescent current of the proposed DPA is set to 60 mA and the gate bias voltages of the peaking PAs are set to −5.5 V in both Mode I and Mode II with drain supply voltage of 28 V for all the three transistors.

A. Measurements under CW Signal Stimulation

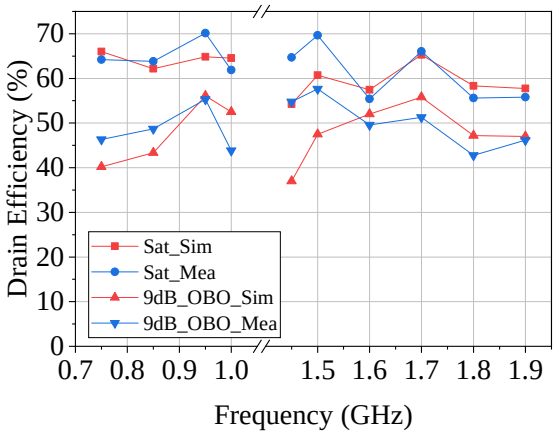


Fig. 22. Simulated (Sat) and measured (Mea) drain efficiency of the fabricated DPA at different frequencies.

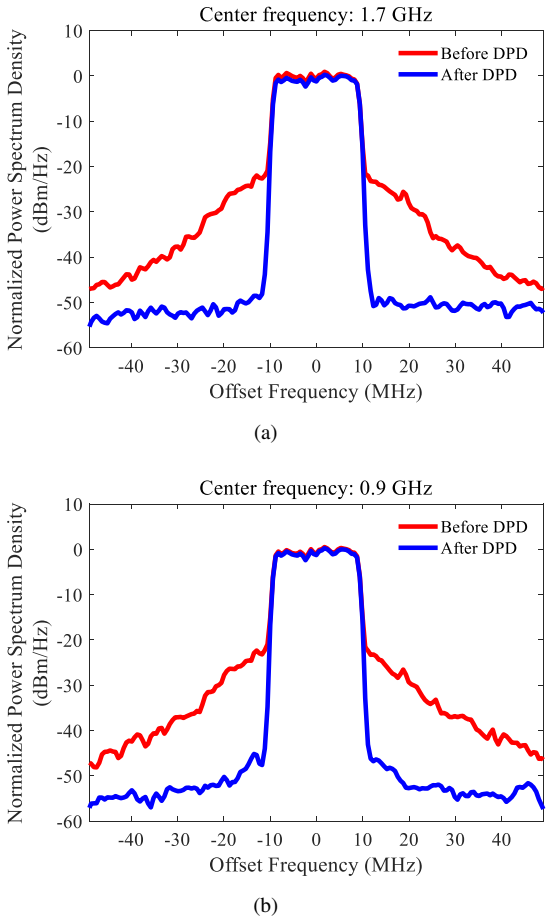


Fig. 23. Measured output spectrum of fabricated DPA before and after DPD at (a) 1.7 GHz and (b) 0.9 GHz.

The measurement under CW signal is performed first. The input signal is generated by a vector signal generator (VSG). In order to obtain sufficient input power, an RF driver is used. The output power is measured by a spectrum analyzer. The measured drain efficiency and gain of the fabricated DPA with respect to the output power are shown in Fig. 21. In Mode I, the saturated drain efficiency achieves 55.4% – 69.6% and the power added efficiency (PAE) achieves 50% – 63% with a saturated output power of 44.45 – 45.8 dBm. The drain efficiency at 9 dB OBO is in the range of 42.8% – 57.7%. 11.5–13.6 dB small-signal gain is obtained in Mode I. In Mode II, the saturated drain efficiency achieves 61.9% – 70.1% and the PAE achieves 54% – 64% with a saturated output power of 43.91 – 45.1 dBm. The drain efficiency at 9 dB OBO is within the range of 43.8% – 55.3%. 11.4 – 13.2 dB small-signal gain is obtained in Mode II. It can be clearly observed from the measurement results that the fabricated PA presents obvious Doherty behaviour with enhanced high efficiency range.

TABLE I
PERFORMANCE OF THE PROPOSED DPA WITH A 20-MHZ MODULATED SIGNAL WITH 8-DB PAPR

Frequency (GHz) (GHz)	Average Pout (dBm)	Average DE (%)	ACPR before DPD (dBc)	ACPR after DPD (dBc)
1.7	34.3	45.7	-27.9/-26.7	-50.3/-50.2
0.9	36	54.6	-27.8/-26.9	-49.9/-50.3

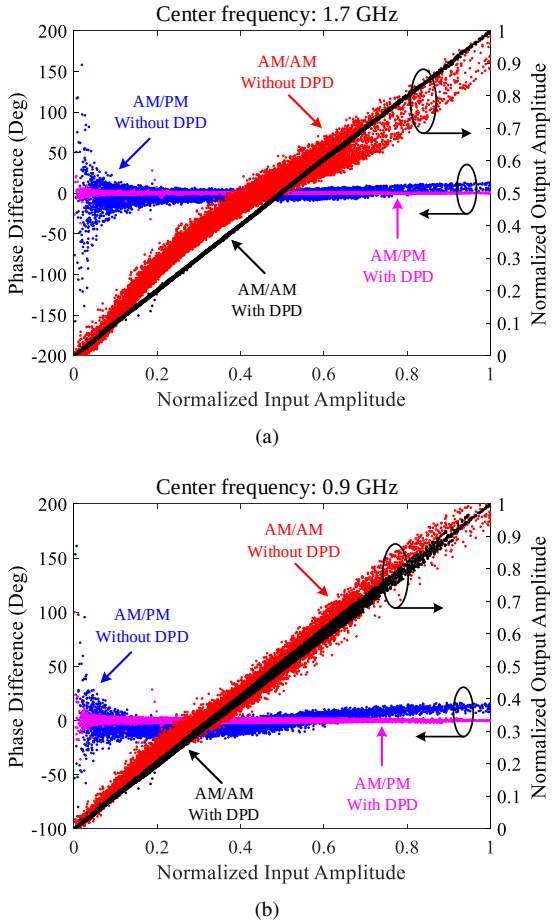


Fig. 24. Measured AM/AM and AM/PM curves of the proposed DPA at (a) 1.7 GHz and (b) 0.9 GHz.

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED MULTI-BAND/BROADBAND DPAS AND LMBAS

Ref. (Year)	Type	Frequency (GHz)	Pmax (dBm)	Gain (dB)	DE_{SAT} (%)	OBO (dB)	DE_{OBO} (%)
[29] 2016	Dual-Band	1.8/2.6	43.7-43.9	10.5-12.1	60-72	6	51-63
[30] 2016	Quad-Band	0.73/1.65/2.67/3.57	41.7-42.5	6-19 *	52.7-43.1	6	44.6-58.9
[11] 2019	Broadband	1.6-2.6	45.5-46	9-11 *	53-66	6/9.5	51-63@6 dB OBO 50-53@9.5 dB OBO
[31] 2019	Dual-Mode Three-Band	2.2-2.7/2.8-4.1/4.2-4.8	39.2-41.0	7.5-11.7	50-72	6	35.0-49.7
[27] 2019	Dual-Band	2.1/3.4	47.5-48	8-10 *	63-72	9	43-50
[28] 2019	Dual-Band	1.4/3.5	42.1-42.5	10-15 *	68-70	9	55-55.1
[33] 2020	Dual-Mode Six-Band	1.52-1.72/1.8-2.2/2.38-2.53/ 3.67-3.82/3.9-4.3/4.53-4.68	39.6-41.5	8.7-13.5	54.4-71.4	6	42.2-56.7
[21] 2018	LMBA	1.7-2.5	48-48.9	9.8-13.5	48-58 **	6/8	43-53@6 dB OBO 39-50@8 dB OBO **
[22] 2020	LMBA	1.45-2.45	45.6-46.7	11.2-13.4	67.1-77.9	6/8	51.2-64.4@6 dB OBO 47.8-55.7@8 dB OBO
[25] 2021	H-ALMBA	1.7-3	42-43	8-12.5 *	63-81	5/10	51-62@5 dB OBO 50-66@10 dB OBO
This work	Dual-Mode Dual-Band	0.75-1/1.45-1.9	43.91-45.8	11.4-13.6	55.4-70.1	9	42.8-57.7

* -Graphically estimated ** -PAE

In order to better demonstrate the broadband performance of the fabricated DPA, drain efficiency at saturation and 9 dB OBO versus frequency are shown in Fig. 22 with simulation results for comparison. The fabricated DPA has achieved relatively higher saturation and OBO efficiency at some of the operation frequencies, while the measurement results are consistent with the simulation data in the overall trend. Due to the inaccuracy of the simulation model and fabrication variations, the measurement results at 1.45 GHz and 1.5 GHz have deviated from the simulation results.

B. Measurements under Modulated Signal Stimulation

In order to present the performance of the fabricated DPA when amplifying modulated signals, an LTE signal with a bandwidth of 20 MHz and a PAPR of 8 dB is used to measure the DPA. Digital pre-distortion (DPD) is performed to improve the linearity of the DPA. The generation of modulated signals, the acquisition and processing of the output signal of the fabricated DPA are completed by using the Xilinx Zynq UltraScale+ RFSoC evaluation board (ZCU111). The generalized memory polynomial (GMP) model is used as the DPD model, and the direct learning structure is used to iterate the coefficients until convergence. Measured output spectrum of the fabricated DPA before and after DPD at 1.7 GHz and 0.9 GHz is shown in Fig. 23. It can be seen that, the linearity of the DPA can be greatly improved after DPD performed.

To better present the performance of the fabricated DPA under modulated signal stimulation, the AM/AM and AM/PM characteristics of the DPA with and without DPD at 1.7 GHz and 0.9 GHz are shown in Fig. 24 and more data are presented in Table I. In Mode I, the center frequency of the modulated signal is 1.7 GHz and the ACPR before DPD is -27.9/-26.7 dBc. After DPD performed, the ACPR can be improved to -50.3/-50.2 dBc with a average output power of 34.3 dBm and average DE of 45.7%. In Mode II, the center frequency of the modulated signal is 0.9 GHz and the ACPR before DPD is -27.8/-26.9 dBc. After DPD performed, the ACPR can be improved to -49.9/-50.3 dBc with a average output power of 36 dBm and average DE of 54.6%.

C. Performance Comparison

Table II compares the performance of the fabricated DPA with some recently published multi-band or broadband DPAs and LMBAs. It can be seen that, the proposed dual-mode DPA achieves large high efficiency range in two largely separated bands, that is usually not possible to achieve in dual-mode DPAs such as [31] and [33]. Compared with other single-mode multi-band DPAs, the proposed architecture shows much better fractional bandwidth in each mode with comparable efficiency performance at both saturation and OBO. When compared with broadband DPAs and LMBAs, the proposed architecture is simpler in order to cover operation bands with a large frequency span. In summary, the proposed dual-mode three-way DPA shows a more balanced performance in various indicators.

V. CONCLUSION

This paper presents the theory and design of a novel dual-band three-way DPA. The dual-mode gate bias DPA design is generalized to three-way DPA architectures for high efficiency range enhancement. Novel LMN and LCN are employed in the proposed DPA to achieve the dual-mode three-way DPA operation, while providing over 25% fractional bandwidth in each mode. The fabricated three-way DPA using commercial

GaN transistors successfully realizes the proposed dual-mode operation with 9 dB high efficiency range. The proposed DPA architecture provides a new approach to designing multi-band PAs with a large high efficiency range.

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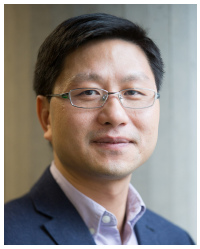

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