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Charge-Domain Signal Processing of Direct RF Sampling Mixer with Discrete-Time Filters in Bluetooth and GSM Receivers

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RF circuits for multi-GHz frequencies have recently migrated to low-cost digital deep-submicron CMOS processes. Unfortunately, this process environment, which is optimized only for digital logic and SRAM memory, is extremely unfriendly for conventional analog and RF designs. We present fundamental techniques recently developed that transform the RF and analog circuit design complexity to digitally intensive domain for a wireless RF transceiver, so that it enjoys benefits of digital and switched-capacitor approaches. Direct RF sampling techniques allow great flexibility in reconfigurable radio design. Digital signal processing concepts are used to help relieve analog design complexity, allowing one to reduce cost and power consumption in a reconfigurable design environment. The ideas presented have been used in Texas Instruments to develop two generations of commercial digital RF processors: a single-chip Bluetooth radio and a single-chip GSM radio. We further present details of the RF receiver front end for a GSM radio realized in a 90-nm digital CMOS technology. The circuit consisting of low-noise amplifier, transconductance amplifier, and switching mixer offers 32.5 dB dynamic range with digitally configurable voltage gain of 40 dB down to 7.5 dB. A series of decimation and discrete-time filtering follows the mixer and performs a highly linear second-order lowpass filtering to reject close-in interferers. The front-end gains can be configured with an automatic gain control to select an optimal setting to form a trade-off between noise figure and linearity and to compensate the process and temperature variations. Even under the digital switching activity, noise figure at the 40 dB maximum gain is 1.8 dB and +50 dBm IIP2 at the 34 dB gain. The variation of the input matching versus multiple gains is less than 1 dB. The circuit in total occupies 3.1 mm². The LNA, TA, and mixer consume less than 15.3 mA at a supply voltage of 1.4 V.

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1. INTRODUCTION

The continuous technology innovation in CMOS forces to integrate more circuits resulting in lower solution price while offering more features [1]. Designing a radio for the wireless and cellular standards with large digital circuitry, such as digital baseband (DBB), application processor, and memory on the same chip becomes a challenging task due to the coupling of the digital spurious noise through silicon substrate, interconnect, and package [2]. While high level of integration impedes achieving a low noise figure, low supply voltage makes linearity hard to achieve.

Recently, we have demonstrated a highly integrated system-on-chip (SoC) in the discrete-time Bluetooth receiver. The receiver architecture [3–6] uses *direct RF sampling* in the receiver front-end path. In the past, only *subsampling* mixer receiver architectures have been demonstrated: they operate at lower IF frequencies [7, 8] and suffer from noise folding and exhibit susceptibility to clock jitter. In this architecture,

discrete-time analog signal processing is used to sample the RF input signal as it is down-converted, down-sampled, filtered, and converted from analog to digital with a discrete-time $\Sigma\Delta$ ADC. This method achieves great selectivity right at the mixer level. The selectivity is digitally controlled by the LO clock frequency and capacitance ratio, both of which are extremely precise in deep-submicron CMOS processes. The discrete-time filtering at each signal processing stage is followed by successive decimation. The main philosophy in architecting the receive path is to provide all the filtering required by the standard as early as possible using a structure that is quite amenable to migration to the more advanced deep-submicron processes. This approach significantly relaxes the design requirements for the following baseband amplifiers.

In this paper, we also present a 90-nm CMOS realization of a GSM receiver [9–11] RF front end incorporating the discrete-time signal processing. The RF front end provides an embedded variable gain amplifier (VGA) function

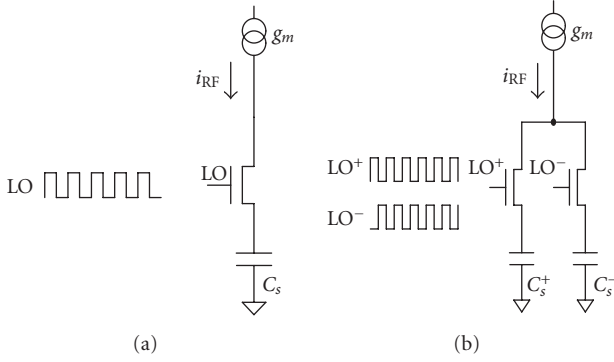


FIGURE 1: Temporal MA operation at RF rate: (a) single-ended, (b) pseudodifferential configurations.

that is digitally configurable and offers fine gain control. The switched capacitor filter (SCF) implements a highly-linear second-order lowpass filter. The input S_{11} is constant over the desired frequency range while achieving 1.8 dB noise figure (NF) in the highest gain setting of 40 dB where the RF front-end circuits consume only 15.3 mA. The gain can be configured with an automatic-gain-control algorithm in the receiver to select an optimal setting with a trade-off between noise figure and linearity and to compensate for process and temperature variations. The objective is to realize a receiver front-end circuit with adjustable lowpass filters that is small in size while enabling the software-defined radio (SDR) of the future.

The organization of this paper is as follows. Section 2 presents discrete-time signal processing of the RF front-end mixer with an emphasis on Bluetooth examples. Section 3 describes a specific implementation of the described techniques and concepts in a GSM front-end radio. Silicon realization of the Bluetooth and GSM radios is presented in Section 4. Performance of the GSM front-end receiver is shown in Section 6.

2. DISCRETE-TIME OPERATION

2.1. Direct sampling mixer

The basic idea of the current-mode direct sampling mixer [3, 4] is illustrated in Figure 1(a). The *low-noise transconductance amplifier* (LNTA) converts the received RF voltage v_{RF} into i_{RF} in current domain through the transconductance gain g_m . The current i_{RF} gets switched by the half-cycle of the *local oscillator* (LO) and integrated into the sampling capacitor C_s . Since it is difficult to switch the current at RF rate, it could be merely redirected to an identical sampler that is operating on the opposite half-cycle of the LO clock, as shown in Figure 1(b) for a pseudodifferential configuration.

If the LO oscillating at f_0 frequency is synchronous and in phase with the sinusoidal RF waveform, the voltage gain of a single RF half-cycle is

$$G_{v,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \cdot \frac{g_m}{C_s} \quad (1)$$

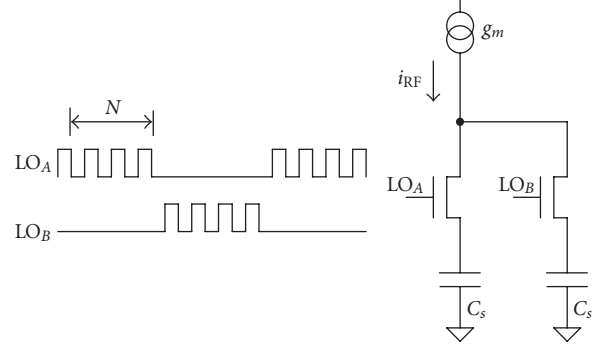


FIGURE 2: Temporal MA operation at RF rate with cyclic charge readout.

and the accumulated charge on the sampling capacitor is

$$G_{q,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \cdot g_m. \quad (2)$$

In the above equations, the $1/\pi$ factor is contributed by the half-cycle sinusoidal integration. As an example, if $g_m = 30$ mS, $C_s = 15.925$ pF, and $f_0 = 2.4$ GHz, then $G_{v,RF} = 0.25$.

2.2. Temporal moving average

Continuously accumulating the charge as shown in Figure 1 is not very practical if it cannot be read out. In addition, a mechanism to prevent the charge overflow is needed. Both of these operations are accomplished by fixing the integration window length followed by charge readout phase that will also discharge the sampling capacitor such that the next period of integration would start from the same zero condition. The RF sampling and readout operations are cyclically rotated on both C_s capacitors as shown in Figure 2. When LO_A rectifies N RF cycles that are being integrated on the first sampling capacitor, LO_B is off and the second sampling capacitor charge is being read out. On the following N RF cycles the operation is reversed. This way, the charge integration and readout occur at the same time and no RF cycles are missed.

The sampling capacitor integrates the half-rectified RF current over N cycles. The charge accumulated on the sampling capacitor and the resulting voltage ($V = Q/C_s$) increases with the integration window, thus giving rise to a discrete signal processing gain of N .

The temporal integration of N half-rectified RF samples performs a *finite-impulse response* (FIR) operation with N all-one coefficients, also known as *moving-average* (MA), according to the equation

$$w_i = \sum_{l=0}^{N-1} u_{i-l}, \quad (3)$$

where u_i is the i th RF sample of the input charge sample, w_i is the accumulated charge. Since the charge accumulation is done on the same capacitor, this formula could also be used

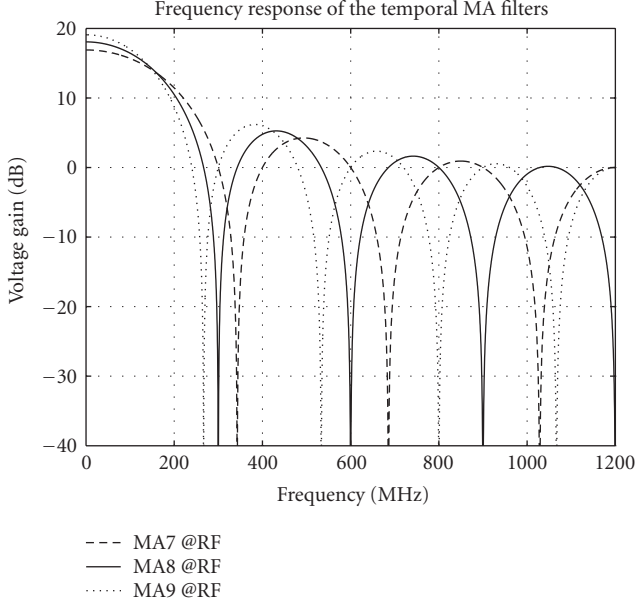


FIGURE 3: Transfer function of the temporal MA operation at RF rate.

in the voltage domain. Its frequency response is a *sinc* function and is shown in Figure 3 for $N = 8$ (solid line) and $N = 7, 9$ (dotted lines) with sampling rate $f_0 = 2.4$ GHz. It should be noted that this filtering is done on the same capacitor in time domain resulting in a most *faithful* reproduction of the transfer function.

Due to the fact that the MA output is being read out at the lower rate of N RF clock cycles, there is an additional aliasing with foldover frequency at $f_0/2N$ and located halfway to the first notch. Consequently, the frequency response of MA = 7 with decimation of 7 exhibits less aliasing and features wider notches than MA = 8 or MA = 9 with decimation of 8 or 9, respectively.

It should be emphasized that the voltage G_v and charge G_q signal processing gains of the temporal moving average (TMA) (followed by decimation) are merely due to the sampling time interval expansion of this discrete-time system (the sampling rate of the input is at the RF frequency): $G_{v,\text{tma}} = G_{q,\text{tma}} = N$.

In the following analysis, the RF half-cycle integration voltage gain of $g_m/\pi C_s f_0$ is tracked separately. Since this gain depends on the absolute physical parameters of usually low tolerance (g_m value of the preceding LNTA stage and the total integrating capacitance of the sampling mixer), it is advantageous to keep it decoupled from the discrete signal processing gain of the MTDSM.

2.3. High-rate IIR filtering

Figure 2 is now modified to include recursive operation that gives rise to the IIR filtering capability, which is generally considered stronger than that of FIR.

A “history” sampling capacitor C_H is added in Figure 4. The integration operation is continually performed on the “history” capacitor $C_H = a_1 C_s$ and one of the two rotating “charge-and-readout” capacitors $C_R = (1 - a_1)C_s$ such that the total RF integrating capacitance, as seen by the LNTA, is always $C_H + C_R = C_s$. When one of the C_R capacitors is being used for readout, the other is being used for RF integration.

The IIR filtering capability comes into play in the following way. The RF current is being integrated over N RF cycles, as described before. This time, the charge is being shared on both C_H and C_R capacitors proportionately to their capacitance values. At the end of the accumulation cycle, the active C_R capacitor, that stores $(1 - a_1)$ of the total charge, stops further accumulating in preparation for charge readout. The other rotating capacitor joins the C_H capacitor in the RF sampling process and, at the same time, obtains $(1 - a_1)/(a_1 + (1 - a_1)) = 1 - a_1$ of the total remaining charge in the “history” capacitor, provided it has no initial charge at the time of commutation. Thus the system retains a_1 portion of the total system charge of the previous cycle.

If the input charge accumulated over the most recent N RF samples is w_j , then the charge s_j stored in the system at sampling time j , where $i = N \cdot j$ (as stated earlier, i is the RF cycle index) could be described as a single-pole recursive IIR equation:

$$s_j = a_1 s_{j-1} + w_j, \quad (4)$$

$$x_j = (1 - a_1) s_{j-1}, \quad (5)$$

$$a_1 = \frac{C_H}{C_H + C_R}. \quad (6)$$

The output charge x_j is $(1 - a_1)$ of the system charge in the most recent cycle. This discrete-time IIR filter operates at f_0/N sampling rate and introduces a single pole with the frequency attenuation of 20 dB/dec. The equivalent pole location in the continuous-time domain for $f_{c1} \ll f_0/N$ is

$$f_{c1} = \frac{1}{2\pi N} \cdot \frac{f_0}{N} \cdot (1 - a_1) = \frac{1}{2\pi N} \cdot \frac{f_0}{N} \cdot \frac{C_R}{C_H + C_R}. \quad (7)$$

Since there is no sampling time expansion for the IIR operation, the discrete signal processing charge gain is one. In other words, due to the charge conservation principle, the input charge per sample interval is on average the same as the output charge. For the voltage gain, however, there is an impedance transformation of $C_{\text{input}} = C_s$ and $C_{\text{output}} = (1 - a_1)C_s$, thus resulting in a gain:

$$G_{q,\text{iir1}} = 1, \quad G_{v,\text{iir1}} = \frac{1}{1 - a_1} = \frac{C_H + C_R}{C_R}. \quad (8)$$

As an example, the IIR filtering with a single coefficient of $a_1 = 0.9686$, placing the pole at $f_{c1} = 1.5$ MHz ($C_R = 0.5$ pF, $C_H = 15.425$ pF) is performed at $f_0/N = 2.4$ GHz/8 = 300 MHz sampling rate and it follows the FIR MA = 8 filtering of the input at f_0 RF sampling rate. The voltage gain of the high-rate IIR filter is 31.85 (30.06 dB).

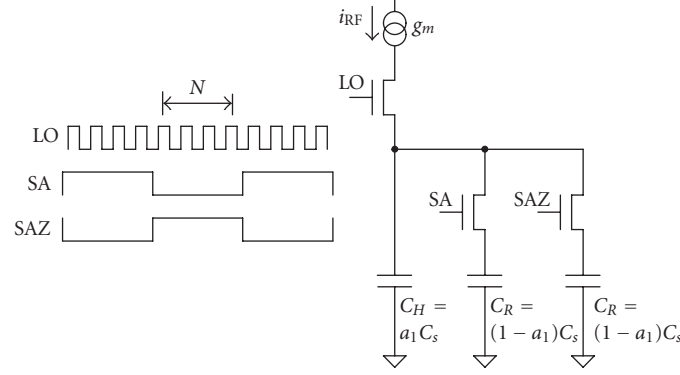


FIGURE 4: IIR operation with cyclic charge readout.

2.4. Additional spatial MA filtering zeros

For practical reasons, it is difficult to read out the x_j output charge of Figure 4 at $f_0/N = 300$ MHz rate. The output charge readout time is extended $M = 4$ times by adding redundancy of four to each of the two original C_R capacitors as shown in Figure 5. The input charge is cyclically integrated within the group of four C_R capacitors. Adding the redundant capacitors gives rise to an additional antialiasing filtering just before the second decimation of M . This could also be considered as equivalent to adding additional $M - 1$ zeros to the IIR transfer function in (4). After the first bank of four capacitors gets charged ($S_{A1} - S_{A4}$ in Figure 5), the second bank ($S_{B1} - S_{B4}$) is in the process of being charged and the charge on first bank of capacitors are summed and read out (R_A). Physically connecting together the four capacitors performs an FIR filtering described as the spatial moving average of $M = 4$:

$$y_k = \sum_{l=0}^{M-1} x_{k-l}, \quad (9)$$

where y_k is the output charge and sampling time index $j = M \cdot k$. R_A and R_B in Figure 5 are the readout/reset cycles during which the output charge on the four nonsampling capacitors is transferred out and the remnant charge is reset before the capacitors are put back into the sampling operation. It should be noted that after the reset phase, but before the sampling phase, the capacitors are unobtrusively precharged [5] in order to implement a dc-offset cancellation or to accomplish a feedback summation for the $\Sigma\Delta$ loop operation.

Since the charge of four capacitors is added, there is a charge gain of $M = 4$ and a voltage gain of 1. Again, as explained before, the charge gain is due to the sampling interval expansion: $G_{q,sma} = M$ and $G_{v,sma} = 1$.

Figure 6 shows frequency response of the temporal moving average with a decimation of 8 ($G_v = 18.06$ dB), the IIR filter operating at RF/8 rate ($G_v = 30.06$ dB), and the spatial moving average filter operating at RF/32 rate ($G_v = 0$ dB) with a decimation of 4. The solid line is the composite transfer function with the dc gain of $G_v = 48.12$ dB. The first decimation of $N = 8$ reveals itself as aliasing. It should be noted

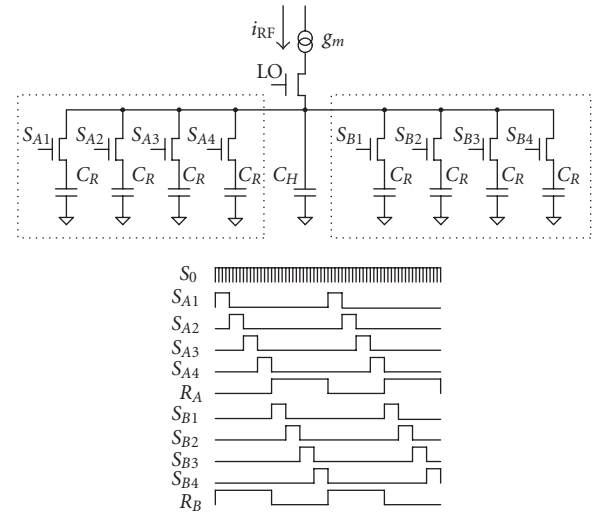


FIGURE 5: IIR operation with additional FIR filtering. The readout and reset circuitry is not shown.

that it is possible to avoid aliasing of a very strong interferer into the critical IF band by simply changing the decimation ratio N . This brings out advantages of integrating RF/analog with digital circuitry by opening new avenues of novel signal processing solutions not possible before.

2.5. Lower-rate IIR filtering

The voltage stored on the rotating capacitors cannot be readily presented to the MTDSM block output without an active buffer that would isolate the high impedance of the mixer from the required low driving impedance of the output. Figure 7 shows the mechanism to realize the second, lower-rate, IIR filtering through passive charge sharing. The active element, the operational amplifier, does not actually take part in the IIR filtering process. It is merely used to sense voltage of the buffer feedback capacitor C_B and present it to the output with a low driving impedance. Figure 7 additionally suggests possibility of differentially combining, through the

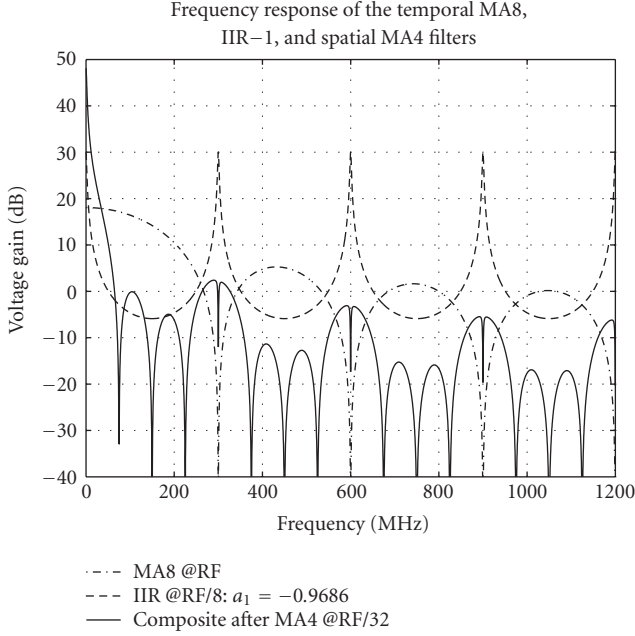


FIGURE 6: Transfer functions of the temporal MA filter and the IIR filter operating at RF/8 rate. The solid line is the composite transfer at the output of the spatial MA filter.

operational amplifier, the opposite (180 degree apart) processing path.

The charge y_k accumulated on the $M = 4$ rotating capacitors is being shared during the dumping phase with the buffer capacitor C_B . At the end of the dumping phase, the $M \cdot C_R$ capacitors get disconnected from the second IIR filter and their charge reset before they could be reengaged in the MTDSM operation of Figure 5. This charge loss mechanism gives rise to IIR filtering. If the input charge is y_k , then the charge z_k stored in the buffer capacitor C_B at sampling time k is

$$z_k = a_2(z_{k-1} + y_k) = a_2 z_{k-1} + a_2 y_k, \quad (10)$$

$$a_2 = \frac{C_B}{C_B + MC_R}. \quad (11)$$

Equation (10) describes a single-pole IIR filter with coefficient a_2 and input y_k scaled by a_2 , where a_2 corresponds to the storage-to-total capacitance ratio $C_B/(C_B + MC_R)$. Conversely, due to the linearity property, it could also be thought of as an IIR filter with input y_k and output scaled by a_2 .

This discrete-time IIR filter operates at f_0/NM sampling rate and introduces a single pole with the frequency transfer function attenuation of 20 dB/dec. The equivalent pole location in the continuous-time domain for $f_{c2} \ll f_0/(NM)$ is

$$f_{c2} = \frac{1}{2\pi} \frac{f_0}{NM} \cdot (1 - a_2) = \frac{1}{2\pi} \frac{f_0}{NM} \cdot \frac{MC_R}{C_B + MC_R}. \quad (12)$$

The actual MTDSM output is the voltage sensed on the buffer feedback capacitor z_k/C_B . The previously used charge stream model cannot be directly applied here because the “output” charge z_k is not the one that leaves the system.

The charge “lost” or reflected back into the $M \cdot C_R$ capacitor for subsequent reset is $(1 - a_2)(z_{k-1} + y_k)$. Due to charge conservation principle, the time-averaged values of charge input, y_k , and charge leaked out, $(1 - a_2)(z_{k-1} + y_k)$, should be equal. As stated before, the leak-out charge is not the output from the signal processing standpoint. It should be noted that the amplifier does not contribute to the net charge change of the system and, consequently, the only path of the charge loss is through the same $M \cdot C_R$ capacitors being reset after the dumping phase.

The output charge z_k stops at the IIR-2 stage and does not further propagate, therefore it is of less importance for signal processing analysis. The charge discrete signal processing gain of the second IIR stage is

$$G_{q,iir2} = \frac{a_2}{1 - a_2} = \frac{C_B}{MC_R}. \quad (13)$$

The input/output impedance transformation is MC_R/C_B . Consequently, the voltage gain of IIR-2 is unity:

$$G_{v,iir2} = 1. \quad (14)$$

2.6. Cascaded MTDSM filtering

The cascaded discrete signal processing gain equations of the MTDSM mixer are

$$\begin{aligned} G_{q,dsp} &= G_{q,tma} \cdot G_{q,iir1} \cdot G_{q,sma} \cdot G_{q,iir2} \\ &= N \cdot 1 \cdot M \cdot \frac{C_B}{MC_R} \\ &= \frac{NC_B}{C_R}, \\ G_{v,dsp} &= G_{v,tma} \cdot G_{v,iir1} \cdot G_{v,sma} \cdot G_{v,iir2} \\ &= N \cdot \frac{C_H + C_R}{C_R} \cdot 1 \cdot 1 \\ &= \frac{N(C_H + C_R)}{C_R}. \end{aligned} \quad (15)$$

Including the RF half-cycle integration (1) and (2), the total single-ended gain is

$$\begin{aligned} G_{q,tot} &= G_{q,RF} \cdot G_{q,dsp} \\ &= \frac{1}{\pi} \cdot \frac{1}{f_0/N} \cdot g_m, \end{aligned} \quad (16)$$

$$\begin{aligned} G_{v,tot} &= G_{v,RF} \cdot G_{v,dsp} \\ &= \frac{1}{\pi} \cdot \frac{1}{f_0/N} \cdot \frac{g_m}{C_R}. \end{aligned} \quad (17)$$

Note the similarity between (17) and (1). In both cases, the term $R_{sc} = 1/f_s C_s$ is an equivalent resistance of a switched capacitor C_s sampling at rate f_s . For example, if $f_s = 300$ MHz and $C_R = 0.5$ pF, then the equivalent resistance is $R_{sc} = 6.7$ k Ω . Since the MTDSM output is differential, the gain values in the above equations are actually doubled.

The dc-frequency gain $G_{v,tot}$ in (17) requires further elaboration. The gain depends only on the g_m of the LNTA stage, rotating capacitor value, and the rotation frequency. Amazingly, it does not depend on the other capacitor values, which contribute only to the filtering transfer function at higher frequencies.

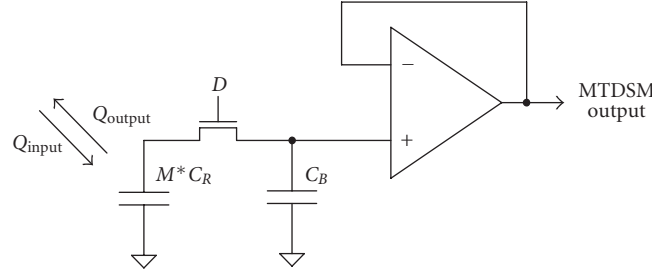


FIGURE 7: Second IIR filter.

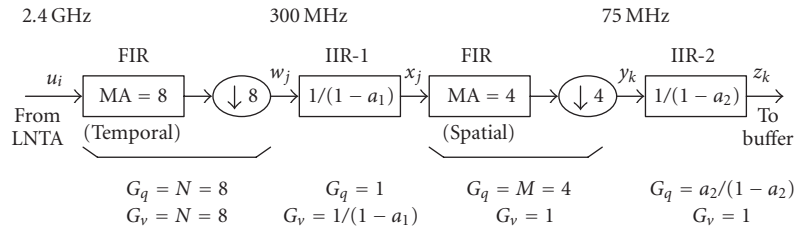


FIGURE 8: Discrete signal processing in the MTDSM.

2.7. Near-frequency interferer attenuation

Most of the lower-frequency filtering could be realistically done only with the first and second IIR filters. The two FIR filters do not have appreciable filtering capability at low frequencies and are mainly used for antialiasing.

It should be noted that the best filtering could be accomplished by making 3-dB corner frequencies of both IIR filters the same and placing them as close to the higher end of signal band as possible:

$$f_{c1} = f_{c2}. \quad (18)$$

This gives the following constraint:

$$C_B = C_H - (M - 1)C_R. \quad (19)$$

2.8. Signal processing example

Figure 8 shows the block diagram from the signal processing standpoint for our specific implementation of $f_0 = 2.4$ GHz, $N = 8$, $M = 4$. The following equations describe the time-domain signal processing: (3) for w_i , (4) and (5) for x_j , (9) for y_k , and (10) for z_k .

The first aliasing frequency (at $f_0/N = 300$ MHz) is partially protected by the first notch of the temporal MA = 8 filter. However, for higher-order aliasing and overall system robustness, it has to be protected with a truly continuous-time filter, such as an antenna filter. A typical low-cost Bluetooth-band duplexer can attenuate up to 40 dB at 300 MHz offset.

For the above system with an aggressive cut-off frequency of $f_{c1} = f_{c2} = 1.5$ MHz, using $C_R = 0.5$ pF will result in a dc-frequency voltage gain of 63.66 or 36 dB (17) and the required capacitance is $C_H = 15.425$ pF (7) and $C_B = 13.925$ pF (12). The z -domain coefficients of the IIR filters

are $a_1 = 0.9686$ and $a_2 = 0.8744$. The dc-frequency gains are $G_{v,iir1} = 31.85$ and $G_{v,iir2} = 1$. The transfer function of these IIR filters is shown in Figure 9. The spatial MA = 4, which follows IIR-1, does not appreciably contribute to filtering at lower frequencies but serves as an antialiasing filter for the lower-rate IIR-2. Since the 3-dB point of IIR-2 is slightly corrupted by the discrete-time approximation, the composite attenuation at the cut-off frequencies $f_{c1} = f_{c2} = 1.5$ MHz is about 5.5 dB. The attenuation drops to 13 dB at 3 MHz.

Within the 1 MHz band of interest, there is a 3-dB signal attenuation. For the most optimal detector operation, this in-band filtering should be taken into consideration in the matched-filter design. Figure 10 shows the phase response of the above structure versus the ideal constant group delay.

2.9. MTDSM feedback path

The MTDSM feedback correction could be unobtrusively injected into either group of the four rotating capacitors of Figure 5 when they are not in the active sampling state. This way, the main signal path is not perturbed. The feedback correction is accomplished through charge injection/equalization between the “feedback capacitor” C_F and the rotating capacitors C_R in the MTDSM structure by shorting all of them together after the C_R group of capacitors gets reset, but before they are put back to the sampling system. The feedback charge accumulation structure is shown in Figure 11. Each feedback capacitor C_F is associated with one of the two rotating capacitors of group “A” and “B.” The two groups commutate the charging process.

Voltage on the feedback capacitor can be calculated as follows. Charging the feedback capacitor C_F with the current i_{fbck} for the duration of T will result in incremental accumulation of $\Delta Q_{in} = i_{fbck} \cdot T$ charge. This charge gets

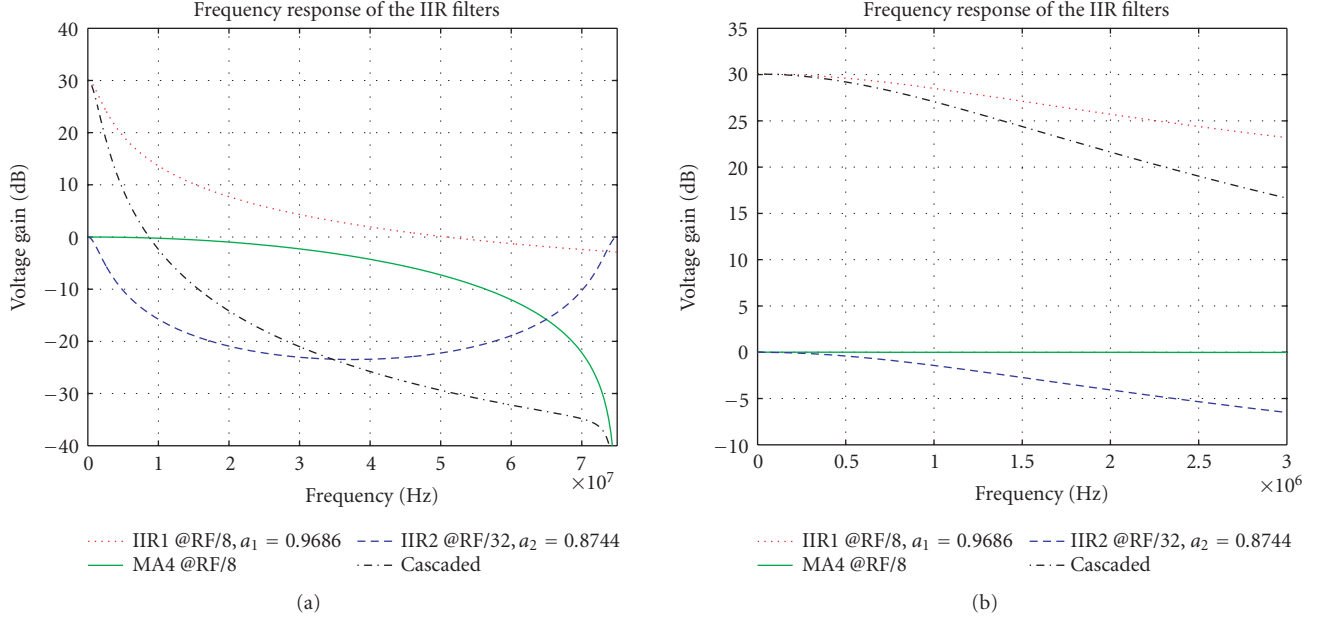


FIGURE 9: Transfer functions of the IIR filters with two poles at 1.5 MHz (bottom zoomed).

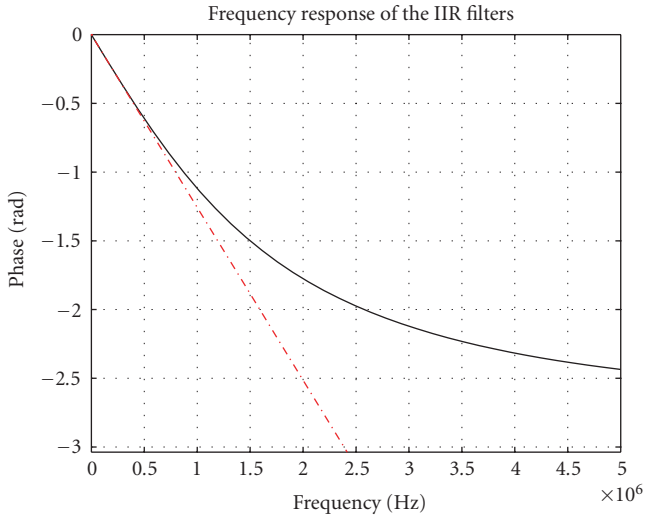


FIGURE 10: Phase response of the IIR filters with two poles at 1.5 MHz.

added to the total charge $Q_F(k)$ of the feedback capacitor at the k th time instance:

$$Q_F(k) = Q_F(k-1) + \Delta Q_{in} = Q_F(k-1) + i_{fbck} \cdot T. \quad (20)$$

During the charge distribution moment, the feedback capacitor gets connected with the previously reset group of rotating capacitors $M \cdot C_R$. The charge depleted from C_F is dependent on the relative capacitor values:

$$\Delta Q_{out}(k) = \frac{MC_R}{C_F + MC_R} Q_F(k). \quad (21)$$

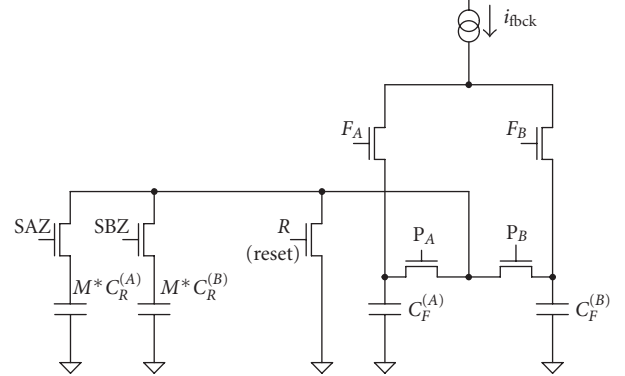


FIGURE 11: Feedback into the rotating capacitors.

The charge transferred to the rotating capacitors is proportional to the total accumulated charge Q_F or voltage on the feedback capacitor $V_F = Q_F/C_F$. At first, the accumulated charge is small, so the outgoing charge is small. Since the incoming charge is constant, the Q_F charge will continue accumulating until the net charge intake becomes zero. Equilibrium is reached when $\Delta Q_{in}(k) = \Delta Q_{out}(k)$:

$$i_{fbck} \cdot T = \frac{MC_R}{C_F + MC_R} Q_F(k). \quad (22)$$

Transformation of the above gives the equilibrium voltage:

$$V_{F,eq} = i_{fbck} \cdot T \cdot \frac{C_F + MC_R}{C_F \cdot MC_R}. \quad (23)$$

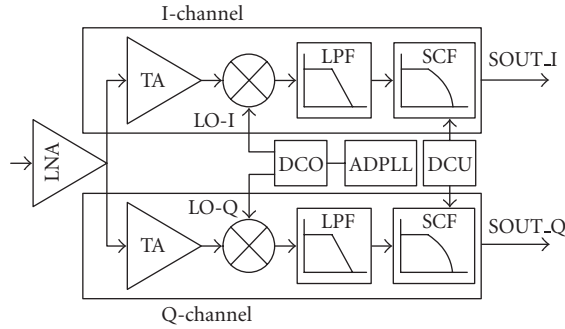


FIGURE 12: Receiver front-end diagram.

The $\Delta Q_{\text{out,eq}}$ charge transfer into the rotating capacitors at equilibrium will create voltage on the bank of rotating capacitors:

$$V_R = \frac{i_{\text{fbck}} \cdot T}{MC_R}. \quad (24)$$

As shown in Section 2.5, the voltage transfer function from the rotating capacitors to the history capacitor is unity. Therefore, the bias voltage developed on C_H is

$$V_H = \frac{i_{\text{fbck}} \cdot T}{MC_R}. \quad (25)$$

3. A GSM RECEIVER FRONT-END ARCHITECTURE

The receiver front end is shown in Figure 12 and consists of an LNA followed by two transconductance amplifiers (TAs) and two passive mixers. The RF input signal is amplified by the LNA and splits into I/Q paths where it is further amplified in the TA. It is then down-converted to a low intermediate frequency (IF) that is fully programmable (but defaults to 100 kHz) by the following mixers driven by an integrated local oscillator (LO). The IF signal is sampled and lowpass-filtered by passing through the switched-capacitor filter (SCF). The LO signals are generated using an all-digital PLL (ADPLL) [12] that incorporates a digitally controlled oscillator (DCO). The digital control unit (DCU) provides all the clocks for the SCF operation.

Although the front-end circuit requires two TAs, two mixers, and quadrature LO signals, the receiver has an excellent sensitivity and good linearity at a low supply voltage (V_{DD}) of 1.4 V thus offering excellent performance that satisfies the GSM requirements. The power is supplied by an integrated low-drop-out (LDO) regulator.

3.1. Low-noise amplifier

A differential LNA is implemented to improve noise figure which could be degraded by substrate coupling originating from DBB since the impact of the switching noise of more than a million digital gates on the same silicon die could not have been known precisely. Figure 13 shows a simplified schematic diagram of the LNA. A variable gain feature with seven digitally configurable steps is implemented. In the

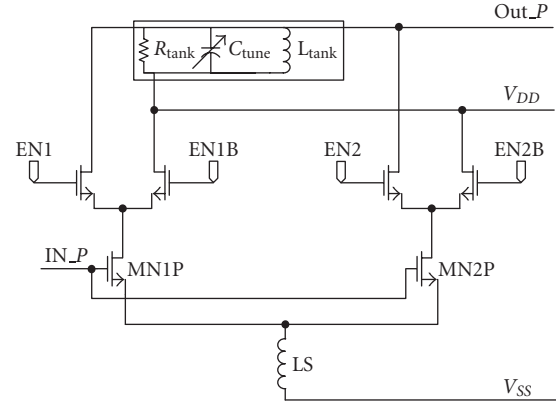


FIGURE 13: LNA core schematic.

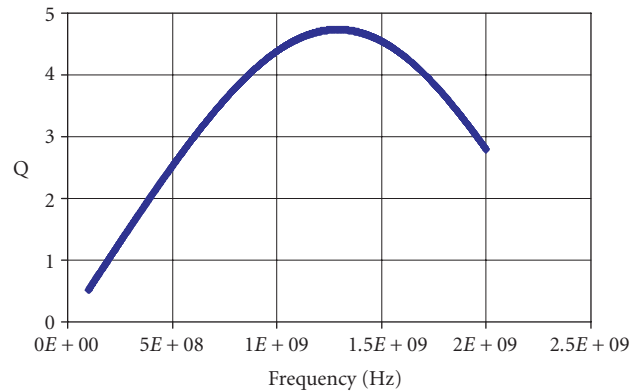


FIGURE 14: Inductor Q-factor.

high-gain mode, four voltage gains are realized with a 2-dB step between 21 dB and 29 dB. In the low-gain mode, there are three gain steps with a 2-dB step between 3 dB and 9 dB. As shown in Figure 13, the multiple cascode stages are connected in parallel with one source degeneration inductor and one inductive load. Each stage has digital configurability.

The top transistors of the cascode stage used for bypassing gain contribution are shunted to V_{DD} . Since the bottom transistors of the cascode stage operate in all gain settings, the input impedance is constant to the first order over gain selections, which is critical for constant input power and noise matching. Inductive source degeneration using package bond wires is implemented to improve linearity. The LNA load is an on-chip spiral inductor using multiple metal layers with metal width = $5.9 \mu\text{m}$, metal space = $2 \mu\text{m}$, inner diameter = $81.9 \mu\text{m}$, and 10 turns. This inductor is drawn as a center-tap configuration for better matching between the differential branches and achieving a higher quality factor (Q). As shown in Figure 14, the inductance is 8.9 nH and Q is > 4 at 900 MHz, where Q is defined as $|\text{imag}(y_{11})/\text{real}(y_{11})|$. To reduce the substrate effect, all doping under the inductor is blocked to preserve a higher resistivity.

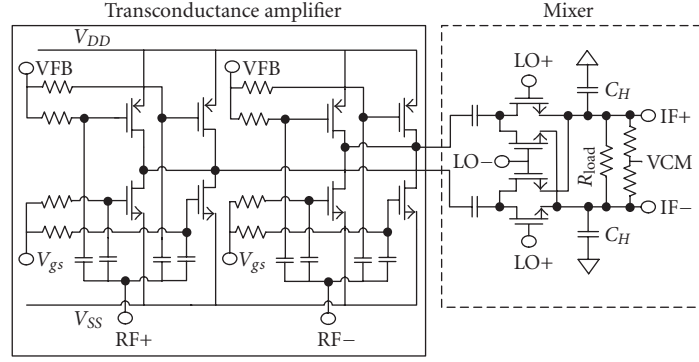


FIGURE 15: TA and mixer core schematic.

The inductor is tuned with the capacitance at the LNA load which comprises tuning capacitors together with parasitics. The tuning capacitor is realized using metal-insulator-metal (MIM) capacitors and switches. Two capacitors are connected differentially with a switch and two pull-down transistors to keep both source/drain voltages of the switch low and Q of the capacitor bank high. The achieved effective Q is 100 at 900 MHz. When the switch is turned off to be in a low capacitance value, the parasitic capacitance of the MIM capacitors and transistors still has an effective Q of about 100. Compared to MOS capacitor, MIM capacitor provides a much better trade-off between Q and C_{ON}/C_{OFF} ratio. In this design, a C_{ON}/C_{OFF} ratio of larger than 4 was achieved while Q is still greater than 100. The selectable capacitance ranges 2.5 pF in total because in this process, MIM capacitance can vary up to $\pm 20\%$ from its nominal value. With this design, all GSM bands can be fully covered.

The differential LNA draws 7.3 mA. The LNA input is protected against ESD by one reverse-biased diode to V_{DD} and three forward-biased diodes in series to V_{SS} . ESD structures at LNA input are aimed to protect larger than 2 kV human body model (HBM). The LNA bond pad is shielded with lower metal-1 layer to eliminate the substrate coupling while minimizing parasitic capacitance which is about 100 fF.

3.2. TA and mixer

Figure 15 shows a simplified TA and mixer schematic diagram. A highly efficient push-pull amplifier is chosen for the TA because of its low noise and good linearity characteristics. The variable gain feature is implemented in the TA with a 3-bit control. A feedback amplifier is used to set the dc bias voltage of the TA output node to V_{REF} which is set to half of V_{DD} so as to provide maximum signal swing. Resistors in Figure 15 are large enough to prevent significant RF signal loading. The differential TA draws 4 mA in the maximum gain mode.

A double-balanced switching mixer is connected to the TA output via ac-coupling capacitors so that the dc voltage at the TA output is isolated from the mixer. This topology has an excellent feature of reduced $1/f$ noise because there is

no dc current flowing through making it suitable for direct-conversion or near-zero IF receivers. By adding a capacitive load (C_H , history capacitor) to the mixer output, lowpass filtering can be obtained to reduce large interferers. In this mixer, two switches are toggled by one of the complementary LO signals (LO+, LO-) from a digitally controlled oscillator (DCO). Since the mixer is connected to the switched capacitor filter (SCF), its loading effect can be represented as R_{load} which is about 4.5 k Ω .

3.3. SCF

The schematic diagram of the switched capacitor filter block (SCF) is shown in Figure 16. The switches are controlled by the digital control unit (DCU) that generates the timing waveforms shown in Figure 17. For one LO cycle, the RF signal of the mixer output is integrated into a history capacitor (C_H) and a rotating capacitor (C_{R1}). Since the four rotating capacitors sequentially connect to C_H in a fixed order, the charge transfer via C_{R1} is a direct sampling of IF signal. It is also clear that a charge loss on C_H through C_{R1} creates the loading (R_{load}) to the mixer output. For two LO cycles, two rotating capacitors in the first bank sample the IF signal on C_H while the rotating capacitors in the second bank and C_{B1} share charge. Because of the half sampling rate from the mixer output to C_{B1} , the decimation operation creates a *sinc* function that has notches at the foldover frequencies, $NLO/2$, where N is a positive integer. Transconductance (g_m) of TA, C_H and the loading (R_{load}) of SCF create the first IIR filtering response of g_m -C antialiasing lowpass filtering prior to the main *sinc* filter. However, the TA sees a periodic constant load at its output.

After the two C_{R1} capacitors in one bank are disconnected from C_H , these carry the charge of past 2 IF samples created by the charge sharing between two C_{R1} and C_H . Next, the two C_{R1} capacitors share charge with the buffer capacitor C_{B1} and a second rotating capacitor, C_{R2} . The overall effect is to create a second IIR filtering stage in which $2C_{R1}$ delivers input, C_{B1} holds the memory, and C_{R2} captures a glimpse of the output of the second IIR filter stage. This charge is subsequently shared with a second buffer capacitor, C_{B2} , resulting

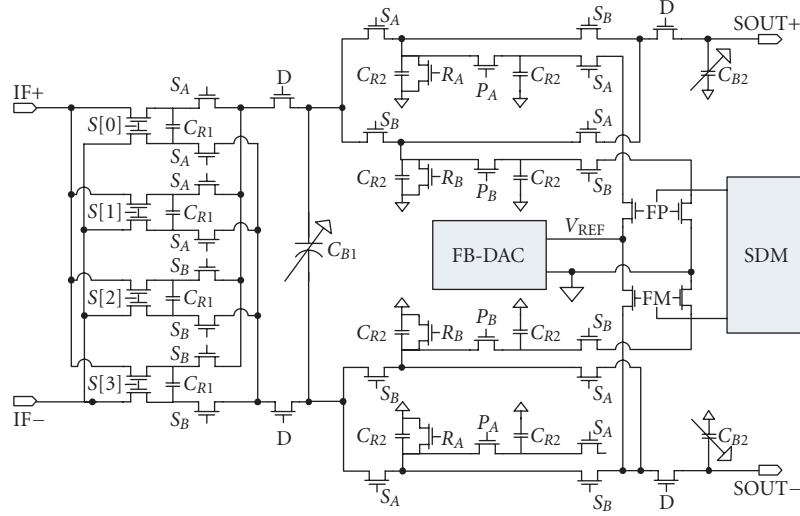


FIGURE 16: SCF core schematic.

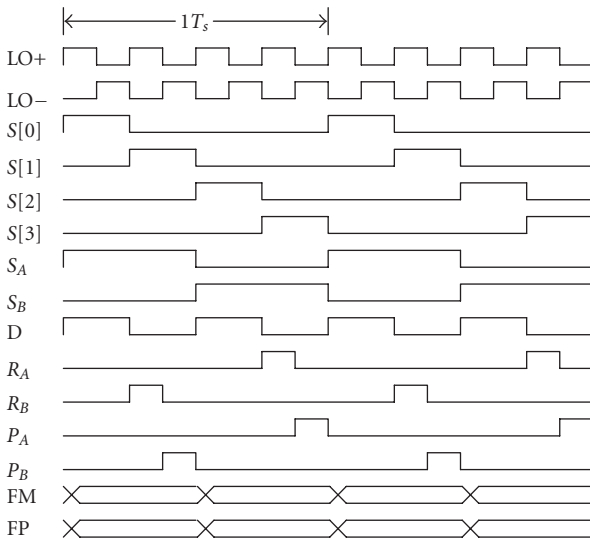


FIGURE 17: DCU clock diagram.

in the third IIR filter stage. While charge samples are passed on from the C_H to C_{B2} through a series of charge combination, splitting and recombination operations, the IF information at mixer output are always kept on C_H together with two C_{R1} capacitors from one bank. The three IIR filters have corner frequencies that are given by respective ratios of rotating capacitors (C_{R1} , C_{R2}) to fixed capacitors (C_H , C_{B1} , C_{B2}) and may be readjusted by changing the size of the capacitors. The capacitor ratios in the SCF are programmable which allows the filter corner frequency to be adjustable over a wide range, thereby allowing its use in a multistandard environment.

After the charge sharing of C_{R2} with C_{B2} , C_{R2} is reset (RA, RB) and precharged (PA, PB) by the 1-bit feedback circuit

(FB-DAC) provided by a sigma-delta modulator that connects the output of a low-noise feedback voltage reference to C_{R2} . Zero DAC code produces approximately 50% duty cycle at FM and FP clocks which brings the common mode voltage of the SCF exactly at half of V_{REF} . In the presence of a dc offset, the duty cycle is changed with sigma-delta noise shaping to cancel the offset voltage.

3.4. DCO

A DCO circuit schematic is shown in Figure 18 [12]. L1A and L1B are two halves of a center-tap inductor. Because of the shortcoming of this 90-nm digital CMOS Cu process which has thin metal interconnects, it is difficult to design an inductor with even a moderate Q. To enhance the Q of the inductor, an Al layer is patterned and connected in parallel with the Cu windings. M3-5 plus the Al layer were used to form L1 while only M3-5 layers were used for L0. The total Cu and Al thickness are only $0.75 \mu\text{m}$ and $1.0 \mu\text{m}$, respectively. The simulated single-ended Q using an $\text{imag}(y_{11})/\text{real}(y_{11})$ definition is 3.6 and 6.7 at 0.9 and 3.6 GHz, respectively. The differential phase stability Q is 3.6 and 10.2 at 0.9 and 3.6 GHz, respectively [13].

The varactor is implemented using an npoly-nwell MOSCAP structure. Extrapolating from measurement data, the $C_{\text{max}}/C_{\text{min}}$ ratio is > 3 within the ranges of desired gate length L_g and gate width W_g per finger. The resulting total tolerable fixed parasitic capacitance is 720 fF. MOSCAP was chosen because the gate oxide thickness (t_{ox}) is one of the best controlled parameters in this CMOS process, whose corner variation is within $\pm 2.5\%$. The four different phases of LO driving the I- and Q-mixers in Figure 15 are generated from the DCO frequency which oscillates at $4\omega_0$, where ω_0 is in the GSM band frequencies. A fully digital circuit (ADPLL) is built around the DCO to adjust its phase and frequency deviations in a negative feedback manner.

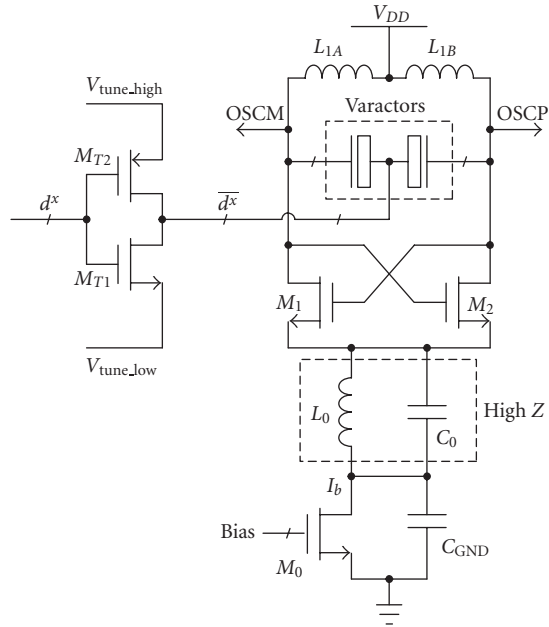


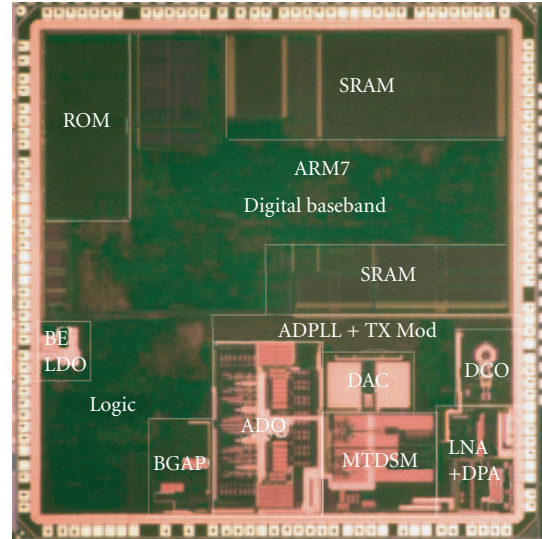
FIGURE 18: DCO core schematic.

4. SILICON REALIZATION

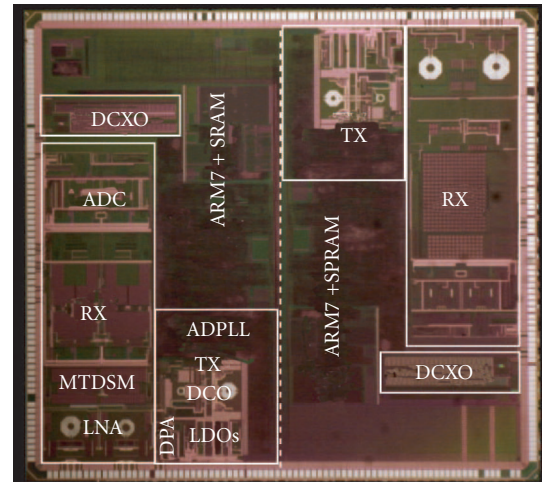
The presented techniques have been realized in silicon. Figure 19 shows two chip micrographs representing the first and second generation of digital RF processor (DRP), respectively: (1) commercial 10 mm² single-chip Bluetooth radio in 130 nm CMOS, and (2) a fully functional preproduction version of the single-chip GSM radio in 90-nm CMOS. The GSM chip consists of two independent pairs of transmitters and receivers to study various on-die coupling mechanisms, which are especially important in full-duplex WCDMA operations with RX and TX diversity. The 90-nm process features the following parameters that characterize the process: 0.27 μm minimum metal pitch, five levels of copper metal, 1.2 V nominal transistor voltage, 2.6 nm gate oxide thickness, logic gate density of 250 kgates/mm², SRAM cell density of 1.0 Mb/mm². The measured RX sensitivity of -82 dBm for Bluetooth and -110 dBm for GSM, versus the respective specifications of -70 dBm and -102 dBm, is quite competitive with conventional solutions. The overall GSM RX noise figure is only 2 dB.

5. GSM RX FRONT-END PERFORMANCE

The LNA input is matched using an external inductor and a capacitor with a balun for impedance ratio of 50 to 100 Ω . The measured LNA input matching with S_{11} is < -10 dB over the whole GSM band. When the curves of S_{11} versus multiple LNA gains are compared, largest variation is less than 1 dB. Figure 20 displays the front-end voltage gains versus different LNA and TA gain settings. The front-end gains can be configured with an automatic-gain-control (AGC) function to select an optimal gain setting trading off noise figure for linearity. This circuit adds 32.5 dB dynamic range to the receiver.



(a)



(b)

FIGURE 19: Die micrographs of radios employing two generations of DRP: (a) the commercial single-chip Bluetooth radio; (b) the preproduction version of the single-chip GSM radio.

The measured noise figure in the maximum gain mode is 1.8 dB which is excellent, when considering the fact that several hundred thousand digital logic gates are switching on the same die. With LO frequency set to 869.1 MHz, +50 dBm of IIP2 is measured with a front-end gain of 34 dB where the LNA gain is set to 2 dB below the maximum gain (6_LNA) and TA to its middle gain setting (3_TA). To mimic the EDGE environment, two tones of 875.2 MHz and 875.3 MHz are injected into the LNA for the IIP2 test (power of -36 dBm). The LNA, two TAs, and mixers consume 15.3 mA from an internal LDO voltage of 1.4 V. Since this work has digitally configurable gain with a fine resolution, it is different from a conventional front-end approach that is typically built for two large steps. A major advantage of our approach is that

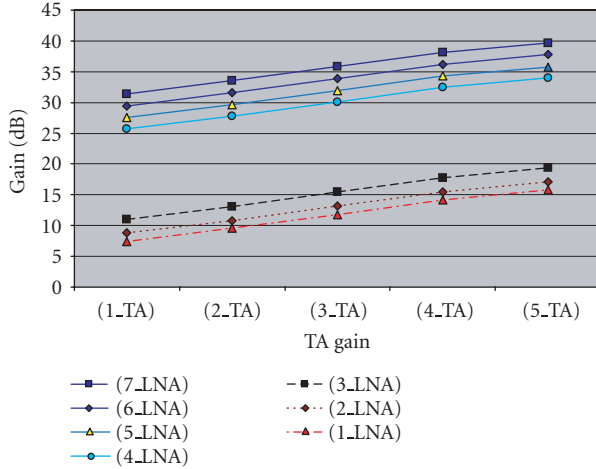


FIGURE 20: Measured voltage gain.

TABLE 1: Measured performance.

	Measured data
Noise figure (1 kHz—100 kHz)	2.0 dB
NF with -25 dBm blocker at 3-MHz offset	5.0 dB
S_{11}	< -10 dB
IIP ₂	+50 dBm
IIP ₃	-15 dBm
P_1 dB	-25 dBm
Gain	+34 dB
Front-end current consumption	15.3 mA

the circuit performance can be finely optimized by selecting the appropriate gain settings.

Table 1 summarizes the measured performance when the front-end gain of 34 dB is selected with LNA gain setting number 6 (max -2 dB) and TA gain setting number 3.

Since the SCF is a highly-linear filter, little degradation in linearity has been measured. In Figure 21, two pairs of measured plots at SCF output show the lowpass filtering where the 3-dB frequencies are set to 150 kHz and 270 kHz.

6. CONCLUSION

We have presented an RF direct sampling technique that achieves great selectivity right at the mixer level. The dynamic range requirements of the following ADC are thus significantly relaxed. The selectivity is digitally controlled by the LO clock frequency and the capacitance ratio, both of which are extremely precise in digital deep-submicron CMOS processes. In order to validate the proposed technique, the *multi-tap direct sampling mixer* (MTDSM)-based front-end RX has been fabricated as part of commercial Bluetooth and GSM radios in digital deep-submicron CMOS processes. We have also presented implementation details of the GSM receiver front end realized in a 90-nm digital CMOS technology. It includes LNA, transconductance amplifier (TA), mixer for I

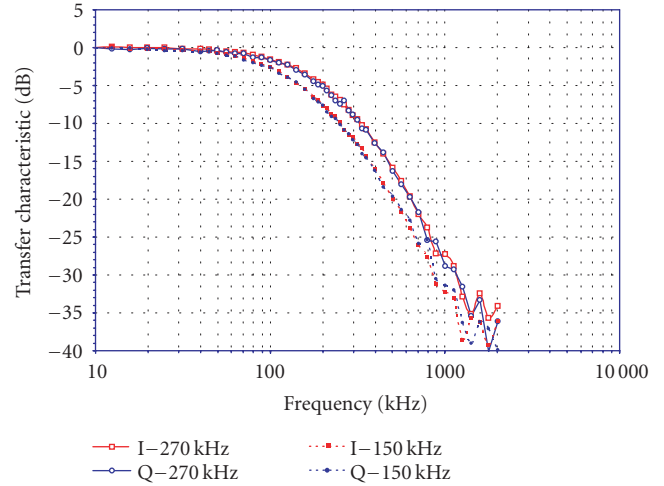


FIGURE 21: Measured filtering characteristics.

and Q channels with switched capacitor filter (SCF). While providing 35 digitally configurable gain steps ranging from 40 dB down to 7.5 dB, this fully integrated front-end circuit demonstrates a good noise figure of 1.8 dB at 40 dB maximum gain and +50 dBm IIP2 at 34 dB of gain, while a million of digital logic gates are simultaneously running on the same die. This paper demonstrates feasibility and attractiveness of employing the charge-domain RF signal processing within a larger system-on-chip (SoC) designs.

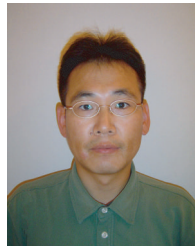
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