High-buck in Buck and High-boost in Boost Dual-Mode Inverter (Hb^{2}DMI)

Mohammad Ali Abbaszadeh, Mohammad Monfared, *Senior Member, IEEE*, and Hamed Heydari-doostabad, *Member, IEEE*

Abstract- The application of the dual-mode time-sharing technique in a novel transformerless photovoltaic (PV) inverters is proposed and investigated. The simultaneous high step-down or high step-up conversion with 97.6 % peak efficiency and injected current with THD < 2% is achieved. The leakage current problem, which is a main concern with the transformerless PV inverters, is around 20 mA. The indirect current control, especially at transition modes of operation is highly improved by utilizing a fast dead-beat control scheme. The working principles of the proposed converter show that the step-down and the step-up voltage gains are $(D/(1-D))^2$ and $D/(1-D)^2$, respectively. Furthermore, a 1 kW, 220 VAC and 200 VDC experimental prototype is implemented to confirm the theoretical achievements.

Index terms- Dual-mode time-sharing, leakage current, on-grid inverter, transformerless.

I. Introduction

PHOTOVOLTAIC (PV) inverters can be categorized based on the power rating of the converter. The micro-inverters are usually smaller than 400 W and the string-inverters are commonly 2 kW or less [1]. The use of transformer-based structures is very common because of the need for high voltage gain for micro-inverters. As a result, the efficiency of micro-inverters is almost lower than the string-inverters. Transformerless PV converters offer high energy conversion efficiencies, safety and low costs. Some specific conditions such as low number of panels in series, partial shading, panel ageing, temperature variation etc. cause the voltage of the PV panels to be less than the peak value of the grid voltage. Accordingly, a step-up DC-DC converter as the pre-front stage for the inverter is essential for the grid-tied applications resulting in the two-stage converters [1]–[3]. The traditional two-stage converters suffer from either unnecessary switching losses [4]–[6] or conduction losses [7]–[9]. However, in [9] a parallel power processing is used, which reduces the switching and conduction losses of a two-stage converter. In two-stage converters, the DC chopper always operates at high frequency switching to keep a constant output voltage in spite of the fluctuations in the voltage of the energy source. Furthermore, the inverter in the second power processing stage is intended to produce the AC voltage and injects all available output power into the grid with a sinewave carrier-based high-frequency pulse width modulation (PWM) control.

The dual-mode time-sharing technique which was proposed in [10], intelligently reduces the unnecessary high-frequency switching losses by assigning the time to use either the DC stage or the inverter stage during each period of the grid voltage. In this technique, the step-up mode of the converter only works when the PV voltage level is less than the instantaneous value of the grid voltage and the step-down mode operates when the PV voltage level is higher than the instantaneous value of the grid voltage. Consequently, in comparison with the classical two-stage grid-tied transformerless converters, the dual-mode converters are even more efficient.

More efficiency improvement of the dual-mode converter has been introduced in [11]. In this converter, the traditional interleaved boost converter at the PV side in front of the traditional buck converter and full-bridge unfolding stage at the grid side has been proposed. The two-stage dual-mode topology is even more improved by changing the position of the boost and the buck stages in front of the half-bridge inverter, known as the *Aalborg* inverter (buck in buck and boost in boost inverter) in [12] and in front of the full-bridge inverter in [13]. These let share a common inductance between the input-buck and the output-boost stages. The *Aalborg* inverter suffers from some drawbacks, such as the requirement for two DC sources and increased number of semiconductors. To improve the efficiency and avoid the unbalance of two input DC voltage sources of the *Aalborg* inverter, a coupled-inductor (CI) is used to regulate both input DC sources in [14] and [15]. A new tap-inductor (TI) based buck-boost inverter to provide very high step-up voltage gain presented in [16]. Despite the increased number of components and inappropriate transient during low grid voltage at zero-crossing points, the overall efficiency has improved. Recently, to improve the efficiency of the dual-mode converters, a three-phase interleaved with a parallel topology has been proposed in [17] and [18], respectively. Both converters suffer from numerous elements and complicated PWM strategies.

However, the inappropriate transients of injected current from negative to positive half-cycles at the zero-crossing points of grid voltage and from the step-down to the step-up modes of operation, low voltage gain, high voltage and current stress of devices, are the main weaknesses of the dual-mode converters.

Manuscript received September 13, 2019; revised December 26, 2019 and March 3, 2020; accepted April 1, 2020.
(*Corresponding author: Mohammad Monfared.*)

M. A. Abbaszadeh and M. Monfared are with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran (e-mail: mohammad.abbaszadeh@mail.um.ac.ir; m.monfared@um.ac.ir).

H. Heydari-doostabad is with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, Ireland (e-mail: hamed.heydari-doostabad@ucd.ie).

To tackle these issues, a high gain DC-DC converter as the DC stage with a wide range of output voltage during both step-down and step-up modes is convenient.

Clearly, the traditional buck converter operates with an extremely low duty cycle in the high step-down applications, resulting in large size of the filter, poor current ripple cancellation, high switching and conduction losses and limited attainable switching frequencies [19].

Furthermore, a high step-up voltage conversion in the traditional step-up converters needs a very high duty cycle or turn ratio, resulting in increasing the copper loss of windings, the leakage inductance, the voltage spike, stress on semiconductors, conduction losses, severity of diode revers-recovery problem and electromagnetic interference (EMI) [20].

Consequently, an integration of a high step-down converter with a high step-up converter offers more proper performance. This paper proposes a new two-stage transformerless PV inverter with the dual-mode time-sharing conversion technique. The DC stage is a novel wide range high-voltage gain converter with step-down and step-up modes and positive output voltage polarity. In the step-down mode, the voltage gain is quadratic, the converter works with two high-frequency switches and a reasonable number of components to reach a high voltage gain, which causes low voltage and current stresses on semiconductors. In the step-up mode, the voltage gain is semi-quadratic, which causes higher voltage gain and the number of high-frequency switch is reduced to one. Therefore, the number of components and the power losses are minimized.

The flexible reactive power control system qualifies a better integration of PV the system into the low-voltage grid and based on recent standards, such as VDE-AR-N-4105, transformerless inverters need to have reactive power capability as well as low voltage ride-through capability. According to [18], to have the reactive power capability, a PV inverter needs to provide a current path during the zero-voltage states at the negative power region (NPR). The NPR is defined as the time region during which the instantaneous values of the grid current and voltage have opposite polarities.

A modified modulation strategy developed for the proposed inverter, which allows the reactive power exchange capability.

Finally, an indirect dead-beat (IDB) current controller is adopted that offers accurate, fast and smooth control performance under different working conditions. Various experimental results on a 1 kW prototype are presented which validate the performance of the proposed converter. Furthermore, the proposed converter can be classified as a string-inverter, according to the input DC voltage range and the rated power. Consequently, a thorough comparison between the proposed converter and the major string-inverters has been done.

This paper is organized as follows. The basics of the proposed converter and the states of operation are introduced in Section II. Section III presents the IDB current control scheme. The comparison of the proposed topology with the main competitors is presented in Section IV. In Section V, the experimental results and analysis are provided and the conclusion is given in Section VI.

II. Proposed High Buck in Buck and High Boost in Boost Dual Mode Inverter (Hb^{2}DMI)

As shown in Fig. 1, the proposed Hb^{2}DMI consists of six switches (S_1, S_2, S_{p1}, S_{p2}, S_{n1} and S_{n2}), four diodes (D_1-D_4), two inductors (L_1, L_2), the lifting capacitor C_{dc}, the output capacitor C_o and the grid-side inductor filter L_g. The proposed PV inverter is a step-down and step-up DC to DC converter followed by the unfolding stage to inject alternative current to the grid.

The proposed DC to DC converter works with different voltage gain relations during the step-down and the step-up modes. During the step-down mode, the switches S_1 and S_2 are PWM controlled, synchronously. During the step-up mode, the switch S_1 is always on and the switch S_2 is PWM controlled.

A. Operation Modes

As shown in Fig 2(a), once the PV voltage is higher than the absolute instantaneous voltage of the grid, the step-down mode of the converter starts. Also, as soon as the PV voltage is lower than the absolute value of grid voltage, the converter works in the step-up mode of operation. Fig. 2(b) shows the realization of the overall modulation algorithm.

The proposed Hb^{2}DMI works in six distinct modes of operation, depicted in Fig. 3 and illustrated in the following:

Mode Ⅰ: (t_0-t_1 and t_2-t_3) During the step-down mode at the positive half cycle, two distinct states can be recognized:

State 1 ($NT_s < t < (N+D)\ T_s$) where T_s is the sampling time, N is the number of switching (sampling) intervals and t is time: the switches S_1 and S_2 and the diode D_3 conduct, while the diodes D_1, D_2 and D_4 are reverse biased. From Fig. 3(a), it can be seen that the inductor L_1 charges from the input source V_{PV} via the diode D_3, while the inductor L_2 charges from the capacitor C_{dc} and the load is supplied from the output capacitor C_o. The voltages across inductors are

$$v_{L1} = +V_{PV} \tag{1}$$

$$v_{L2} = -v_{Cdc}. \tag{2}$$

State 2 ($(N+D)T_s < t < (N+1)T_s$): the switches S_1 and S_2 are turned off and D_3 is reverse biased, while D_1, D_2 and D_4 conduct. As shown in Fig. 3(a), the inductor L_1 discharges into C_{dc} through D_1 and D_4. The inductor L_2 discharges into C_o through D_2. The voltages are

$$v_{L1} = -v_{Cdc} \tag{3}$$

$$v_{L2} = +V_o. \tag{4}$$

From the voltage-second balance for L_1, the voltage across the capacitor C_{dc} can be obtained from (1) and (3) as

$$v_{Cdc} = D/(1-D)V_{PV} \tag{5}$$

where D is the duty cycle of the switch.

The voltage-second balance for the inductor L_2 gives the voltage gain of the proposed converter during the step-down mode from (2), (4) and (5) as

$$M_{step-down} = \frac{V_o}{V_{PV}} = \left(\frac{D}{1-D}\right)^2. \tag{6}$$

From (6), it is obvious that the proposed topology can sharply step-down the input voltage when the duty cycle is below 0.5. It also can step-up when the duty cycle is beyond 0.5.

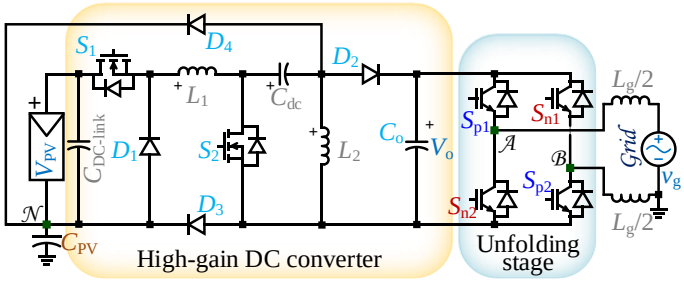

Fig. 1. Proposed Hb²DMI.

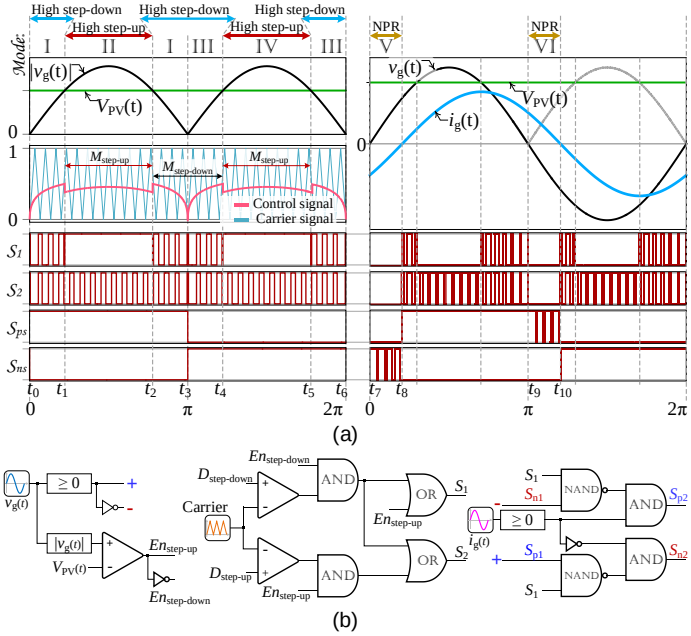

Fig. 2. Operation principle:
(a) PWM signals at PF = 1 (left) and PF ≠ 1 (right) and (b) realization.

Mode II: (t_1-t_2) When the PV voltage is lower than the grid voltage at the positive half cycle, the proposed converter operates in the step-up mode. It must be mentioned that the proposed topology offers a considerably higher voltage gain in the step-up mode by keeping on the switch S_1.

There are two states for the step-up mode as:

State 1 ($NT_s < t < (N+D)\,T_s$): the switches S_1 and S_2 conduct and the diode D_3 is forwarded biased and conducts too. According to the previous explanations for Fig. 3(b), the inductors L_1 and L_2 are charged and the load is supplied from C_o. Therefore, the inductor voltage equations in this state are

$$v_{L1} = +V_{PV} \tag{7}$$

$$v_{L2} = -v_{Cdc}\,. \tag{8}$$

State 2 ($(N+D)T_s < t < (N+1)T_s$): the switch S_2 is turned off and the diodes D_1 and D_3 are reverse biased, while D_2 and D_4 conduct. From Fig. 3(b), the positive voltage across C_{dc} is the difference between the input voltage and the voltage across L_1. The inductor L_2 discharges into C_o through D_2. The inductors voltage equations are

$$v_{L1} = +V_{PV} - v_{Cdc} \tag{9}$$

$$v_{L2} = +V_o\,. \tag{10}$$

The voltage across C_{dc} is readily obtained from (7) and (9) as

$$v_{Cdc} = 1/(1-D)V_{PV}\,. \tag{11}$$

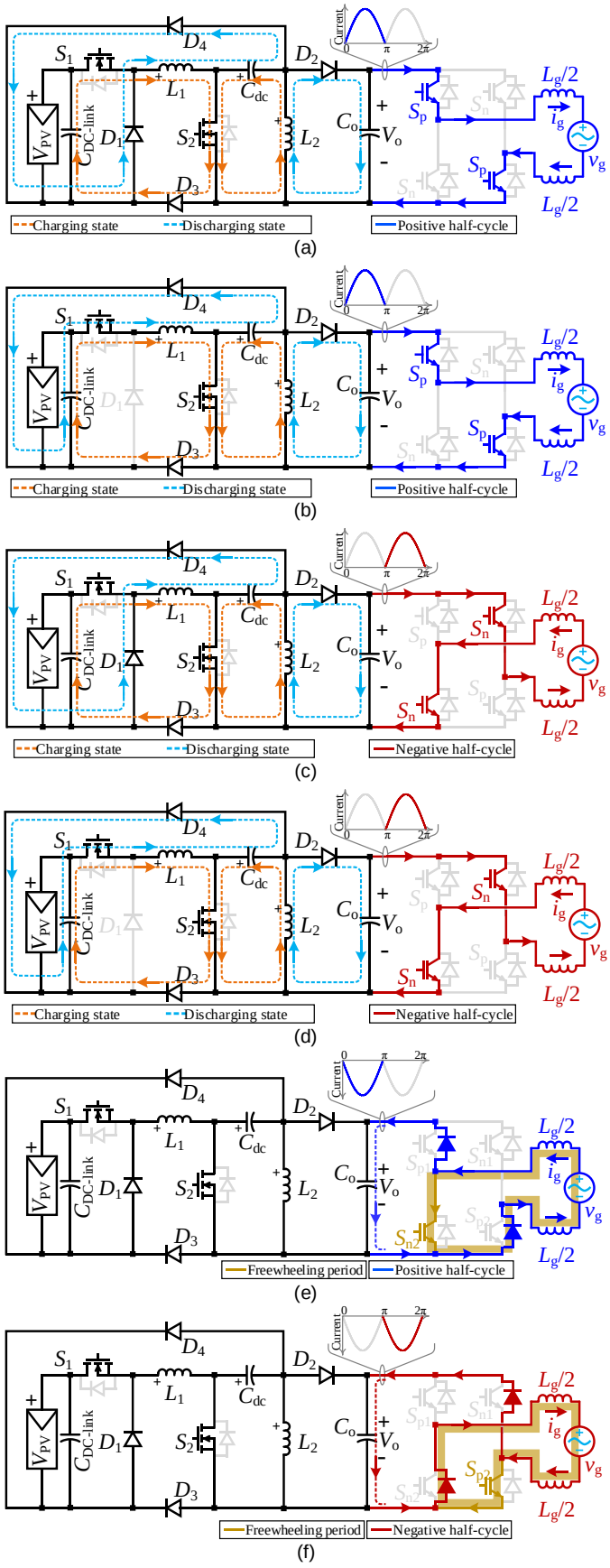

Fig. 3. Six operation modes of Hb²DMI: (a) mode I, (b) mode II, (c) mode III, (d) mode IV, (e) mode V and (f) mode VI.

TABLE I
COMPARISON BETWEEN STRUCTURE 1 AND 2

	Structure 1	Structure 2
No. of semiconductors:	2 switches 4 diodes	1 switch 3 diodes
Voltage gain (V_o/V_{PV}):	$\left(D/(1-D)\right)^2$	$D/(1-D)^2$
Total voltage stress: $0 \le t < DT_s$	$\frac{1}{(1-D)^2}V_{PV}$	$\frac{3-D}{1-D}V_{PV}$
Total voltage stress: $DT_s \le t < T_s$	$\frac{2D^2-D+1}{(1-D)^2}V_{PV}$	$\frac{D^2-D+1}{0.5(1-D)^2}V_{PV}$

Similarly, the voltage gain during the step-up mode of operation can be obtained from (8), (10) and (11) as

$$M_{\text{step-up}} = \frac{V_o}{V_{PV}} = \frac{D}{(1-D)^2}. \quad (12)$$

Evident from (12), the proposed converter can step-up the input voltage when the duty cycle is higher than 0.38.

As shown in Fig 3(a) and (b), during both modes I and II, the switches S_{p1} and S_{p2} conduct.

Mode III: (t_3-t_4 and t_5-t_6) When the PV voltage is higher than the absolute value of grid voltage during the negative half cycle, the proposed converter operates in the step-down mode which has voltage gain $M_{\text{step-down}}$ of (6). As shown in Fig 3(c), during this mode, the switches S_{n1} and S_{n2} are turned on. Similar to mode I, S_1 and S_2 are PWM controlled, simultaneously.

Mode IV: (t_4-t_5) When the PV voltage is lower than the absolute value of grid voltage during the negative half cycle, the proposed converter operates in the step-up mode with $M_{\text{step-up}}$ of (12). According to Fig 3(d), during this mode, the switches S_{n1} and S_{n2} receive the gate signals. Similar to mode II, S_1 is always on and only S_2 is PWM controlled.

Mode V: (t_7-t_8) During the positive half cycle of the grid voltage and when the instantaneous value of i_g is negative (as shown in Fig. 3(e)), the current through L_g increases in the freewheeling circuit consisting of S_{n2} and the body diode of S_{p2}.

Mode VI: (t_9-t_{10}) During the negative half cycle of the grid voltage and when the instantaneous value of i_g is positive (as shown in Fig. 3(f)), the current through L_g increases in the freewheeling circuit consisting of S_{p2} and the body diode of S_{n2}.

It must be mentioned that the proposed DC topology is able to operate step-down or step-up in both modes I and III (structure 1) and modes II and IV (structure 2). As shown in Table I, the proposed DC structure 2 has a lower number of semiconductors and higher step-up voltage gain than structure 1. However, the total voltage stress (TVS) of structure 1 during the step-down mode is lower. Similarly, the TVS of structure 2 during the step-up mode is lower. Reducing the applied voltage usually has a positive impact on efficiency and reliability. Consequently, to have the lowest overall voltage stress in the converter and at the same time to increase the voltage gain, the structure 1 during the step-down mode and the structure 2 during the step-up mode is chosen.

Due to the fewer number of components in the proposed structure 2, it could be a good choice for implementing the PV inverter. However, because of the higher voltage rating required compared to the proposed structure 1, it is more advantegous to disable the structure 2 at the high voltage levels of PV (V_{PV} > v_g) and use structure 1 instead. Therefore, the dual-mode converter is proposed.

B. Design of Components

The capacitor $C_{\text{DC-link}}$ performs as a buffer for the instantaneous power difference between the grid and the PV. Thus, to maintain the ripple of the DC-link voltage (ΔV_{DC}) below a specific value, the required $C_{\text{DC-link}}$ is:

$$C_{\text{DC-link}} = P_0/(\omega_0 V_{PV}\Delta V_{DC}) \quad (13)$$

where P_0 is the average power, ω_0 is the grid angular frequency and V_{PV} is the PV side DC voltage.

The inductors L_1 and L_2 required for continuous conduction mode can be calculated as

$$L_{1,\text{step-down}} \ge \frac{D^2V_{PV}^2}{2f_sP_0}, L_{1,\text{step-up}} \ge \frac{DV_{PV}^2}{2f_sP_0} \quad (14)$$

$$L_{2,\text{step-down}} \ge \frac{D^4V_{PV}^2}{2(1-D)^2f_sP_0}, L_{2,\text{step-up}} \ge \frac{D^2V_{PV}^2}{2(1-D)^2f_sP_0} \quad (15)$$

where f_s is the switching frequency.

The voltage ripples of capacitors C_{dc} and C_o define the minimum required capacitances in both modes as

$$C_{\text{dc,step-down}} \ge \frac{(1-D)^2P_0}{f_sD^2V_{PV}^2\Delta v_{Cdc}}, C_{\text{dc,step-up}} \ge \frac{(1-D)^2P_0}{f_sV_{PV}^2\Delta v_{Cdc}} \quad (16)$$

$$C_{\text{o,step-down}} \ge \frac{(1-D)^4P_0}{f_sD^3V_{PV}^2\Delta v_{Co}}, C_{\text{o,step-up}} \ge \frac{(1-D)^4P_0}{f_sDV_{PV}^2\Delta v_{Co}}. \quad (17)$$

The value of grid side inductor L_g is chosen from the maximum allowed current ripple Δi_g as follows

$$L_g \ge \Delta v_{Co}/(2f_s\Delta i_g) \quad (18)$$

III. INDIRECT DEAD-BEAT CURRENT CONTROL

The current controller must ensure the current through L_g, shown as i_g, is a pure sinusoid. Following the proposal of [12] and due to the problem of non-minimum phase with the direct current control, the indirect current control of converter by adjusting the current of L_2, i_{L2}, instead of i_g is employed. The formulation is based on the instantaneous power balance at the two ports of the circuit, detailed in the Appendix, that establishes a relation between the grid current reference and the inductor L_2 current reference as

$$\begin{cases} i_{L2,\text{step-down}}^* = |i_g^*|\left(1+\sqrt{|v_g(t)|/V_{PV}}\right) & V_{PV} \ge |v_g| \\ i_{L2,\text{step-up}}^* = 2|i_g^*|\left(-\frac{V_{PV}}{|v_g(t)|}+\sqrt{\left(2+\frac{V_{PV}}{|v_g(t)|}\right)^2-4}\right)^{-1} & V_{PV} < |v_g| \end{cases} \quad (19)$$

where | | is the absolute operator. The rectified sinusoidal current, i_{L2} can be regulated by directly calculating the optimal duty cycle for the next switching period by a dead-beat strategy [17]. As will be shown, the simple yet efficient indirect dead-beat control technique only requires the value of L_2 to directly calculate the control signal for the PWM block from the measured source and grid voltages, measured inductor current and its reference.

During all these modes of operation, when S_2 is on, the voltage across inductor L_2 can be determined as

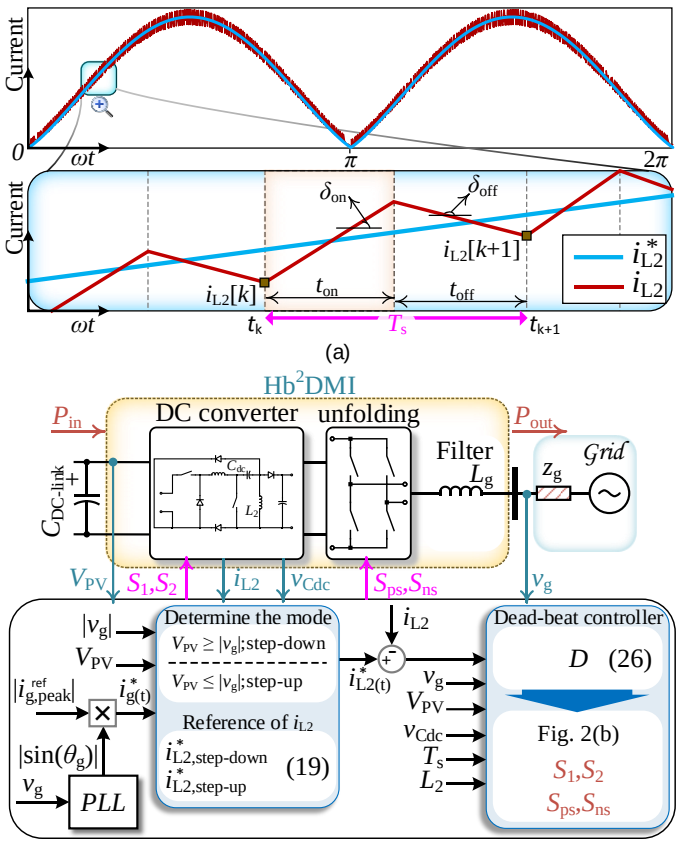

Fig. 4. Proposed indirect dead-beat controller: (a) waveforms and (b) control diagram.

$$v_{L2} = L_2\, di_{L2}/dt = -v_{Cdc}. \tag{20}$$

Similarly, when the switch S_2 is off, the inductor voltage is

$$v_{L2} = L_2\, di_{L2}/dt = +V_o. \tag{21}$$

Fig. 4(a) shows the slope of the inductor current during S_2 on state (δ_{on}) and during S_2 off state (δ_{off}), calculated as

$$\begin{cases} \delta_{on} = di_{L2}/dt = -v_{Cdc}/L_2 \\ \delta_{off} = di_{L2}/dt = +V_o/L_2 \end{cases} \tag{22}$$

From which the inductor current at the next sampling period ($i_{L2}[k+1]$) can be estimated from its current value ($i_{L2}[k]$) as

$$i_{L2}[k+1] = i_{L2}[k] + \delta_{on} \times t_{on} + \delta_{off} \times t_{off} \tag{23}$$

where t_{on} and t_{off} are on state and off state times of S_2, respectively.

The controller is intended to eliminate the error, i_e, between the reference current (i_{L2}*) and $i_{L2}[k+1]$, i.e.

$$i_e = i_{L2}^* - i_{L2}[k+1] = i_{L2}^* - i_{L2}[k] - \delta_{on} \times t_{on} - \delta_{off} \times t_{off} = 0 \tag{24}$$

which gives t_{on} is

$$t_{on} = \frac{i_{L2}^* - i_{L2}[k] - \delta_{off} T_s}{\delta_{on} - \delta_{off}}. \tag{25}$$

Using (25), the optimal duty cycle can be concluded as

$$D = \frac{t_{on}}{T_s} = \frac{L_2(i_{L2}^* - i_{L2}[k]) + v_{Cdc} T_s}{-v_{Cdc} - v_g}. \tag{26}$$

The simplified control diagram of Hb^{2}DMI is shown in Fig. 4(b). By comparing the instantaneous grid voltage and the PV voltage, the step-down or step-up mode of the Hb^{2}DMI is decided. Afterwards, the reference current i_{L2}* is calculated from (19). The reference and measured values of i_{L2} are then used by the dead-beat algorithm to determine the optimal duty cycle from (26). The PWM modulator, depicted in Fig. 2(b), uses this duty cycle to generate the switching signals.

IV. Practical Considerations and Comparison

A. Semiconductors Ratings

The voltages across the switches and the diodes during the step-down and the step-up modes are

$$V_{S1,step-down} = V_{PV} \tag{27}$$

$$V_{S2,step-down} = \frac{D}{(1-D)^2} V_{PV}, V_{S2,step-up} = \frac{1}{(1-D)^2} V_{PV} \tag{28}$$

$$V_{D1,step-down} = V_{D1,step-up} = V_{PV} \tag{29}$$

$$V_{D2,step-down} = \frac{D}{(1-D)^2} V_{PV}, V_{D2,step-up} = \frac{1}{(1-D)^2} V_{PV} \tag{30}$$

$$V_{D3,step-down} = \frac{D^2}{(1-D)^2} V_{PV}, V_{D3,step-up} = \frac{D}{(1-D)^2} V_{PV} \tag{31}$$

$$V_{D4,step-down} = \frac{D}{1-D} V_{PV}, V_{D4,step-up} = \frac{1}{1-D} V_{PV}. \tag{32}$$

The min/max currents of the inductors in both modes are as

$$I_{L1,min,max} = \begin{cases} P_0/(DV_{PV}) \pm DV_{PV}/(2 f_s L_1) & V_{PV} \geq |v_g| \\ P_0/V_{PV} \pm DV_{PV}/(2 f_s L_1) & V_{PV} < |v_g| \end{cases} \tag{33}$$

$$I_{L2,min,max} = \begin{cases} \dfrac{(1-D)P_0}{D^2 V_{PV}} \pm \dfrac{0.5 D^2 V_{PV}}{(1-D) f_s L_2} & V_{PV} \geq |v_g| \\ \dfrac{(1-D)P_0}{DV_{PV}} \pm \dfrac{0.5 DV_{PV}}{(1-D) f_s L_2} & V_{PV} < |v_g| \end{cases} \tag{34}$$

From which, the peak current of the switches and the diodes are

$$\begin{aligned} &I_{S1} = I_{L1}, I_{S2} = I_{L1} \\ &I_{D1} = I_{L1}, I_{D2} = I_{L2}, I_{D3} = I_{L1}, I_{D4} = I_{L1} \end{aligned}. \tag{35}$$

B. Common Mode Analysis

The equivalent common-mode circuit of Hb^{2}DMI includes the parasitic capacitor between the ground and the PV array, C_{PV}, the ground resistance, R_g, the filter inductance, L_g and the pole voltages (V_{AN}, V_{BN}). The common-mode leakage current, i_{CM}, originated from the common-mode voltage (V_{CM}) is

$$i_{CM} = V_{CM}/Z_{CM} = \frac{(V_{AN} + V_{BN})/2}{0.25 L_g s + R_g + 1/(C_{PV} s)} \tag{36}$$

where Z_{CM} is the common-mode impedance that its magnitude is minimum at its resonance frequency.

Furthermore, the leakage current originated from the grid is

$$i_{CM,vgrid} = 0.5\,|v_g|/Z_{CM} \tag{37}$$

The grid is supposed to be ideal and it will cause a very low leakage current.

Furthermore, one of the main advantages of Hb^{2}DMI is the low-frequency variation of V_{CM}. The values of V_{AN}, V_{BN} and V_{CM} during four modes of operation are summarized in Table II. It is clear that V_{CM} varies at double the line frequency.

TABLE II
COMMON MODE AND POLE VOLTAGES

Mode *I* to *IV*:	V_{AN}	V_{BN}	V_{CM}
Charging state [0 - DT_s]:	S_2V_O	0	$V_O/2$
Discharging state [DT_s - T_s]:	0	$\bar{S}_2V_O$	

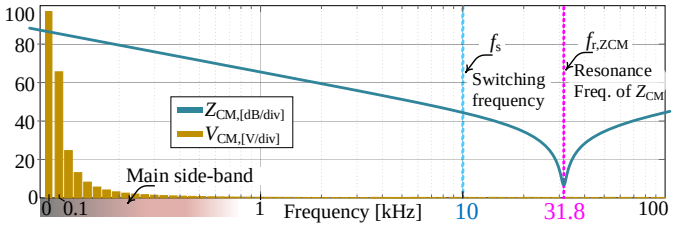

Fig. 5. Magnitude Bode plot of Z_{CM} and harmonic spectrum of V_{CM}.

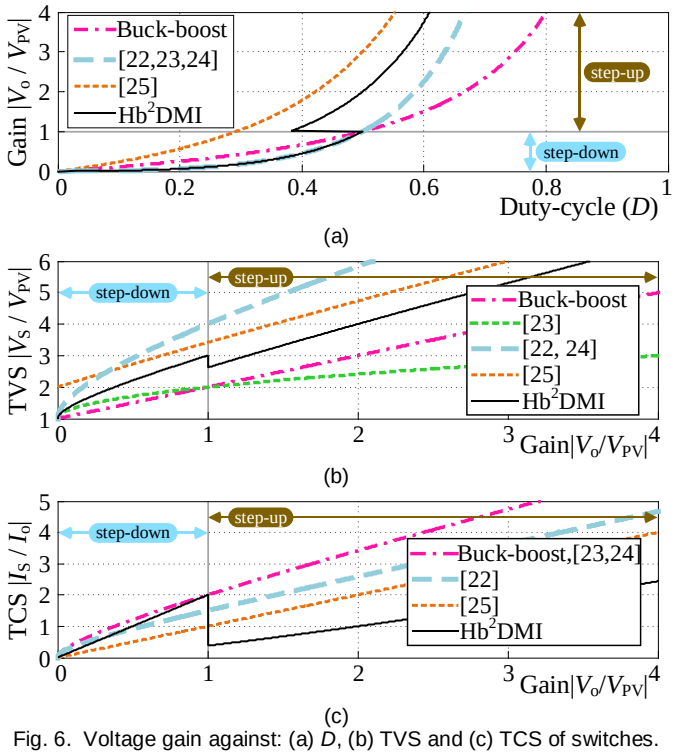

Fig. 6. Voltage gain against: (a) *D*, (b) TVS and (c) TCS of switches.

Therefore, the resonant frequency of Z_{CM} is much far from the main sideband of V_{CM}.

The Bode magnitude plot of Z_{CM} and the harmonic spectrum of V_{CM} are plotted in Fig. 5. Clearly, the magnitude of Z_{CM} is considerably high at low frequencies. Consequently, as it was discussed in [21], the leakage current originated from V_{CM} ripples is almost negligible.

C. Comparison of Proposed Inverter

The DC stage of Hb²DMI operates in two modes which results in a high voltage gain in step-up mode, higher than those of competitors in [22]–[24] and traditional buck-boost converters as shown in Fig. 6(a).

The DC converter in [25] has a higher voltage gain in the step-up mode but the proposed DC converter has a much wider operating range and a high voltage gain in the step-down mode.

Furthermore, as shown in Fig. 6(b), the normalized voltage stress of switches in the proposed DC converter during both step-up and down modes is lower than the converters presented in [22], [25] and [24].

TVS and total current stress (TCS) are defined as the sum of the blocking voltages and conducting currents of components during $0 < t < DT_s$ or $DT_s < t < T_s$.

The traditional quadratic buck-boost converter in [23] cannot work in a wide range. When the duty cycle is larger than 0.5, the voltage stress of a diode will become negative and results in malfunction of the converter in [23]. This disadvantage causes the traditional quadratic buck-boost converter works only in step-down mode as it was mentioned in [22]. Besides, as shown in Fig. 6(c), the proposed DC converter offers less current stress of switches than [23] and [24] during step-down and less than [22]–[24] during step-up mode. Table III shows a comparison in terms of the number of elements, voltage gain, efficiency, total harmonic distortion (THD) of injected current and other characteristics, among Hb²DMI and the modern single-phase inverters. The voltage gain of Hb²DMI is higher than all competitors at the step-down mode. During the step-up mode, the voltage gain of [26] is higher than Hb²DMI.

TABLE III
COMPARISON AMONG HB²DMI AND THE COMPETITORS

	Converter [11]	Aalborg [12]	CI Aalborg [14]	Converter [13]	qSBI [26]	Buck-boost [16]	TI buck-boost [16]	IIDMI [17]	DMIMI [18]	Hb²DMI
No. Inductor (total *L*):	3 (0.8 mH)	3 (1.8 mH)	2 (5.4 mH)	3 (1.8 mH)	2 (12 mH)	2 (0.7 mH)	2 (0.7 mH)	4 (3.7 mH)	3 (2.5 mH)	3 (3 mH)
No. Capacitor (total *C*):	2 (2002μF)	3 (2.2 μF)	3 (2.2 μF)	4 (10 μF)	2 (2020 μF)	2 (62 μF)	2 (62 μF)	2 (2002 μF)	3 (2002 μF)	2 (682 μF)
No. Diode:	3	4	6	4	6	0	0	3	4	4
No. Switch:	7	6	6	8	4	6	8	11	10	6
No. High frequency switch per half-cycle:	2@buck 1@boost	2	2	2	4	2	2	6	5	2@buck 1@boost
No. Gate driver:	4	6	6	7	4	4	5	6	4	4
No. DC source:	1	2	2	2	1	1	1	1	1	1
DC stage voltage gain (step-down; step-up):	*D* 1/(1-*D*)	*D* 1/(1-*D*)	*D* 1/(1-*D*)	*D* 1/(1-*D*)	*D* 1/(1-2*D*)	*D*/(1-*D*)	*D* (1+*D*(n2/n1))/(1-*D*)	*D* 1/(1-*D*)	*D* *D*/(1-*D*)	$D^2/(1-D)^2$ $D/(1-D)^2$
Switching Freq. [kHz]:	50	40	40	50	10	60	60	10	30	10
Rated power [kW]:	2.5	2	0.5	1.5	0.8	1	1	2.2	1	1
Leakage current [mA]:	-	-	-	80.7	-	-	-	26.8	20	≈ 20
Injected current THD [%]:	-	-	-	4.61	2.61	-	-	1.9	2.31	≈ 2
Peak efficiency [%]:	98.5	97.6	-	97.65	< 94	-	-	98.2	97.31	97.6
Freq. of V_{CM}:	Low	Low	Low	Low	High	-	-	Low	High	Low
Reactive power capability ?:	No	No	No	No	No	No	No	No	Yes	Yes

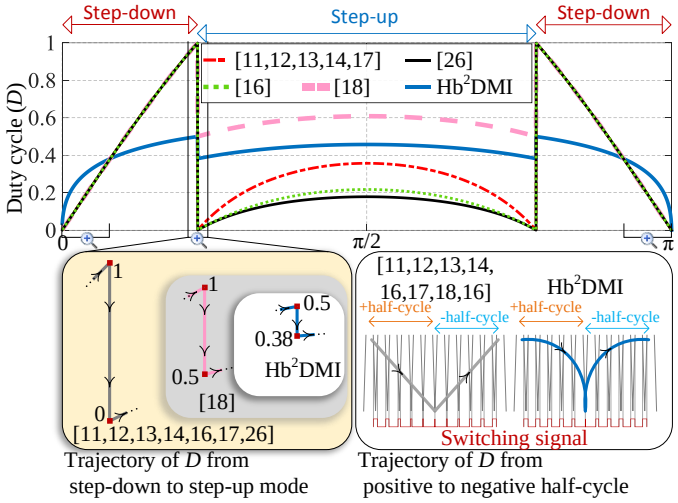

Fig. 7. Duty cycle of the main single-phase inverters.

Nonetheless, the total number of elements in [26] and [16] is lower than Hb²DMI, but the number of switches with high-frequency operation for Hb²DMI is minimum.

Due to high-frequency variation of V_{CM} in [18], [26] and [16], the common mode filter or increasing the switching frequency is essential, which both reduce the efficiency.

All the dual-mode converters in Table III suffer from inappropriate transients, both from step-down to step-up modes and positive to negative half-cycles and vice versa. These transients are caused by the high changes in the duty cycle between step-down and step-up modes and low value of the duty cycle at the moment of the half-cycle change.

As shown in Fig. 7, Hb²DMI offers more smooth duty cycle at the moment of changes between the step-down and the step-up modes. Furthermore, the high value of duty cycle at the transition between the positive and the negative half-cycles causes less ripple of i_g. Consequently, from the perspective of the quality of the injected current, the Hb²DMI is more advantageous for on-grid applications.

V. Performance Evaluation

A 1 kW laboratory prototype, shows in Fig. 8, is developed with the parameters listed in Table IV. An STMicroelectronics STM32F303 floating-point digital controller is used to implement the proposed current control algorithm.

Figure 9 shows the steady-state performance of the proposed converter under 1 kW output power. Clear from Fig. 9, the proposed converter generates highly sinusoidal current even when the grid voltage is harmonically polluted. With a closer look at the current waveform, one can detect a very smooth mode transition from the step-down to the step-up and from negative to positive half-cycle. This caused the THD of the Hb²DMI current remains as low as 2 %. The maximum ripple of around 10 % in the inductance current is also evident that is in accordance with the design criteria.

The transient response to the step jumps in the reference current and the input DC voltage are presented in Fig. 10. Clearly a fast-dynamic current performance is achieved and a high step change in the PV voltage has almost no effect on the output current waveform. The IDB current controller, as already expected, offers a high dynamic performance in response to any changes in the references, inputs and other disturbances.

As already mentioned, the common mode leakage current is a main concern with any grid connected PV converters. Fig. 11 shows the experimental results of the pole voltages, the common mode voltage and the resultant leakage current. Clearly, the common mode voltage of Hb²DMI changes at twice the line frequency, as already predicted in Table I. So, the leakage current is almost zero.

The proposed PWM technique allows Hb²DMI to operate below the unity power factor (UPF). As shown in Figs. 12(a) and (b), Hb²DMI with the proposed PWM strategy is operating properly for both leading and lagging power factors.

The transient performance of the proposed PWM and control system is investigated experimentally and the results are shown in Fig. 13. A fast and smooth transient response, either from UPF to leading power factor as shown in Fig. 13(a), or from UPF to lagging power factor as shown in Fig. 13(b) is obvious.

The measured THDs at different power levels are presented in Fig. 14(a). The proposed converter provides low THD values under different loading conditions. However, as already pointed out, the Hb²DMI current waveform is susceptible to deterioration at mode transition that slightly increases the THD. This effect is more obvious at lower powers.

As mentioned earlier, the IDB current controller needs the

Fig. 8. Experimental hardware prototype.

TABLE IV
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value
Input voltage V_{PV}	400 V, 200 V
Grid voltage v_g	220 V, 50 Hz
Switching frequency f_s	10 kHz
Nominal power	1 kW
Inductor L_1, L_2 and L_g	1 mH
Capacitor C_{dc}	680 µF
Capacitor C_o	2.2 µF, 39 µF
Parasitic capacitor C_{PV}	92 nF
$C_{DC\text{-}link}$	8160 µF
MOSFET	SPW35N60CFD IPW80R280P7
IGBT	IXGH48N60C3D1
Diode	IDW16G65C5 IDW15G120C5
Gate drivers (opto-coupler and isolated supply)	TLP250 and MAU153

value of L_2 to predict the optimal duty cycle. As a result, the performance of the IDB current controller, considering the L_2 mismatches, denoted by ΔL_2, in the term of THD is investigated and shown in Fig. 14(b). The stable operation of the proposed IDB current controller even with high mismatches is obvious. Besides the THD of the injected current remains below the standard requirement of 5 %.

The measured efficiencies under different loading levels are plotted in Fig. 14(c). Evidently, a very high peak efficiency is achieved. From this figure, the European Efficiency (EU) and the California Energy Commission (CEC) efficiency can be calculated as 97.07 % and 97.36 %, respectively.

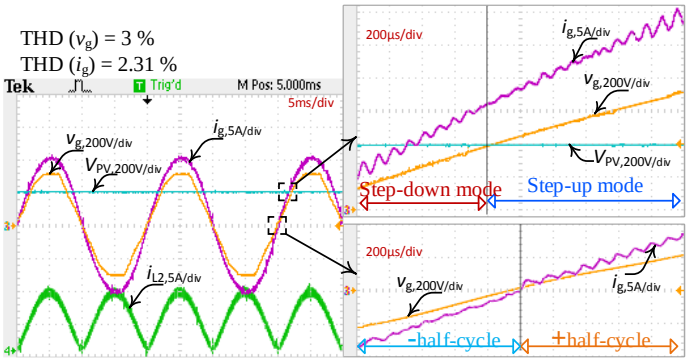

Fig. 9. Waveforms of PV voltage (V_{PV}), grid voltage (v_g), grid current (i_g), inductor current (i_{L2}) and zoomed views of transient from step-down to step-up mode and negative to positive half-cycle.

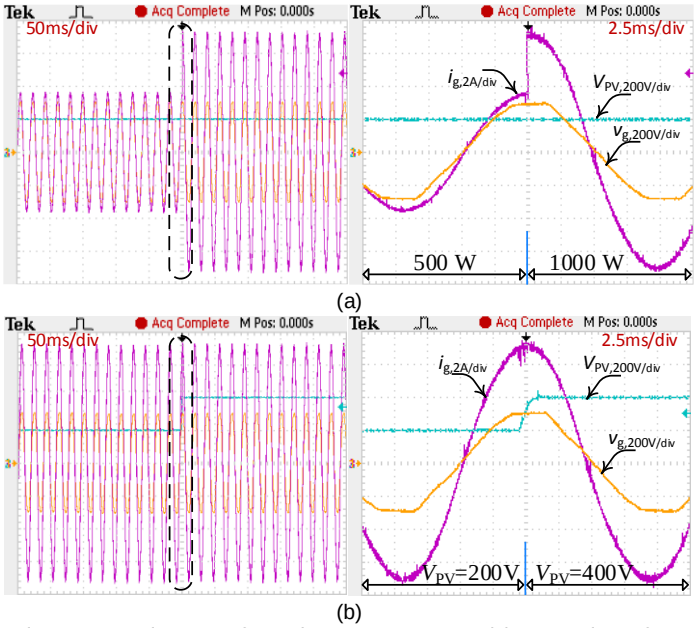

Fig. 10. Transient waveforms in response to step (a) current jump from half to full of rated power and (b) V_{PV} jump from 200 V to 400 V.

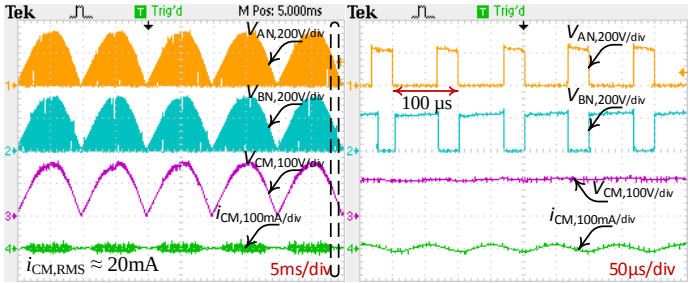

Fig. 11. Waveforms of V_{AN}, V_{BN}, V_{CM} and i_{CM}.

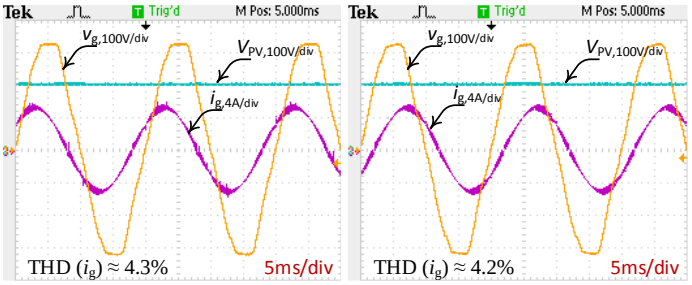

Fig. 12. Waveforms of V_{PV}, v_g and i_g under: (a) 0.8 leading and (b) 0.8 lagging power factors.

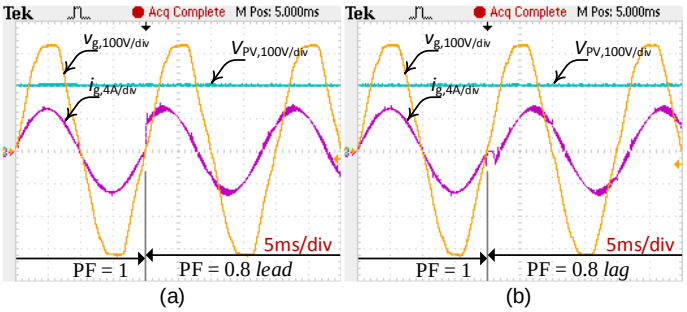

Fig. 13. Transient waveforms from unity to (a) 0.8 leading and (b) 0.8 lagging power factors.

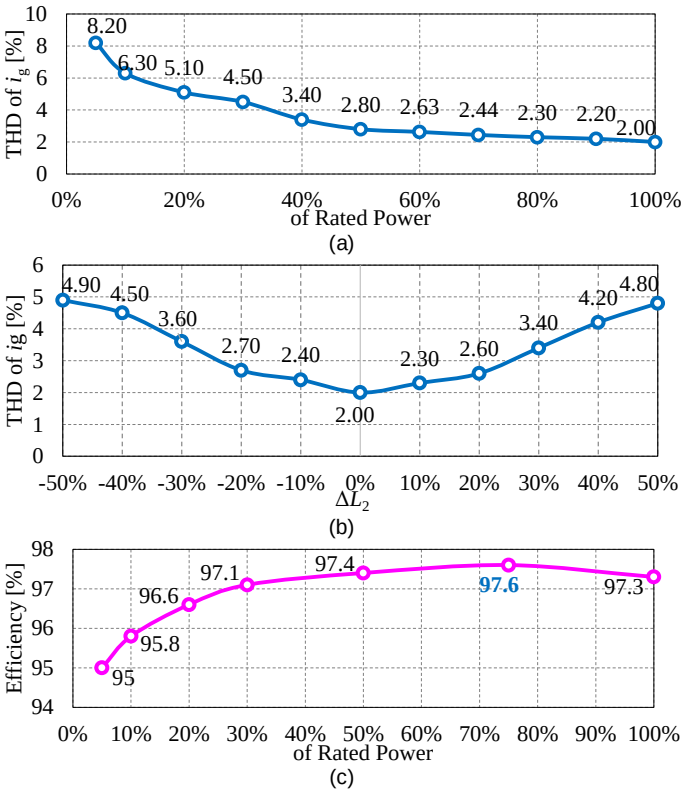

Fig. 14. (a) Grid-injected current THD% versus output power and (b) inductance mismatch under 1 kW, (c) efficiency versus output power.

VI. Conclusion

A new single-phase transformerless dual-mode inverter, as a two-stage topology is proposed that has a simple structure while provides a wide range of voltage gain to tackle the weaknesses of modern dual-mode inverters. The operating principles, components design, an indirect dead-beat current control, common mode analysis and comparisons with competitors are

presented. Through the theoretical analyses and the experimental results from a 1 kW prototype, it is demonstrated that the Hb²DMI offers many advantages, such as high step-down and step-up voltage gain, simple PWM scheme, low leakage current, high quality of injected current, reactive power exchange capability and high energy conversion efficiency that make it a proper solution for on-grid PV applications.

APPENDIX

Based on the instantaneous power balance the following equation can be written:

$$V_{\mathrm{PV}}(t)\times I_{\mathrm{PV}}(t)=v_{\mathrm{g}}(t)\times i_{\mathrm{g}}(t)\,. \tag{38}$$

During the step-down mode of operation, one has:

$$\begin{cases} i_{\mathrm{L1}}\times D=I_{\mathrm{PV}} \\ i_{\mathrm{L1}}=D/(1-D)i_{\mathrm{L2}} \end{cases} \Rightarrow I_{\mathrm{PV}}=\frac{D^2}{1-D}i_{\mathrm{L2}} \Rightarrow i_{\mathrm{L2}}=\frac{1}{1-D}i_{\mathrm{g}} \tag{39}$$

and the gain and duty cycle are:

$$M_{\text{step-down}}=\frac{V_{\mathrm{o}}}{V_{\mathrm{PV}}}=(\frac{D}{1-D})^2, D=\sqrt{\frac{V_{\mathrm{o}}}{V_{\mathrm{PV}}}}/(1+\sqrt{\frac{V_{\mathrm{o}}}{V_{\mathrm{PV}}}})\,. \tag{40}$$

From (39) and (40), one can yield:

$$i_{\text{L2,step-down}}=(1+\sqrt{v_{\mathrm{g}}/V_{\mathrm{PV}}})i_{\mathrm{g}}\,. \tag{41}$$

Similarly, during the step-up mode of operation, one can write:

$$\begin{cases} i_{\mathrm{L1}}=I_{\mathrm{PV}} \\ i_{\mathrm{L1}}=D/(1-D)i_{\mathrm{L2}} \end{cases} \Rightarrow I_{\mathrm{PV}}=\frac{D}{1-D}i_{\mathrm{L2}} \Rightarrow i_{\mathrm{L2}}=\frac{1}{1-D}i_{\mathrm{g}} \tag{42}$$

$$M_{\text{step-up}}=\frac{V_{\mathrm{o}}}{V_{\mathrm{PV}}}=\frac{D}{(1-D)^2}, D=0.5(2+\frac{V_{\mathrm{PV}}}{V_{\mathrm{o}}}-\sqrt{(2+\frac{V_{\mathrm{PV}}}{V_{\mathrm{o}}})^2-4}) \tag{43}$$

$$i_{\text{L2,step-up}}=2(-V_{\mathrm{PV}}/v_{\mathrm{g}}+\sqrt{(2+V_{\mathrm{PV}}/v_{\mathrm{g}})^2-4})^{-1}i_{\mathrm{g}}\,. \tag{44}$$

ACKNOWLEDGMENT

The authors would like to thank Science Foundation Ireland (SFI) SFI/16/IA/4496, Active Distribution Management Enabled by Distributed Power Electronics for their support.

REFERENCES

[1] R. Teodorescu, M. Liserre, and P. Rodríguez, *Grid Converters for Photovoltaic and Wind Power Systems*. Chichester, UK: John Wiley & Sons, Ltd, 2011.

[2] S. M. Sharkh, M. A. Abusara, G. I. Orfanoudakis, and B. Hussain, *Power Electronic Converters for Microgrids*. Singapore: John Wiley & Sons, Singapore Pte. Ltd, 2014.

[3] Y. Yang, K. A. Kim, F. Blaabjerg, and A. Sangwongwanich, *Advances in Grid-Connected Photovoltaic Power Conversion Systems*. Elsevier, 2019.

[4] Quan Li and P. Wolfs, "A Review of the Single Phase Photovoltaic Module Integrated Converter Topologies With Three Different DC Link Configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[5] D. Meneses, F. Blaabjerg, Ó. García, and J. A. Cobos, "Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[6] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4537–4551, Jul. 2015.

[7] M. Lee, J.-W. Kim, and J.-S. Lai, "Single inductor dual buck-boost inverter based on half-cycle PWM scheme with active clamping devices," *IET Power Electron.*, vol. 12, no. 5, pp. 1011–1020, May 2019.

[8] P. Li, R. Li, S. Cai, and Y. Hong, "Intermediate Voltage Regulation for Total Harmonic Distortion Reduction of Two-Stage Inverters Under Model Predictive Control Scheme via Observers," *IEEE Access*, vol. 7, pp. 51940–51951, 2019.

[9] A. Anurag, N. Deshmukh, A. Maguluri, and S. Anand, "Integrated DC–DC Converter Based Grid-Connected Transformerless Photovoltaic Inverter With Extended Input Voltage Range," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8322–8330, Oct. 2018.

[10] N. A. Ahmed, H. W. Lee, and M. Nakaoka, "Dual-Mode Time-Sharing Sinewave-Modulation Soft Switching Boost Full-Bridge One-Stage Power Conditioner Without Electrolytic Capacitor DC Link," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 805–813, 2007.

[11] Z. Zhao, M. Xu, Q. Chen, J.-S. (Jason) Lai, and Y. Cho, "Derivation, Analysis, and Implementation of a Boost–Buck Converter-Based High-Efficiency PV Inverter," *IEEE Trans. Power. Electron.*, vol. 27, no. 3, pp. 1304–1313, 2012.

[12] W. Wu, J. Ji, and F. Blaabjerg, "Aalborg inverter - A new type of 'buck in buck, boost in boost' grid-tied inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4784–4793, Sep. 2015.

[13] S. Dutta and K. Chatterjee, "A Buck and Boost Based Grid Connected PV Inverter Maximizing Power Yield from Two PV Arrays in Mismatched Environmental Conditions," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5561–5571, 2018.

[14] H. Wang, W. Wu, H. S. H. Chung, and F. Blaabjerg, "Coupled-Inductor-Based Aalborg Inverter with Input DC Energy Regulation," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3826–3836, 2018.

[15] S. Dutta and K. Chatterjee, "A Coupled Inductor based Buck-Boost type Grid Connected Transformerless PV Inverter having the Ability to Control Two Subarrays Simultaneously," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5543-5553, 2020.

[16] O. Husev, O. Matiushkin, C. Roncero-Clemente, F. Blaabjerg, and D. Vinnikov, "Novel Family of Single-Stage Buck–Boost Inverters Based on Unfolding Circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7662–7676, Aug. 2019.

[17] H. Heydari-doostabad and M. Monfared, "An Integrated Interleaved Dual-Mode Time-Sharing Inverter for Single-Phase Grid-Tied Applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 286–296, Jan. 2019.

[18] A. Pourfaraj, M. Monfared, and H. Heydari-doostabad, "Single-Phase Dual-Mode Interleaved Multi- level Inverter (DMIMI) for PV Applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2905-2915, Apr. 2020.

[19] M. Hajiheidari, H. Farzanehfard, and E. Adib, "High-Step-Down DC-DC Converter with Continuous Output Current Using Coupled-Inductors," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10936–10944, Nov. 2019.

[20] N. Elsayad, H. Moradisizkoohi, and O. Mohammed, "A New Single-Switch Structure of a DC-DC Converter with Wide Conversion Ratio for Fuel Cell Vehicles: Analysis and

Development," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. PP, no. c, pp. 1–1, 2019.

[21] Y. Chen, D. Xu, and J. Xi, "Common-Mode Filter Design for a Transformerless ZVS Full-Bridge Inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 2, pp. 405–413, Jun. 2016.

[22] N. Zhang, G. Zhang, K. W. See, and B. Zhang, "A Single-Switch Quadratic Buck–Boost Converter With Continuous Input Port Current and Continuous Output Port Current," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4157–4166, May 2018.

[23] D. MaksimoviC and S. Cuk, "Switching Converters with Wide DC Conversion Range," *IEEE Trans. Power Electron.*, vol. 6, no. I, pp. 151–157, 1991.

[24] S. Miao, F. Wang, and X. Ma, "A New Transformerless Buck-Boost Converter With Positive Output Voltage," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2965–2975, 2016.

[25] S. Ding and F. Wang, "A New Negative Output Buck–Boost Converter with Wide Conversion Ratio," *IEEE Trans. Ind. Electron.*, vol. 64, no. 12, pp. 9322–9333, Dec. 2017.

[26] M. Nguyen and T. Tran, "A Single-Phase Single-Stage Switched-Boost Inverter With Four Switches," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6769–6781, Aug. 2018.

Mohammad Ali Abbaszadeh received the B. Sc. and the M. Sc. degrees in electrical engineering from Ferdowsi university of Mashhad, Iran, in 2017 and 2020, respectively.

His research interests include power electronics, especially PV inverters, dc converters, power quality, and control systems.

Mohammad Monfared (S'07–M'10-SM'15) received the B.Sc. degree in electrical engineering from Ferdowsi University of Mashhad, Iran, in 2004, and the M.Sc. and Ph.D. degrees (both with honors) in electrical engineering from Amirkabir University of Technology, Tehran, Iran, in 2006 and 2010, respectively.

He is currently an Associate Professor at Ferdowsi University of Mashhad, Iran, where he has received the Best Researcher Award in 2015. His research interests include power electronics, renewable energy systems, and power quality.

Hamed Heydari-doostabad (M'20) received the Ph.D. (Hons.) degree in electrical engineering from the Ferdowsi University of Mashhad, Mashhad, Iran, in 2018. He is currently a Post-Doctoral Senior Power System Researcher with the School of Electrical and Electronic Engineering, University College Dublin (UCD), Dublin, Ireland.

His research interests include power electronics, especially grid-following-forming inverters, distributed energy resources (DER), PV inverters, dc converters, power quality, and control systems.