Design Considerations of Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection

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***Abstract*— Digital transmitter (DTX) offers the desired signal efficiency and flexibility than its analog counterpart by merging signal amplification and modulation. Yet, the high-speed digital baseband interface is challenging and bulky for achieving low out-of-band noise. This Brief is an analytical study of the DTX linear interpolation technique, which can be adapted easily for optimizing the replica rejection and noise-filtering capabilities of the DTX.**

***Index Terms*— Digital transmitter (DTX), linear interpolation, quantization noise, replicas.**

I. Introduction

FOR digital transmitter (DTX) design, switching power amplifier is usually deployed to improve the power efficiency. However, it is not trivial to add filters in the signal path. Charge-based filtering technique was proposed to suppress the noise floor [1] but the charge sharing operation limits its output power to be low. Thus, without filtering for both noise and sampling replicas, a SAW-less DTX is difficult to fulfill the stringent requirement of the out-of-band noise (–160 dBc/Hz) [2]. An in-phase and quadrature (I/Q) DTX can outperform a polar one in the noise floor level (e.g., –130 and –112 dBc/Hz at 100 MHz offset in [3], [4]) as the latter one suffers from the time misalignment of the amplitude modulated and phase modulated paths [4-6].

The noise floor of an I/Q mixing digital-to-analog converter (DAC) is dominated by the quantization noise of the DAC array [7] which is strongly related with its baseband sampling frequency and resolution. For example, the signal with a sampling rate of 320 MS/s is ~6 dB lower than the one with 80 MS/s [8]. The noise floor can be suppressed by increasing either of them but the high speed digital input/output (I/O) interface is challenging [9] and bulky. Also, the resolution is limited by the device matching [7]. For example, an effective number of bits (ENOB) of 6.9-bit was achieved with a resolution of 9 bits [3]. Rather than these, exploiting an on-chip interpolation for the baseband signal can relax the speed of the digital interface. In this work, the tradeoffs between the resolution, sampling frequency and linear interpolation is analyzed. They affect the noise and replica rejection. Section II presents the analysis the DAC noise with respect to its resolution and sampling rate. Section III introduces the linear interpolative I/Q DTX for suppressing sampling replicas and noise floor. Section IV shows the simulation results and the conclusion is drawn in Section V.

II. DAC Noise

The signal-to-noise ratio (SNR) of a DAC with respect to quantization noise can be formulated as

$$SNR = \frac{P_S}{\int_0^{\frac{f_S}{2}} P_{NF}(f)df}, \quad (1)$$

where P_S is the signal power in mW, $P_{NF}(f)$ is the noise power density in mW/Hz and f_s is the sampling frequency of the DAC. When the signal frequency is not a sub-harmonic of f_s, the quantization noise can be regarded as random and is flat in the frequency domain. Thus, (1) can be calculated as,

$$SNR(dB) = \frac{P_S}{P_{NF}(dB)} - 10logf_s + 3.01. \quad (2)$$

As the SNR of the DAC is related to the ENOB $SNR(dB) = 6.02N + 1.76$, the relative noise floor level P_{NF}/P_S in dBc/Hz can be derived as,

$$P_{NF}/P_S(dB) = -(6.02N + 10logf_s - 1.25), \quad (3)$$

where N is the ENOB of the DAC. The noise floor level can be suppressed by increasing either the ENOB of the DAC or the sampling frequency. Every 6-dB lower noise floor can be realized by adding 1-bit resolution, or quadrupling the sampling frequency, as shown in Fig. 1. Considering the I/O pin count, raising the resolution of the DAC is more favorable as we only have $(N + 1)$ bits for each channel to obtain a 6-dB lower noise floor. However, we have to increase f_s by 4×, or equivalently having $4N$ bits for each channel with the same f_s, for the same data throughput.

Comparing with a single DAC, the SNR and noise-floor level of an in-phase/quadrature (I/Q) $2 \times N$-bit DAC remain unchanged since the I- and Q-channel signals are orthogonal. The total power of signal and noise are the power sums of the individual channels. Besides, the quantization noise is also filtered by the zero-order hold (ZOH), but its response is frequency dependent and will be discussed in Section IV.

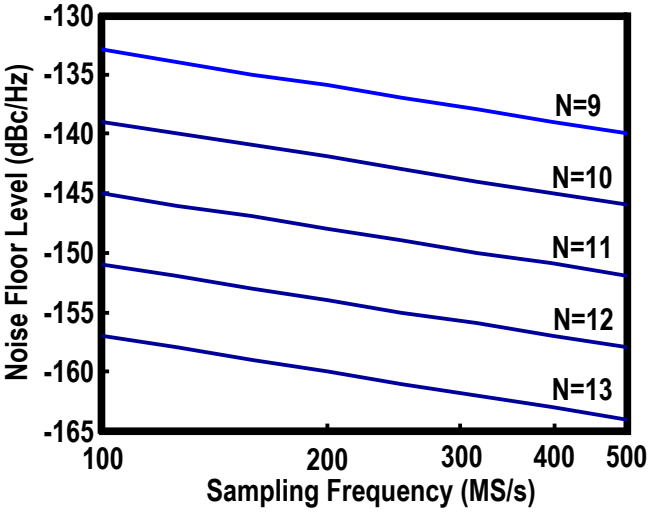

Fig. 1. Noise floor level versus sampling frequency over different ENOBs.

III. Interpolative I/Q DTX

A. Sampling Replicas Suppression

As the complex baseband signal $s(t)$ has a finite sampling frequency. The sampled signal $s_s(t)$ can be expressed as,

$$s_s(t) = s(t)\sum_{n=-\infty}^{\infty}\delta(t-nT_s), \tag{4}$$

which is the multiple of the signal and an infinite impulse train, where T_s is the sampling period. Since the Fourier transform of the impulse train is also an impulse train with a spacing of f_s, replicas of the fundamental signal occur at the multiples of f_s. As adding reconstruction filters is not trivial in DTX design, the replicas can only be filtered by ZOH response. A ZOH signal can be defined as $s_{ZOH}(t) = s_s(t) * h_1(t)$ where $*$ is the convolution operation and $h_1(t)$ which can be expressed as,

$$h_1(t) = \begin{cases} 1/T_s & |t| \le T_s/2 \\ 0 & otherwise \end{cases}. \tag{5}$$

The frequency response of $h_1(t)$ can be calculated as,

$$H_1(jf) = F\{h_1(t)\} = \int_{-\infty}^{\infty} h_1(t)e^{-j2\pi ft}dt = \frac{1}{\pi T_s f}\sin(\pi T_s f), \tag{6}$$

where $F\{.\}$ is the Fourier transform operation. Thus, the ZOH can provide a $sinc$ response for the replicas. Suppose the maximum frequency of the baseband signal is at $f_{BB,max}$, the replica with the least suppression is at $f_s - f_{BB,max}$. In order to have ≥40-dB rejection for the replicas, the over-sampling rate $OSR = f_s/BW$ should be ≥50 that is unacceptably high, where BW is the signal bandwidth which is 2× of $f_{BB,max}$ for a double sideband signal.

To suppress the replicas, a continuous linear interpolated signal $s_{LI}(t) = s_s(t) * h_{LI}(t)$ is a possible solution, where $h_{LI}(t) = h(t) * h(t)$. Thus, the continuous linear interpolation operation can achieve a $sinc^2$ rejection. Yet, a continuous linear interpolation requires infinite resolution and sampling frequency in the digital domain or bulky ramp generation circuits in the analog domain.

Here the linear interpolation function can be approximated as a staircase response. The staircase signal can be simply generated by full adders from the original binary data if the interpolation ratio is a power of two. Then, the resolution and the sampling frequency of the interpolated signal are increased accordingly. A linearly interpolated-by-2 response can be expressed as,

$$h_2(t) = \begin{cases} 1/T_s & |t| \le T_s/4 \\ 1/(2T_s) & T_s/4 < |t| \le 3T_s/4. \\ 0 & otherwise \end{cases} \tag{7}$$

The frequency response of $h_2(t)$ can be calculated as,

$$H_2(jf) = F\{h_2(t)\} = \frac{1}{\pi T_s f}\sin(\pi T_s f)\cos\left(\frac{\pi T_s f}{2}\right). \tag{8}$$

Comparing with the ZOH response, the linear linearly interpolated-by-2 response has additional zeros at the odd multiples of f_s. The required OSR is relaxed to 6.47 for achieving 40-dB replica rejection near f_s. However, the replica near $2f_s$ is not rejected by the addition zeros due to the interplated-by-2 operation. The required OSR is 25 for achieving 40-dB replica rejection in the vicinity of $2f_s$.

Generalizing it to be a 2^k-step response, the frequency response can be derived to be,

$$H_{2^k}(jf) = \frac{1}{\pi T_s f}\sin(\pi T_s f)\prod_{n=1}^{k}\cos\left(\frac{\pi T_s f}{2^n}\right). \tag{9}$$

Replicas up to $(2^k - 1)$-th harmonics can be rejected. The replicas rejection with different interpolation rates are compared in Fig. 2(a) to (d). To achieve 40-dB rejection for all sampling replicas, the required OSR for different linear interpolation rate is summarized in Table I. It shows that the OSR is limited by the non-suppressed replicas when the interpolation rate is up to 8. The OSR is halved for every 2× interpolation due to the $\frac{1}{f}$ rejection. Yet, the first replica is dominant for 16× interpolation because extra interpolation steps do not contribute to the first replica rejection. The optimal interpolation rate is 8/16 where the required OSR for achieving 40-dB replica rejection is 6.25/5.4. A 16× can further reduce the required OSR by 13.6% from the 8× one but the operating frequency for the 16× interpolation circuit will be almost 1.72× higher. For instance, the effective bandwidth of a 20-MHz IEEE 802.11g signal is 16.25 MHz. The minimum required f_s to achieve 40-dB replica rejection for 8×/16× interpolation is 101.6/87.75 MHz. Thus, choosing f_s to be 120/100 MHz for them can leave some margin for the rejection due to mismatches. The operating frequency of the interpolation

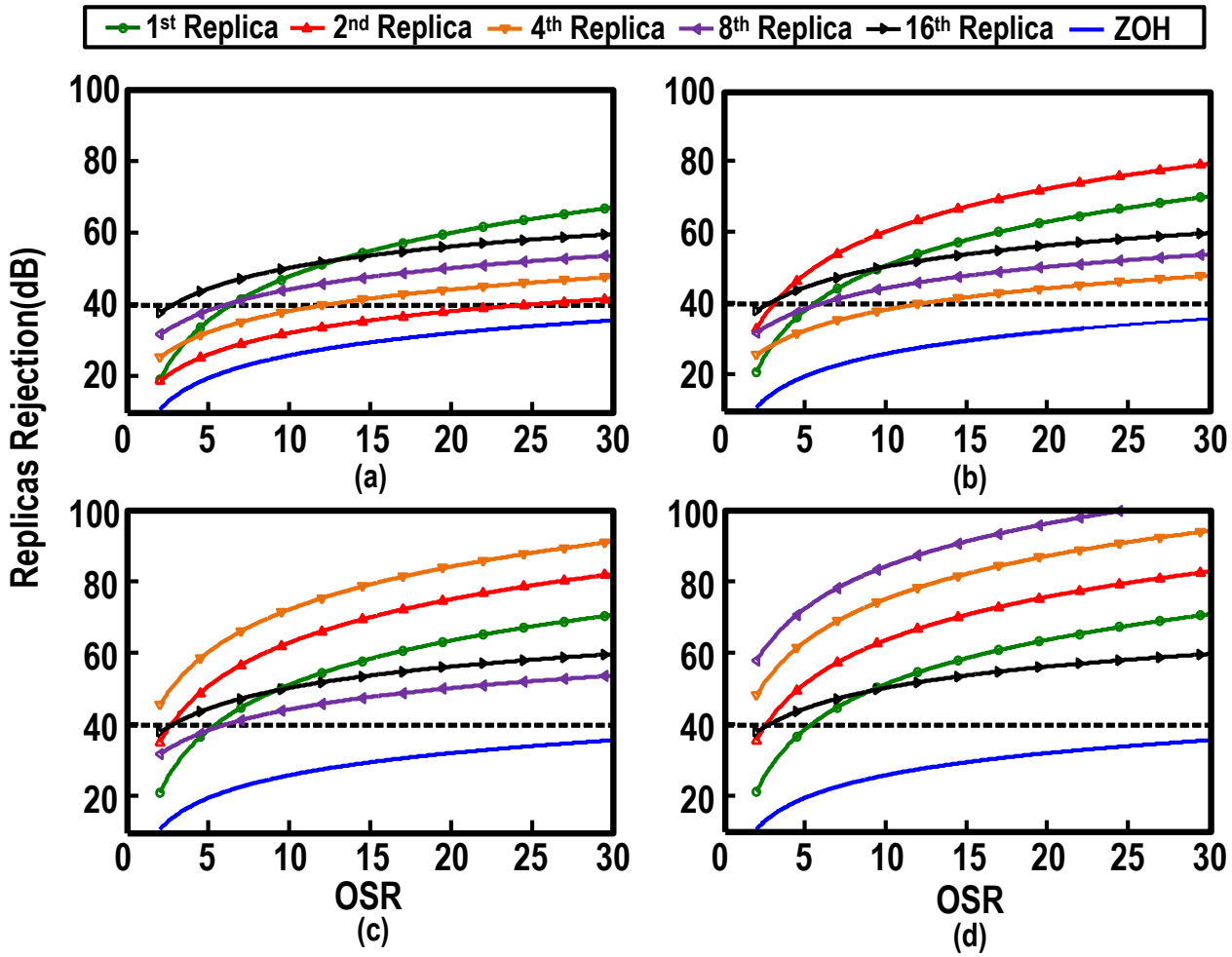

Fig. 2. Replicas rejection versus different OSR for, linearly interpolated (a) by-2, (b) by-4, (c) by-8, and (d) by-16, comparing with zero order hold.

TABLE I
REQUIRED OSR FOR ACHIEVING 40-DB REPLICA REJECTION AT DIFFERENT INTERPOLATION RATES.

Linear Interpolation Rate	1×	2×	4×	8×	16×
Required OSR	50	25	12.5	6.25	5.4
Dominant Replica	1st	2nd	4th	8th	1st

circuit will be 960MHz/1.6GHz, so implementing 16× interpolation can be much more power hungry. Also, a band-limited output matching network can possibly contribute to the eighth replica rejection which means the required OSR for the 8× interpolation can be further decreased.

B. Sampling Replicas Suppression

The quantization noise can be filtered by the interpolation responses while they are frequency dependent. The filtered power spectral density (PSD) of the quantization noise can be expressed as,

$$N_Q(f) = \left|H_{2^k}(jf)\right|^2 P_{NF} \tag{10}$$

The noise floor level is usually reported at a specific frequency offset from the carrier frequency in transmitter design. Rather than that, the average power gain within a certain bandwidth can be defined as,

$$R(2^k, f_a, f_b) = 10log\left(\frac{1}{f_b - f_a}\int_{f_a}^{f_b}\left|H_{2^k}(jf)\right|^2 df\right), \tag{11}$$

which is proportional to the total noise power. Certain values of $R(2^k, f_a, f_b)$ at different bands with different interpolation ratios are summarized in Table II. Without interpolation, the quantization noise is suppressed by 13.5 dB with the ZOH effect while it is suppressed by 26.5 dB with 8× interpolation. When the offset frequency is smaller than $13f_s/16$, the rejection is even lower but the noise is gradually dominated by the spectrum regrowth due to the nonlinearity of the circuit as the offset frequency decreases.

TABLE II
THE NOISE REJECTION ABILITY OF THE INTERPOLATION FUNCTIONS AT DIFFERENT BANDS.

f_a	$11f_s/16$	$13f_s/16$	$15f_s/16$	$17f_s/16$	$19f_s/16$	$21f_s/16$	$23f_s/16$	$25f_s/16$
f_b	$13f_s/16$	$15f_s/16$	$17f_s/16$	$19f_s/16$	$21f_s/16$	$23f_s/16$	$25f_s/16$	$27f_s/16$
$R(1, f_a, f_b)$	–10.3 dB	–16.7 dB	–28.9 dB	–19.2 dB	–14.9 dB	–13.5 dB	–13.5 dB	–14.9 dB
$R(2, f_a, f_b)$	–18.3 dB	–29.4 dB	–51.2 dB	–32.1 dB	–23.0 dB	–18.5 dB	–16.5 dB	–16.5 dB
$R(4, f_a, f_b)$	–19.8 dB	–31.4 dB	–54.2 dB	–36.3 dB	–28.3 dB	–25.1 dB	–24.9 dB	–27.2 dB
$R(8, f_a, f_b)$	–20.1 dB	–31.9 dB	–54.9 dB	–37.2 dB	–29.4 dB	–26.5 dB	–26.5 dB	–29.1 dB
$R(16, f_a, f_b)$	–20.2 dB	–32.0 dB	–55.1 dB	–37.5 dB	–29.7 dB	–26.8 dB	–26.9 dB	–29.5 dB

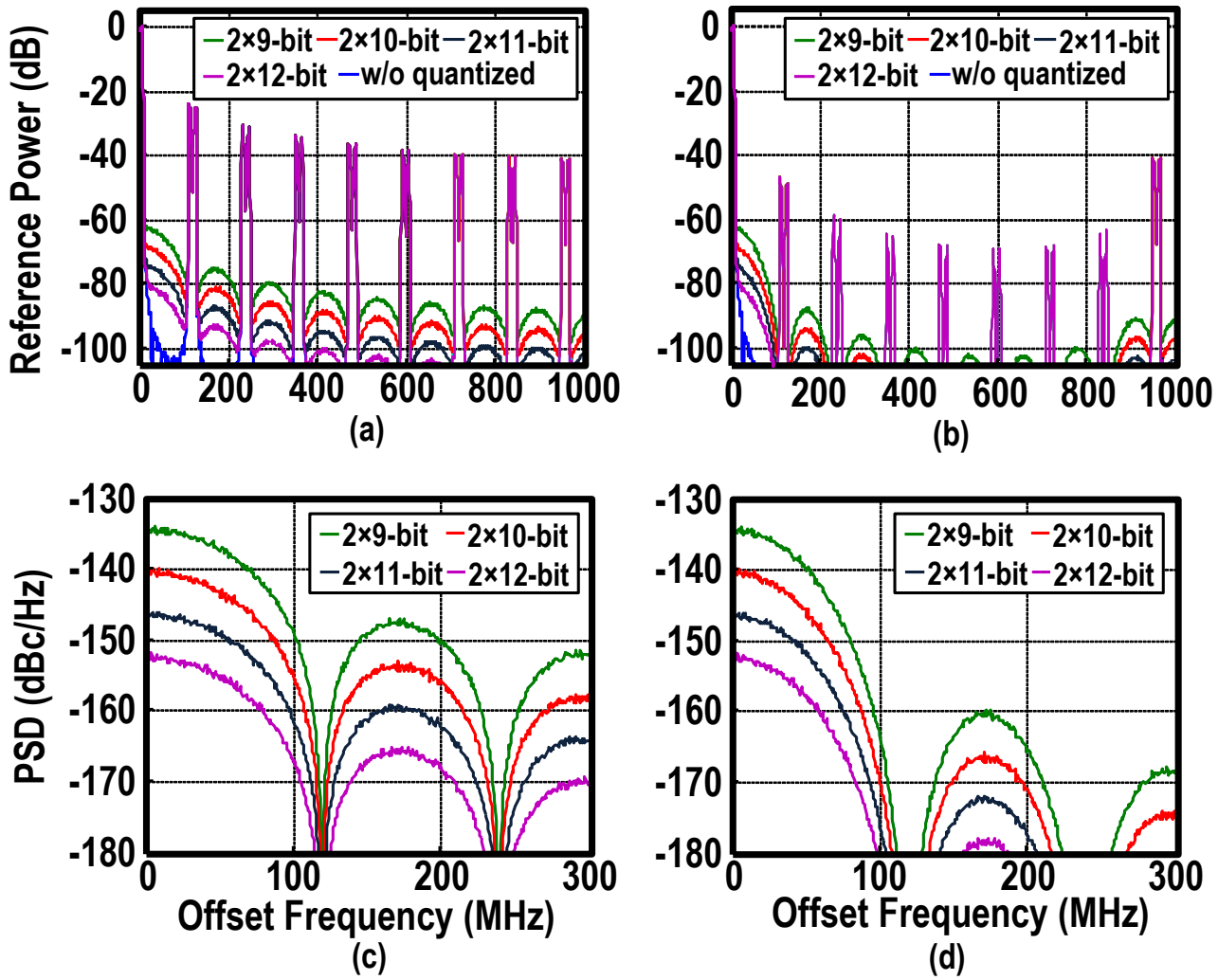

Fig. 3. The OFDM spectrum for, (a) without linear interpolation, (b) with 8× linear interpolation, and the PSD of the quantization noise for, (c) without linear interpolation, and (d) with 8× linear interpolation.

The 8× interpolation can provide 2.2 bits more than the ZOH effect. By combining the noise suppression from the filtering and the noise floor derived in Section II, the overall achievable noise floor can be calculated. Suppose the sampling frequency is chosen to be 120 MHz, without interpolation, a noise floor of –150/–160 dBc/Hz is achievable with 9.5/11.1-bit ENOB. However, a noise of –160 dBc/Hz is achievable with 9.0-bit ENOB with 8× interpolation.

IV. SIMULATION RESULTS AND DISCUSSION

An IEEE 802.11g orthogonal frequency division multiplexing

(OFDM) signal is generated to verify the derived results. The sampling frequency is chosen to be 120 MHz as explained.

The simulated OFDM spectrums and are plotted in Fig. 3(a) and (c). The first replica is suppressed to –24.4/–47.2 dBc without/with interpolation, respectively. The PSDs of the quantization noise are plotted in Fig. 3(b) and (d). The noise level at DC matches the theoretical values as derived in Section II. The noise floor of 2×9/2×10/2×11/2×12-bit ENOB is –147/–153/–159/–165 dBc/Hz all at 95 MHz offset without interpolation. The noise floor of 9-bit ENOB can be –160 dBc/Hz at 96 MHz offset with 8× interpolation. In practical measurement extra caution should be taken for generating the test signal as the noise floor can be easily overwhelmed by the spectrum leakage due to limited memory length.

Note that even the suppressed replicas are 20 to 40 dB higher than the noise floor. To further suppress the replicas, higher order interpolation or RF filtering is necessary. The former requires FIR filters operating up to 1 GHz to increase the sampling rate and resolution. However, the truncation effect will cause addition noise and DC error [10, 11]. The latter requires high-Q bandpass filter which is bulky and power inefficient. Otherwise, a higher sampling frequency has to be chosen.

V. Conclusion

The linear interpolation technique not only can suppress the replicas of the sampling in an RF DTX, but also can lower the quantization noise floor level. In this Brief, we have analyzed in details the tradeoff between the sampling frequency and resolution with the linear interpolation ratio. The results are backed by quantitative examples concerning the practical hardware limits at RF. It is revealed that linear interpolation can aid effectively sampling-frequency reduction without sacrificing the replica rejection. It can also relax the resolution of the baseband signal for smaller I/O pin count.

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References

[1] P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "An incremental-charge-based digital transmitter with built-in filtering," *IEEE J. of Solid-State Circuits*, vol. 50, no. 12, pp. 3065-3076, Dec. 2015.

[2] M. Ingels, D. Dermit, Y. Liu, H. Cappelle and J. Craninckx, "A 2×14bit digital transmitter with memoryless current unit cells and integrated AM/PM calibration," in *Proc. IEEE European Solid State Circuits Conf. (ESSCIRC)*, pp. 324-327, Sept. 2017.

[3] R. Bhat, and H. Krishnaswamy, "Design tradeoffs and predistortion of digital cartesian RF-power-DAC transmitters," *IEEE Trans. on Circuits and Syst. II: Exp. Briefs*, vol. 63, no. 11, pp. 1039-1043, Nov. 2016.

[4] S. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. of Solid-State Circuits*, vol. 46, no. 12, pp. 2977-2987, Dec. 2011.

[5] J. Walling, and D. Allstot, "Linearizing CMOS switching power amplifiers using supply regulators," *IEEE Trans. on Circuits and Syst. II: Exp. Briefs*, vol. 57, no. 7, pp. 497-501, Jul. 2010.

[6] W. Yu, X. Peng, P. Mak, and R. Martins, "A high-voltage-enabled class-D polar PA using interactive AM-AM modulation, dynamic matching, and power-gating for average PAE enhancement," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 64, no. 11, pp. 2844-2857, Nov. 2017.

[7] Z. Bai, A. Azam, D. Johnson, W. Yuan, and J. S. Walling, "Split-array, C-2C switched-capacitor power amplifiers," *IEEE J. of Solid-State Circuits*, vol. 53, no. 6, pp. 1666-1677, Jun. 2018.

[8] S. Yoo et al., "A Class-G switched-capacitor RF power amplifier," *IEEE J. of Solid-State Circuits*, vol. 48, no. 5, pp. 1212-1224, May 2013.

[9] S. Spiridon, et al., "A 375 mW multimode DAC-based transmitter with 2.2 GHz signal bandwidth and in-band IM3<-58 dBc in 40 nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 48, no. 7, pp. 1595-1604, Jul. 2013.

[10] P. Wong, "Quantization and roundoff noises in fixed-point FIR digital filters," *IEEE Trans. on Signal Processing*, vol. 39, no. 7, pp. 1552-1563, Jul. 1991.

[11] L. Koskinen, M. Kosunen, S. Lindfors, and K. Halonen, "Truncation DC-error elimination in FIR filters," in *Proc. IEEE Midwest Symp. on Circuits and Syst. (MWSCAS)*, pp. 1292-1295, Aug. 2000.