Three-Stage Load Modulated Power Amplifier With Efficiency Enhancement at Power Back-Off

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***Abstract*—This paper presents the analysis and design of a three-stage load modulated power amplifier (PA) in which, three amplifiers, each with different biasing, are connected to a four-port coupler. It is illustrated that, by properly configuring current relationships between the three amplifiers, this new load modulated PA can provide flexible output power back-off (OBO) and achieve high efficiency within a large OBO range. The detailed theoretical analysis and design methodology are given. In this architecture, the OBO level can be adjusted by simply setting bias conditions of the relevant amplifiers that correspond to the current relationships. Therefore, after circuit fabrication, the OBO range can still be reconfigured without redesigning the circuit. To validate the proposed approach, a prototype operating at 3.45 GHz is demonstrated and implemented with Gallium Nitride (GaN) transistors. The measured saturated output power reaches 45 dBm with 70.1% drain efficiency. At 6-/8-/10- dB OBO, the fabricated PA can provide up to 62.1%/53.8%/47.3% drain efficiency, respectively. When driven by a 60 MHz 9-dB PAPR long-term evolution (LTE) signal, the PA provides 34 dBm average output power with 44.3% average efficiency. Moreover, measurement results prove that the PA can offer efficiency enhancement when the OBO is reconfigured to 8-dB or 12-dB after fabrication.**

***Index Terms*—5G, GaN, load modulation, power amplifier, reconfigurable, three-stage.**

I. Introduction

TO meet the demand for high data rates and efficient usage of spectrum resources, modulated signals with high peak-to-average power ratio (PAPR) are widely adopted in modern wireless communication systems, which leads to stringent requirements for radio frequency (RF) power amplifiers (PAs) to have high efficiency at output power back-off (OBO).

Doherty power amplifier (DPA) is one of the most popular active load modulated PA architectures, that can provide high power efficiency at OBO. However, the conventional DPA is constrained by the fixed 6-dB OBO and it is intrinsically narrow band. The enhancement on bandwidth and OBO range of DPAs has been extensively studied [1]–[11]. Despite improvements are made, the enhanced efficiency cannot be maintained within the whole OBO range. Since only two peak efficiency points can be achieved in a two-stage DPA, a large efficiency drop is often observed in the middle of the OBO level, especially in the cases where a large power back-off is required. To solve this problem, the three-stage DPA adds one more peaking amplifier into the architecture to provide three peak efficiency points along the OBO range. The efficiency variations inside the back-off range can be holding steady in contrast to the two-stage DPAs, as demonstrated in [12]–[20]. However, the three-stage DPA is more complex with respect to the design of the load modulation network since it involves multiple segments of transmission lines.

Another PA architecture that received significant attentions recently is the load modulated balanced amplifier (LMBA). It has great potential in achieving both wide bandwidth and high efficiency performance[21]–[24]. By employing a coupler as the load modulation network, LMBA exhibits Doherty-like behavior to attain appreciably OBO ranging up to 12-dB, as reported in [25]–[27]. However, the existing LMBAs are still characterized by two peak efficiency points inside the available OBO.

In this paper, we propose an RF-input three-stage load modulated power amplifier to enhance back-off efficiency by exploring the capability of coupler in load modulation process. The proposed architecture includes three amplifiers connected to a coupler functioning as the load modulation network. Different from the LMBA, where two balanced amplifiers use the same bias, in this work, three amplifiers are biased in different modes. One of the amplifiers is biased in Class-B mode and the other two are biased in Class-C mode with different gate bias conditions. Three amplifiers turn on in sequence, similar to a three-stage Doherty. In the proposed architecture, the available OBO level and efficiency performance can be flexibly configured by changing the current relationships between the component amplifiers. The design parameters can be realized by adopting corresponding bias conditions during the circuit design. In contrast to LMBAs, the unbalanced configuration in the proposed architecture offers the efficiency flatness since there are more than two peak efficiency points within the large OBO range. Compared to the three-stage Doherty, the load modulation network is simple to implement, and once the coupler impedance is chosen, the same coupler is able to support different OBO levels. This gives the possibility of reconfiguring the back-off range even after circuit implementation, since the bias settings can be adjusted without modifying the circuit structure. The efficiency performance can still be guaranteed after being reconfigured.

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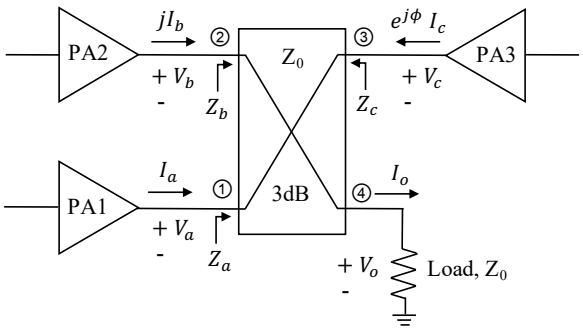


Fig. 1. Block diagram of the proposed PA architecture.

This characteristic offers more flexibility for accommodating various transmit signals in future wireless systems.

The rest of the paper is organized as follows: The configuration of the presented three-stage load modulated power amplifier is introduced in Section II. The load modulation principle and its behavior is also analyzed and explained in this section. The prototype PA is demonstrated in Section III with practical design concerns. The fabrication and measurement results of the proposed design is summarized in Section IV. The conclusion is made in Section V.

II. Theory of Three-stage Load Modulated Power Amplifier Operation

As illustrated in Fig. 1, the proposed three-stage load modulated power amplifier is composed of three PAs, where PA1 works in Class-B mode, PA2 is biased in Class-C mode and PA3 is also biased in Class-C mode but with a deeper bias condition. All the PAs are connected to a 3-dB coupler with port impedance Z_0 when fully matched. Three PAs turn on in sequence, leading to changes in port conditions. Consequently, the port impedance exposed to the working PAs at each stage will change accordingly. The peak efficiency is reached at the end of each stage, thus a high average efficiency performance within the large dynamic range can be achieved. The variation of the PA configurations generates more design freedoms. Therefore, it is necessary to study the impacts of the PA configurations, such as the current level, the turning on point and the phase relationship, in the load modulation process.

A. Load Modulation Principle

To facilitate the analysis, we consider all the PAs, shown in Fig. 1, as ideal voltage controlled current sources. The load modulation process at each stage can be analysed with the Z matrix of the coupler. The 3-dB coupler is a four-port current combiner, where the voltage and current relationship can be expressed as,

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & j & 0 & -j\sqrt{2} \\ j & 0 & -j\sqrt{2} & 0 \\ 0 & -j\sqrt{2} & 0 & j \\ -j\sqrt{2} & 0 & j & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \quad (1)$$

where V_i and I_i (i=1,2,3,4) denotes the voltage and current at each port, respectively. PA1 is connected to port 1 with current magnitude I_a. PA2 is connected to port 2 with current magnitude I_b and 90° phase difference from PA1. PA3 is connected to port 3 with current magnitude I_c and adjustable phase ϕ. The load with impedance Z_0 is connected to port 4. The current profile with normalized drive level k can be written as,

$$I_a = kI_{a,max}, 0 \le k \le 1, \quad (2)$$

$$I_b = \begin{cases} 0 & 0 \le k < k_1; \\ \frac{k-k_1}{1-k_1} I_{b,max} & k_1 \le k \le 1, \end{cases} \quad (3)$$

$$I_c = \begin{cases} 0 & 0 \le k < k_2; \\ \frac{k-k_2}{1-k_2} I_{c,max} & k_2 \le k \le 1. \end{cases} \quad (4)$$

Here we set the current ratio $\alpha = I_{b,max}/I_{a,max}$ and $\beta = I_{c,max}/I_{a,max}$ for convenience. k_1 and k_2 indicate the input drive level when PA2 and PA3 start turning on.

At stage one, since PA2 and PA3 are both off, the impedance at port 2 and 3 are infinite. At the load side, with the relationship given in (1), the output current can be written as,

$$I_o = -I_4 = -\frac{jZ_0(I_3 - \sqrt{2}I_1)}{Z_0} = j\sqrt{2}I_a. \quad (5)$$

PA1 operates at Class-B mode, the impedance at port 1 can be calculated as,

$$Z_{a,s1} = \frac{V_1}{I_1} = \frac{jZ_0(I_2 - \sqrt{2}I_4)}{I_1} = 2Z_0. \quad (6)$$

This value only relates to the impedance of the 3-dB coupler and remains unchanged with the drive level. The coupler is assumed to be lossless, thus the output power at the load equals to the sum of the output power of all the PAs connected. Therefore, at stage one, the output power can be expressed as,

$$P_{out,s1} = \frac{1}{2} I_a^2 Z_{a,s1}. \quad (7)$$

This expression can also be simplified as $P_{out,s1} = Z_0 I_a^2$ ($0 \le k < k_1$) after substituting (5). $V_{i,cc} (i = a, b, c)$ represents the drain supply voltage of each PA. The overall efficiency at this stage can be then calculated as,

$$\eta_{s1} = \frac{\pi}{4} \frac{2I_a^2 Z_o}{V_{a,cc} I_a} = \frac{\pi}{4} \frac{V_a}{V_{a,cc}}. \quad (8)$$

At stage two, with turning on of PA2, the impedance exposed to PA1 and PA2 are modulated with the increasing drive level. Similarly, it can be conducted with the matrix given in (1),

$$Z_{a,s2} = Z_0(2 - \frac{I_b}{I_a}), \quad (9)$$

$$Z_{b,s2} = Z_0 \frac{I_a}{I_b}. \quad (10)$$

With the increasing drive level, the impedance of PA1 decreases from $2Z_0$ and the impedance of PA2 decreases from infinite. The impedance value depends on the coupler impedance and the current level of the two PAs. Similarly, the output power at stage two can be expressed as,

$$P_{out,s2} = \frac{1}{2} I_a^2 Z_{a,s2} + \frac{1}{2} I_b^2 Z_{b,s2}. \quad (11)$$

At this stage, both impedances vary with the current level. To better evaluating how current levels affect the output power, a simplified expression can be obtained after substituting (9)(10), which is $P_{out,s2} = Z_0 I_a^2$ $(k_1 \leq k < k_2)$. As can be observed, the variation of $Z_{a,s2}$ and $Z_{a,s2}$ compensate the variation of I_b. This means the output power increases with the input power in a linear fashion. And the efficiency at stage two can be written as,

$$\eta_{s2} = \frac{\pi}{4} \frac{2I_a^2 Z_0}{V_{a,cc} I_a + V_{b,cc} I_b}. \tag{12}$$

At the final stage, with turning on of PA3, I_c starts to modulate the port impedance of PA1 and PA2. Different from the LMBA described in [21], the asymmetric current profile alters the load modulation behavior, so the impedance of port 1 and port 2 are not the same, which can be written as,

$$Z_{a,s3} = Z_0(2 - \frac{I_b}{I_a} - \frac{\sqrt{2}e^{j\phi} I_c}{I_a}), \tag{13}$$

$$Z_{b,s3} = Z_0(\frac{I_a}{I_b} - \frac{\sqrt{2}e^{j\phi} I_c}{I_b}). \tag{14}$$

Compared with the consistent decreasing impedance in the previous stage, the phase of PA3 determines the port impedance variation trend. From the equations above we can see that, when $\phi = 0$ which means PA1 and PA3 are in phase, $Z_{a,s3}$ and $Z_{b,s3}$ follow the decreasing order and stay at the real axis. When ϕ is inside [-90°, 90°], the impedances still decrease with the drive level but come with an imaginary part.

In the proposed architecture, $Z_{c,s3}$ is modulated due to the asymmetric current of I_a and I_b. The impedance at port 3 can be expressed as,

$$Z_{c,s3} = Z_0(1 - \sqrt{2}\frac{I_a - I_b}{e^{j\phi} I_c}). \tag{15}$$

At stage three, the output power can be calculated as the sum of the output power of all three PAs. Similarly, when substituting the impedance into the expression, we have,

$$P_{out,s3} = \frac{1}{2} Z_0[(\sqrt{2}I_a - I_c \cos\phi)^2 + (I_c \sin\phi)^2]. \tag{16}$$

As can be observed, the variation of $Z_{a,s3}$, $Z_{b,s3}$ and $Z_{c,s3}$ compensate the variation of I_b. Thus, the efficiency at this stage can be calculated as

$$\eta_{s3} = \frac{\pi}{4} \frac{[(\sqrt{2}I_a - I_c \cos\phi)^2 + (I_c \sin\phi)^2] Z_0}{V_{a,cc} I_a + V_{b,cc} I_b + V_{c,cc} I_c}. \tag{17}$$

The maximum output power is reached at the end of this stage. The port impedance at power saturation can be expressed as,

$$Z_{a,sat} = Z_0(2 - \alpha - \sqrt{2}e^{j\phi}\beta), \tag{18}$$

$$Z_{b,sat} = Z_0 \frac{1 - \sqrt{2}e^{j\phi}\beta}{\alpha}, \tag{19}$$

$$Z_{c,sat} = Z_0(1 - \sqrt{2}\frac{1 - \alpha}{e^{j\phi}\beta}). \tag{20}$$

It can be observed that the load modulation behavior is decided by the coupler port impedance and the current profile. With the increasing drive level, the status of port conditions changes the way how the current is combined, bringing a new stage of load modulation. The port impedance Z_a is gradually modulated from $2Z_0$ to $Z_{a,sat}$, and Z_b is modulated from infinite to $Z_{b,sat}$. This load modulation range is adjustable and can be customized based on practical design requirements.

B. Efficiency Performance Analysis

The efficiency performance within the OBO range is highly depended on the PA configurations. Based on the description from (8)(12)(17), the efficiency is affected by the design parameters $k_1, k_2, \alpha, \beta, \phi$, and can be expressed as $H(k_1, k_2, \alpha, \beta, \phi)$. The selection of parameters and its impact on the efficiency performance are discussed below.

Based on the load modulation analysis, the port impedances start to be modulated at stage two and stage three. The maximum power back-off level OBO_{k1} is defined as the power back-off point at the end of stage one under the drive level k_1. Similarly, another efficiency peak is expected at the end of stage two under the drive level k_2, the second power back-off point is defined as OBO_{k2}.

The maximum output power can be written as,

$$P_{out,max} = \frac{1}{2} I_{a,max}^2 [(\sqrt{2} - \beta\cos\phi)^2 + (\beta\sin\phi)^2] Z_0. \tag{21}$$

Thus, the power back-off at the drive level k_1 and k_2 can be calculated as,

$$OBO_{k_1} = \frac{2k_1^2}{(\sqrt{2} - \beta\cos\phi)^2 + (\beta\sin\phi)^2}, \tag{22}$$

$$OBO_{k_2} = \frac{2k_2^2}{(\sqrt{2} - \beta\cos\phi)^2 + (\beta\sin\phi)^2}. \tag{23}$$

From OBO_{k1} to saturation, the efficiency is expected to maintain high average level. It can be noticed that the DC supply voltage remains unclear, which is normally set as the maximum fundamental voltage value. Based on the matrix in (1), when the PA starts conducting, the port voltage will be modulated at the same time due to the changes in the port conditions. For PA1, the voltage at OBO_{k1} is $V_{a,k1} = 2k_1 I_{a,max} Z_0$, and the voltage at OBO_{k2} can be expressed as $V_{a,k2} = [2k_2 - \alpha(k_2 - k_1)/(1 - k_1)] I_{a,max} Z_0$. The condition imposed on PA1 for achieving the maximum efficiency throughout stage two is $V_{a,k1} = V_{a,k2}$, which can be simplified as,

$$\alpha = 2(1 - k_1)|_{V_{a,k1} = V_{a,k2}}. \tag{24}$$

Similarly, the voltage at power saturation can be written as $V_{a,sat} = (2 - \alpha - \sqrt{2}\beta e^{j\phi}) I_{a,max} Z_0$. The condition $V_{a,k2} = V_{a,sat}$ needs to be satisfied to obtain the maximum efficiency for PA1 at OBO_{k2} and saturation, which can be expressed as,

$$\alpha = (1 - k_1) \left. \sqrt{(2 - \frac{\sqrt{2}\beta\cos\phi}{1 - k_2})^2 + (\frac{\sqrt{2}\beta\sin\phi}{1 - k_2})^2} \right|_{V_{a,k2} = V_{a,sat}}. \tag{25}$$

Following the same logic, PA2 turns on at stage two. Its voltage at OBO_{k2} is $V_{b,k2} = k_2 I_{a,max} Z_0$, and will be

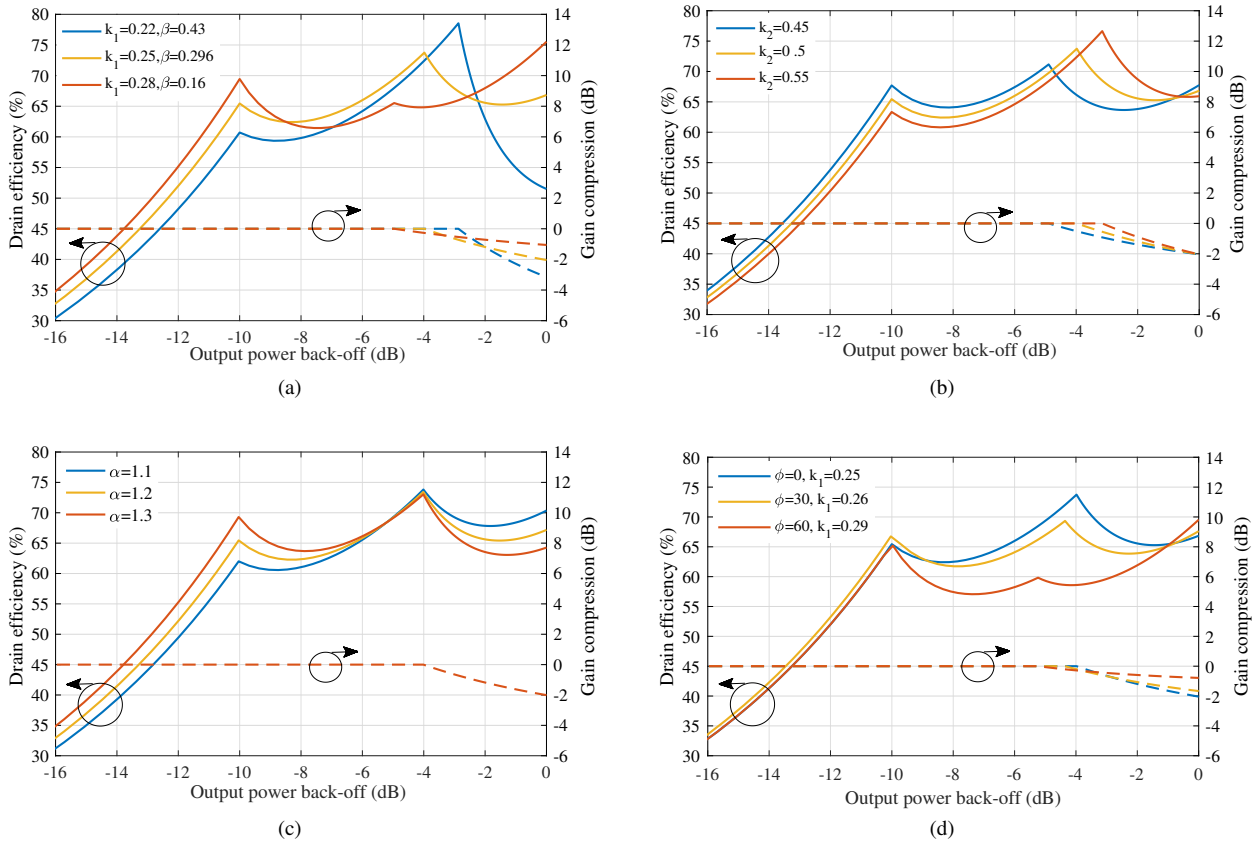


Fig. 2. The efficiency performance versus the output power back-off with varying parameters in the case of 10-dB OBO: (a) k_1 and β (k_2 = 0.5, α = 1.2, ϕ = 0), (b) k_2 (k_1 = 0.25, α = 1.2, β = 0.296, ϕ = 0), (c) α (k_1 = 0.25, k_2 = 0.5, β = 0.296, ϕ = 0) (d) ϕ (k_2 = 0.5, β = 0.296).

modulated to $V_{b,sat} = (1-\sqrt{2}\beta e^{j\phi})I_{a,max}Z_0$ when saturated. Thus, the condition applied to it for keeping high efficiency at OBO_{k2} and saturation is $V_{b,k2} = V_{b,sat}$, which can be conducted as,

$$k_2 = \sqrt{(1-\sqrt{2}\beta\cos\phi)^2 + (\sqrt{2}\beta\sin\phi)^2}\Big|_{V_{b,k2}=V_{b,sat}}. \quad (26)$$

The gain performance can be evaluated with those parameters in the efficiency function. Assuming the maximum input power is $P_{in,max}$, the input power at each stage can be expressed as $P_{in} = P_{in,max}k^2$. Thus, the gain at each stage can be calculated as,

$$G_{s1} = \frac{Z_0 I_a^2}{P_{in,max}k^2} = \frac{Z_0 I_{a,max}^2}{P_{in,max}} \quad (27)$$

$$G_{s2} = \frac{Z_0 I_a^2}{P_{in,max}k^2} = \frac{Z_0 I_{a,max}^2}{P_{in,max}} \quad (28)$$

$$G_{s3} = \frac{\frac{1}{2}Z_0[(\sqrt{2}I_a - I_c\cos\phi)^2 + (I_c\sin\phi)^2]}{P_{in,max}k^2} \quad (29)$$

As can be observed, the gain at stage one and stage two remains constant, while it starts decreasing after PA3 turns on. Instead of using the gain expression above, the gain compression is defined to present the normalized gain performance, which can be written as,

$$G_{comp} = \frac{(\sqrt{2}I_a - I_c\cos\phi)^2 + (I_c\sin\phi)^2}{2k^2 I_{a,max}^2} \quad (30)$$

And it is expressed in dB scale in the following analysis.

C. Design Parameters Selection

The efficiency performance within the OBO range can be customized via setting different design parameters. Let's take the 10-dB OBO as an example. ϕ is set to zero for the convenience of discussion. k_1 and β must comply with (22) after deciding OBO. $0 < k_1 < k_2$ needs to be ensured when selecting these two parameters. After deciding k_1 and β, as a starting point, k_2 can be estimated by using (26) considering the efficiency performance of PA2 at stage three. The value of α can be determined by using (24) and (25) after substituting k_1, k_2 and β. As analysed, (24) and (25) gives conditions for PA1 to obtain the maximum efficiency at stage two and stage three, respectively. Therefore, α shall be chosen inside the range suggested by (24) and (25), to obtain a more balanced efficiency performance for PA1. The parameters selection above is only based on considerations of the regional performance corresponding to specific parameters. When considering the overall efficiency performance, we do not have an analytic solution for it. Therefore, it is necessary to study the impact of each parameter and search for the optimal combinations of parameters under the given OBO.

The impact of each parameter on the efficiency function $H(k_1, k_2, \alpha, \beta, \phi)$ under 10-dB OBO is shown in Fig. 2. To better study them individually, we let one parameter vary while

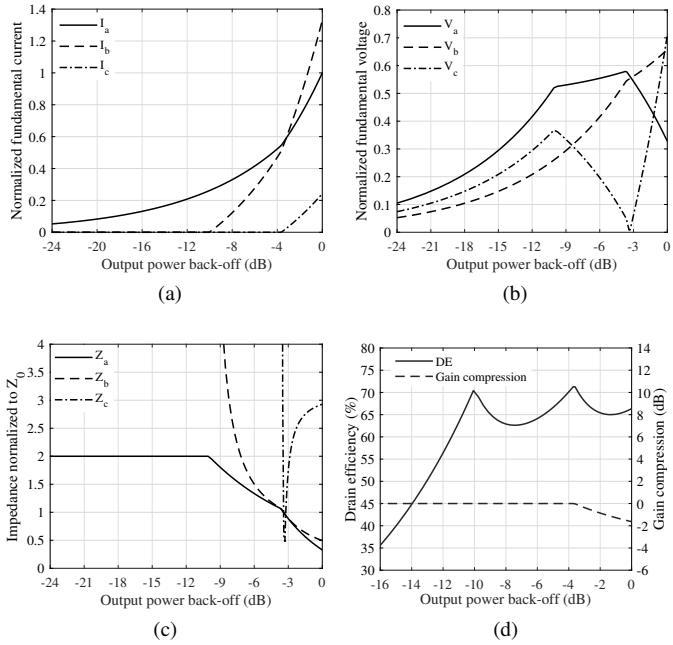


Fig. 3. The optimal efficiency function $H(0.262, 0.545, 1.33, 0.242, 0)$ in the case of 10-dB OBO with respect to (a) the current profile normalized to $I_{a,max}$, (b) the normalized voltage profile, (c) the load modulation trajectories, and (d) the drain efficiency performance.

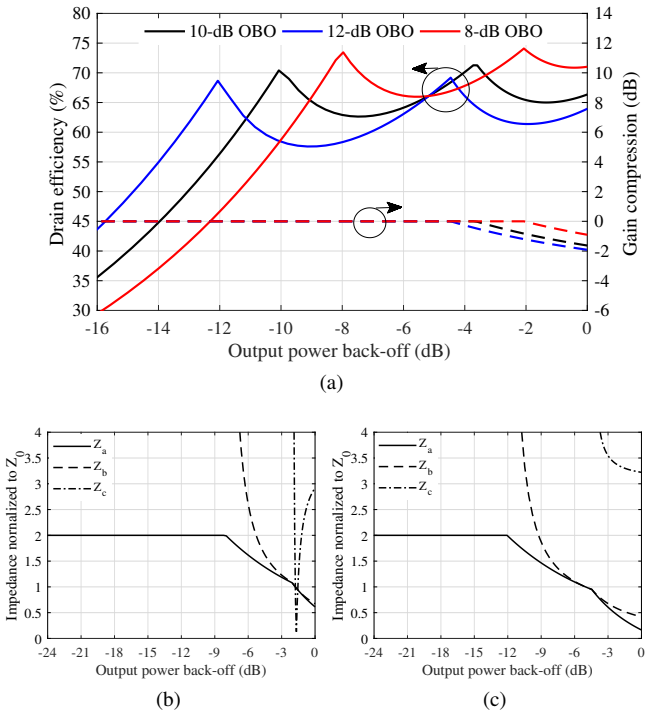


Fig. 4. (a) The efficiency performance of other back-off levels, (b) the load modulation trajectories for 8-dB OBO $H(0.358, 0.71, 1.19, 0.14, 0)$, and (c) the load modulation trajectories for 12-dB OBO $H(0.2, 0.48, 1.44, 0.28, 0)$.

others stay the same. In some cases, there are two varying parameters in order to maintain the desired OBO. Fig. 2(a) illustrates the efficiency with respect to k_1, β varying with k_1 to maintain the 10-dB OBO. By increasing k_1, the efficiency is improved at both OBO_{k1} and saturation, but drops a little at OBO_{k2}. And the gain compression is smaller with larger k_1 when saturated. Conversely, when k_2 is increasing towards $1-\sqrt{2}\beta$, the efficiency at OBO_{k2} increases significantly accompanied with larger OBO_{k2} value, but drops at OBO_{k1} and saturation, as shown in Fig. 2(b). Fig. 2(c) shows that the efficiency is enhanced at high OBO region with larger α, and the gain is not affected by the current level of I_b. Fig. 2(d) indicates the impact of the phase ϕ. k_1 changes with ϕ accordingly to keep the OBO defined by (22). The efficiency at OBO_{k2} is affected most. It drops with increasing ϕ while the gain compression becomes smaller. This impact mainly comes from the variation of k_1 when referring to Fig. 2(a). Therefore, the selection of parameters under a given OBO requires comprehensive considerations, and trade-offs shall be made for obtaining a more balanced efficiency performance.

In view of the impact of each parameter, the efficiency function $H(0.262, 0.545, 1.33, 0.242, 0)$ is considered to be a satisfied efficiency enhancement strategy for 10-dB OBO. The normalized current and voltage profile of the demonstrated case is shown in Fig. 3(a) and Fig. 3(b). The voltage is being modulated throughout the process, and its behavior varies with the current profile. The load modulation trajectories are shown in Fig. 3(c). Z_a is modulated from $2Z_0$ to $1.07Z_0$ at OBO_{k2} which is 3.59 dB, and continues to be modulated to $0.33Z_0$ at saturation. Z_b is modulated from infinite to $1.08Z_0$ at OBO_{k2}, and then modulated to $0.49Z_0$ when saturated. Z_c reaches $2.93Z_0$ when saturated. This large value is caused by the current level difference of PA1 and PA2. As illustrated in Fig. 3(d), three peak efficiency points at OBO_{k1}, OBO_{k2} and saturation are 70.4%, 71.3% and 66.3%, correspondingly. The minimum efficiency at stage two and three is 62.6% and 65%, respectively. When saturated, the gain compression is -1.63 dB. Although the peak efficiencies are not as high as that of the ideal Class-B, the overall efficiency cross the 10-dB OBO is enhanced.

The proposed approach can also be used to search for the optimal efficiency function at other OBO levels. Following the same procedure, the efficiency function $H(0.358, 0.71, 1.19, 0.14, 0)$ which gives the optimal performance at 8-dB OBO and the efficiency function $H(0.2, 0.48, 1.44, 0.28, 0)$ of 12-dB OBO are shown in Fig. 4. The OBO can be further extended by increasing the current level α and β, and shifting the turning on points k_1 and k_2 correspondingly. At the same time, the load modulation range is enlarged since the saturated impedances $Z_{a,sat}$ and $Z_{b,sat}$ are modulated to smaller values. The relatively high average efficiency can still be maintained.

Analysis above proves that, by taking advantage of the coupler structure, the proposed PA architecture can provide efficiency enhancement cross more than one OBO levels, with a relatively simple coupler based load modulation network. In this architecture, different OBOs are realized by adjusting the current level and turning on point of the transistors. When delivering different OBO levels, only the parameters in the efficiency function vary, while Z_0 is fixed. This means that the same load modulation network is able to provide

more OBO levels on condition that the current relationships change accordingly. This characteristic makes the OBO reconfiguration much more flexible and can be very useful in practice. For instance, the characteristics of transmit signals may change in real operation, it is not feasible to redesign the circuit to accommodate the OBO variation. But because of the new architecture, the power back-off level of the PA can be reconfigured by adjusting the bias settings without needs for changing the circuits. In comparison, the three-stage DPA requires more effort in designing the load modulation network and it can only serve for one fixed OBO level. The circuit must be redesigned once the desired OBO changes.

III. Design of Three-Stage Load Modulated Power Amplifier

In this section, we demonstrate the full design procedure by implementing a prototype PA operating with enhanced efficiency performance within the 10-dB OBO. GaN packaged transistors CGH40010F from Wolfspeed are adopted as the active devices. This prototype PA is implemented on the Taconic TLY-5 substrate with 2.2 dielectric constant and 30 mil thickness. The operation frequency is from 3.3 GHz to 3.6 GHz.

A. PA Design

The circuit block diagram of the three-stage load modulated proposed PA is shown in Fig. 5. The desired current of PA1 and PA2 are of a similar scale. The desired current of PA3 is smaller but $Z_{c,sat}$ is much larger than $Z_{a,sat}$ and $Z_{b,sat}$. The difference between the maximum fundamental voltage of the PAs is not significant. Therefore, all PAs employ the same transistor. The PAs are supposed to have the same input power level. Thus, a 3-dB coupler is adopted to split the input power between PA1 and PA2, and to provide the 90° phase difference. The input power divider with the power split ratio of 2:1 is adopted, and a phase adjusting transmission line is added after it. k_1 and k_2 are realized by adjusting the gate bias of each PA.

The load modulation process is fulfilled by the coupler with the impedance Z_0. In practice, the coupler cannot reach the current generator plane directly due to package and parasitic of the transistors. To ensure the port condition is satisfied, the phase shift of the output matching network together with the parasitic network should be equivalent to that of a 180° transmission line. At the output port, an impedance transforming network (ITN) is required to convert Z_0 to the system load.

As analysed in Section II, the efficiency function $H(0.262, 0.545, 1.33, 0.242, 0)$ is considered to be a satisfied solution. The varying current levels can be realized by adjusting the drain supply voltage. However, as shown in the analysis part, the drain supply voltage must be chosen based on the maximum fundamental voltage to guarantee the efficiency performance. In this way, the calculated drain supply voltage cannot provide enough current. To minimise the impact, the efficiency function is modified to $H(0.26, 0.48, 1.2, 0.25, 0)$. α is adjusted to a lower level, while β is slightly larger.

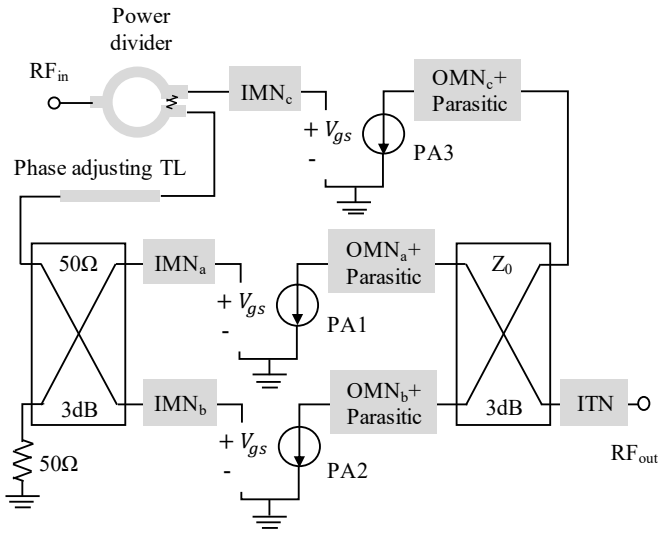


Fig. 5. Block Diagram of the proposed three-stage load modulated power amplifier.

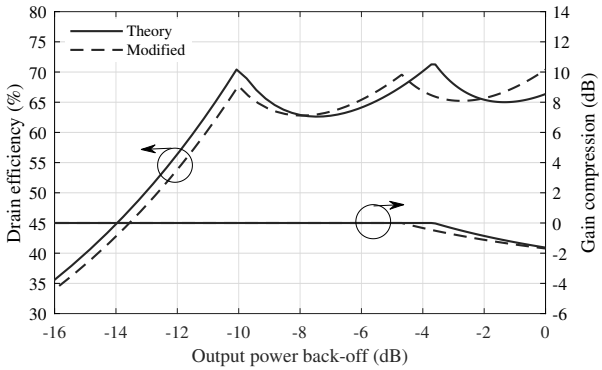
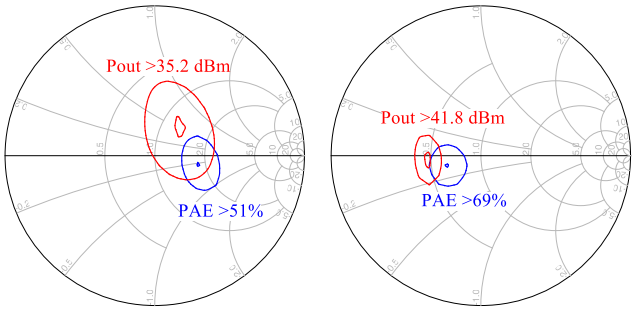


Fig. 6. The modified efficiency function $H(0.26, 0.48, 1.2, 0.25, 0)$ in comparison to the original theoretical one.



(a) (b)

Fig. 7. Simulated PAE contours and output power contours at 3.45 GHz for PA1 at (a) 10-dB OBO and (b) power saturation.

The comparison of the modified efficiency function with the theoretical one is presented in Fig. 6. The efficiency at OBO_{k1} drops a little but the efficiency at saturation increases. The high efficiency within the designed OBO is still maintained.

PA1 works in Class-B mode and its bias voltage is set as $V_{g,a}$ = -3 V and $V_{d,a}$ = 28 V. Under this bias, the

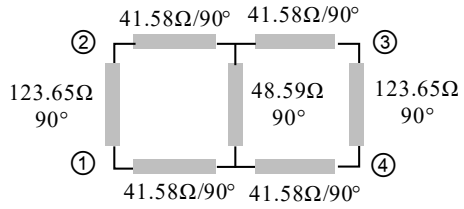
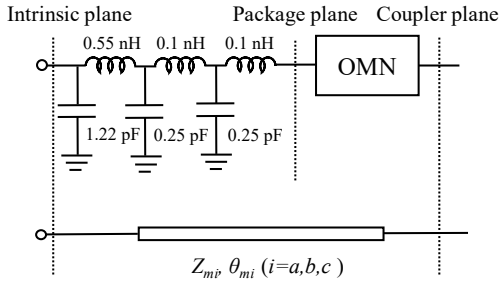


Fig. 8. The two-section branch line 3-dB coupler used in the proposed design.

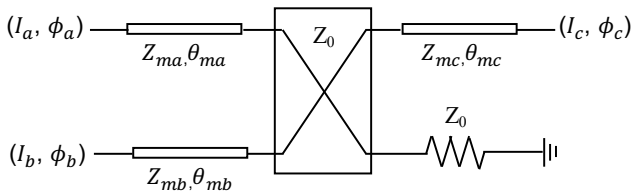
optimal impedance is estimated around R_{opt} = 30 Ω and it provides around 1 A fundamental current at saturation. Under the modified efficiency function, the fundamental voltage of PA1 is modulated from its maximum value at OBO_{k2} to a relatively lower value at saturation. The saturated impedance can be estimated as $Z_{a,sat} = R_{opt}V_{a,s2}/V_{a,sat}$. Based on (18), we have $Z_{a,sat}$ = 0.44 Z_0. The port impedance of the coupler can be then conducted as Z_0 = 50.5 Ω. Therefore, the 3-dB coupler with 50 Ω port impedance is adopted during the implementation. In this way, the input and the output can share the same coupler design, and the load can be directly connected to the coupler at the RF output without extra matching network. The drain supply voltage of PA2 can be obtained by applying the scaling factor α. Taking the knee voltage into consideration, we have $V_{d,b} = \alpha(V_{d,a} - V_{knee}) + V_{knee}$ = 32.8 V when assuming V_{knee} = 4 V. Nevertheless, the maximum fundamental voltage for PA2 is achieved at saturation, and can be estimated as $V_{d,b} = (V_{d,a} - V_{knee})V_{b,sat}/V_{a,k2} + V_{knee}$ = 31.3 V. Therefore, $V_{d,b}$ is set to 32 V as a compromise. When estimating the drain supply voltage of PA3, besides the current level β, its saturated impedance $Z_{c,sat}$ also requires consideration. The drain supply voltage can be estimated as $V_{d,c} = \beta(V_{d,a} - V_{knee})Z_{c,sat}/R_{opt} + V_{knee}$ = 25.3 V. In this implementation, $V_{d,c}$ is chosen as 25 V. The maximum output power can be calculated as 45.3 dBm from (21). PA2 is expected to turn on at OBO_{k1} = -10 dB which corresponds to 35.3 dBm output power. Likewise, PA3 is expected to turn on at OBO_{k2} = -4.86 dB which corresponds to 40.44 dBm output power. The gate bias of PA2 and PA3 is tuned to $V_{g,b}$ = -6 V and $V_{g,c}$ = -8.5 V to guarantee the right turning on point. At the centre frequency 3.45 GHz, the power added efficiency (PAE) contours and output power contours of PA1 observed at the intrinsic plane are illustrated in Fig. 7. At stage one, the impedance Z_a sticks to $2Z_0$=100 Ω, which falls in the high efficiency region of the contours. Then, Z_a is modulated to $1.28Z_0$ = 64 Ω at OBO_{k2}, and reaches $0.44Z_0$ = 22 Ω at saturation. For PA2, the impedance Z_b is modulated from the infinite to $1.34Z_0$ = 67 Ω at OBO_{k2}, and then to $0.54Z_0$ = 27 Ω when saturated. For PA3, the impedance Z_c is directly modulated to the saturated impedance $2.13Z_0$ = 106.5 Ω.

The input power allocation between PAs is achieved with the uneven Wilkinson power divider. However, the width of the transmission lines adopted in the power divider corresponding to 2:1 power split ratio is too narrow to fabricate. Due to this limit, the maximum power split ratio can be achieved is 1.8:1 in this implementation. The power distributed to the two ports are P_2 and P_3 respectively, P_2 delivers the power to the 3-dB coupler and P_2 delivers the power to PA3. Thus, the power division ratio $R = P_2/P_3$ is set as 5.1 dB.

The 3-dB coupler used in this design is the branch-line



(a)



(b)

Fig. 9. (a) Transistor's parasitic and the output matching network. (b) The equivalent output combiner structure adopting two-section branch-line coupler.

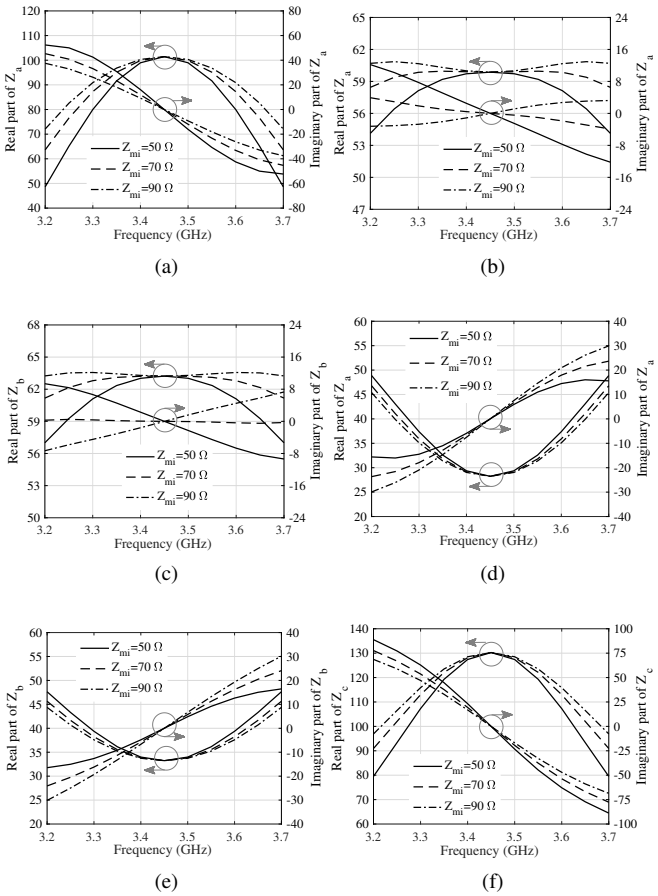


Fig. 10. The simulated port impedances at the end of each stage with sweeping Z_{mi} : (a)Z_a at OBO_{k1}, (b) Z_a at OBO_{k2}, (c) Z_b at OBO_{k2}, (d) Z_a at saturation, (e) Z_a at saturation, (f) Z_c at saturation.

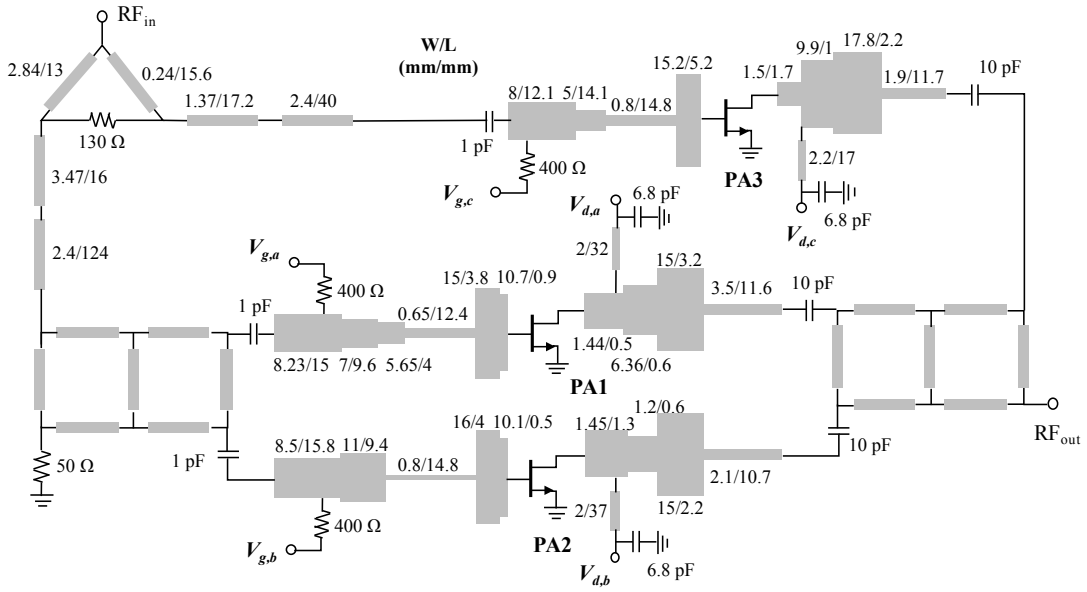


Fig. 11. Circuit schematic of the proposed three-stage load modulated power amplifier.

coupler. The conventional branch-line coupler has one section and is intrinsically narrow band. To broaden the bandwidth, the two-section branch-line coupler with port impedance Z_0 = 50 Ω is adopted, as shown in Fig. 8. Since one more section is added, to maintain the phase relationship, port 2 will be connected to PA1 and port 1 will be connected to PA2. The connection of PA3 remains unchanged.

The output matching network and the parasitic are assumed to be equivalent to one segment transmission line as show in Fig. 9(a). The extracted parasitic and package parameters of the transistor are concluded from [28]. For instance, the passive networks between the intrinsic plane and the coupler plane of PA1 is equivalent to a transmission line with characteristic impedance $Z_{m,a}$ and electrical length $\theta_{m,a}$ = 180°, connecting the coupler and the current source. Therefore, the whole output combiner can be regarded as a 3-dB coupler with three transmission lines connected at port 1, 2 and 3, as presented in Fig. 9(b).

The port impedances at the end of each stage is depicted in Fig. 10. The impact of the characteristic impedance of the equivalent matching network is also presented, and it is assumed Z_{ma}, Z_{mb} and Z_{mc} changes simultaneously and are represented by Z_{mi} for analysis convenience. The phase of each current source inside the frequency band can be expressed as $\phi_i f/f_c$, where f_c represents the centre frequency. In general, a relatively large Z_{mi} is desired in view of the fractional bandwidth at each stage. When considering Z_{ma}, Z_{mb} and Z_{mc} individually, the discussion results still apply. Another practical concern is that the matching network with high Z_{mi} value is not easy to implement, which would restrict the bandwidth performance. Therefore, the preferred impedance of Z_{mi} is around 70 Ω, small variation of Z_{mi} is also acceptable.

Based on the above analysis, the schematic of the proposed three-stage load modulated power amplifier is shown in Fig. 11. The input matching networks are designed according to the simulated load-pull results, and phase adjusting transmission lines are added after the uneven power divider to obtain required phase relationships between PAs.

B. Simulation Results

The simulation results presented are from electromagnetic simulation. The size of the transmission lines are reasonably tuned to achieve desired efficiency enhancement. The simulated fundamental current profile, voltage profile and the load modulation trajectories are shown in Fig. 12. Both of the simulated current ratio α and β meet the expectations in the efficiency function. The voltage profile and the load modulation trajectories fit the behaviors analyzed in the theory.

Fig. 13 presents the simulated drain efficiency and gain performance versus the output power. The maximum output power is 46.2 dBm at 3.4 GHz with 9.2 dB gain, where the peak efficiency reaches 73.08%. Fig. 14 shows the drain efficiency and the saturated power within the designed bandwidth. At the power saturation, the drain efficiency ranges from 69.09% to 73.08%. At 6-dB and 8-dB OBO, the drain efficiency is in the range of 60.7%-70.5% and 56.33%-64.9% respectively. At the designed 10-dB OBO, the efficiency still keeps above 43.6% and reaches as high as 55.1%. As expected, the simulation results valid the proposed three-stage load modulated power amplifier architecture for the average efficiency performance.

C. Reconfigurability of Power Back-off

To demonstrate the reconfigurability, the OBO level of the designed PA is reconfigured to 8 dB and 12 dB, respectively. Like the practical concerns we had in the 10-dB OBO case, the efficiency functions are adjusted for better efficiency performance. The modified efficiency function of 12-dB OBO

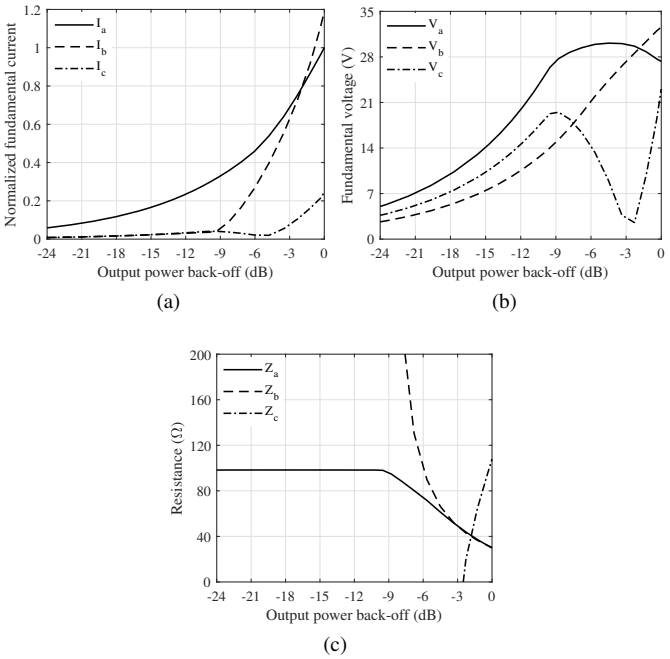


Fig. 12. Simulated (a) normalized fundamental current (b) fundamental voltage and (c) load modulation trajectories versus output power back-off at 3.5 GHz of the implemented 10-dB OBO case.

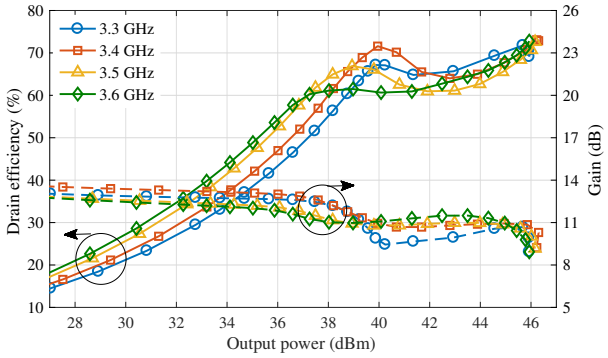


Fig. 13. Simulated drain efficiency and gain versus output power from 3.3 GHz to 3.6 GHz.

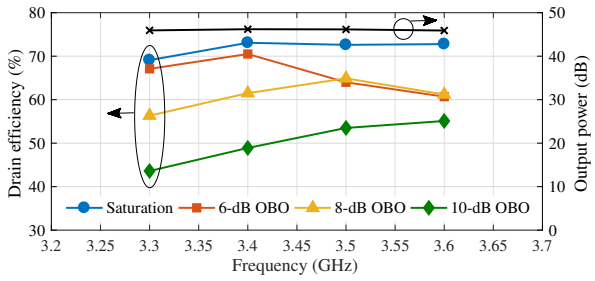


Fig. 14. Simulated drain efficiency and saturated output power inside operating frequency band.

is $H(0.203, 0.47, 1.35, 0.27, 0)$. To extend the OBO to 12 dB, the drain supply voltage of PA1 is tuned to a lower value to achieve the required α and β. Because of it, the maximum fundamental current of PA1 decreases, leading to the drop in the maximum output power. Therefore, its drain supply voltage needs to be chosen carefully to minimize the output power variation and to achieve larger current ratio at the same time. $V_{d,a}$ is then adjusted to 23 V, and the estimation of $V_{d,b}$ and $V_{d,c}$ can be obtained in the same way as the 10-dB OBO case, which is $V_{d,b}$ = 29.7 V, $V_{d,c}$ = 30.8 V. The gate bias of PA2 and PA3 is then adjusted to shallower point to guarantee the right turning on. As for the 8-dB OBO, the corresponding efficiency function is modified to $H(0.34, 0.6, 1.17, 0.2, 0)$. Since smaller current ratio is required, the drain supply voltage of PA1 is adjusted to a higher level, which is $V_{d,a}$ = 32 V. Similarly, the drain supply voltage $V_{d,b}$ and $V_{d,c}$ are estimated as $V_{d,b}$ = 36.7 V, $V_{d,c}$ = 22.7 V. Deeper gate bias of PA2 and PA3 is required. For better efficiency performance, the bias settings for different back-off levels are optimized based on the estimation made, and are summarized in Table I.

TABLE I
BIAS SETTINGS FOR RECONFIGURED OBO

	$V_{g,a}$,$V_{d,a}$	$V_{g,b}$,$V_{d,b}$	$V_{g,c}$,$V_{d,c}$
10-dB OBO	-3V, 28V	-6V, 32V	-8.5V, 25V
12-dB OBO	-3V, 23V	-5.3V, 33V	-8.3V, 29V
8-dB OBO	-3V, 32V	-6.2V, 36V	-9.2V, 23V

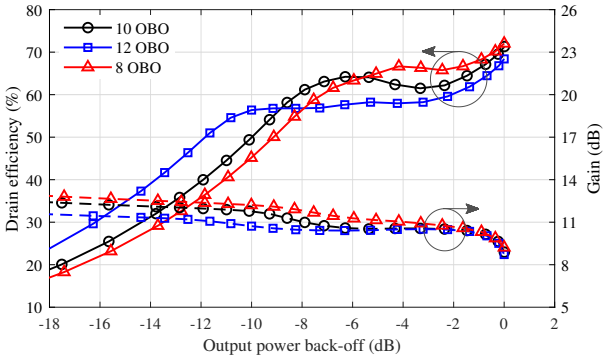


Fig. 15. Simulated drain efficiency and gain performance versus output power back-off with reconfigured 8-dB and 12-dB OBO at 3.5 GHz.

The simulated PA performance with reconfigured OBO is depicted in Fig. 15. To better present the reconfigured results, the drain efficiency and gain versus output power back-off at one single frequency inside the bandwidth is illustrated. The reconfigured 12-dB OBO case has less saturated power of 45.6 dBm compared to 45.9 dBm in the 10-dB OBO case, which is not significant. The overall gain is reduced by 0.86 dB. The drain efficiency at 12-/10-/8-/6-dB back-off level and power saturation are 50%/56.4%/56.8%/58% and 68.4%, respectively. As for the 8-dB OBO case, the saturated power reaches 46.2 dBm with 0.47 dB increase in the small signal gain. The average efficiency within the OBO range is higher than the 10-dB OBO case. At 8-/6-dB OBO and at saturation, the efficiency is 55%/63.4% and 72% respectively. The simulated fundamental current profile, voltage profile and load modulation trajectories of both cases are shown in Fig. 16. Despite the fact that the PA is not optimized at the

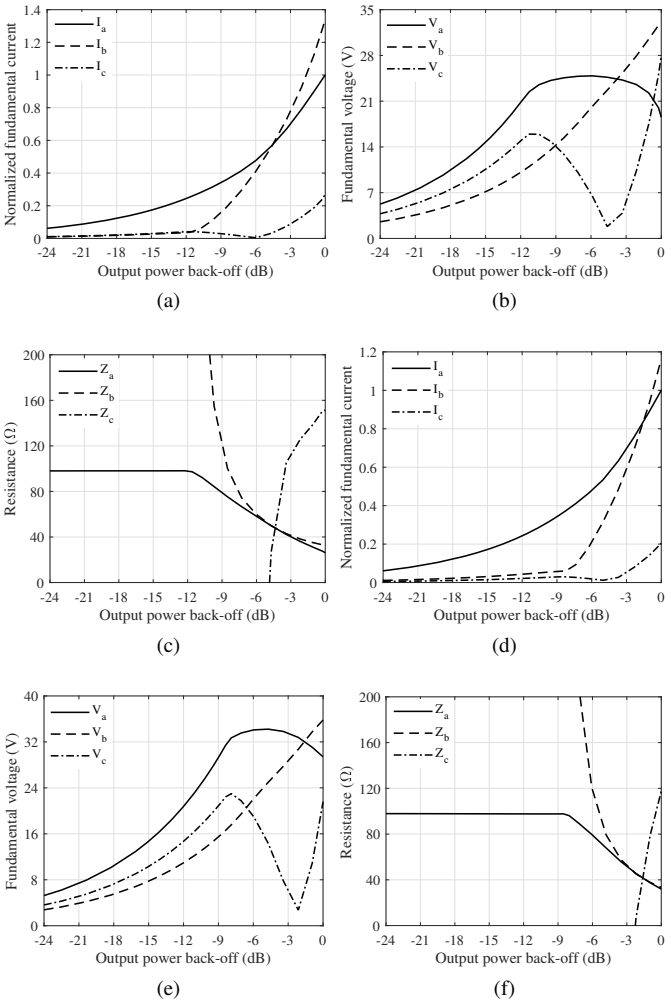


Fig. 16. Simulated (a) normalized fundamental current (b) fundamental voltage and (c) load modulation trajectories of the 12-dB OBO, and (d) normalized fundamental current (e) fundamental voltage and (f) load modulation trajectories of the 8-dB OBO versus output power back-off, respectively.

reconfigured OBO, the proposed architecture still provides satisfied efficiency enhancement within the reconfigured power back-off levels.

IV. Experimental Results

The fabricated power amplifier is shown in Fig. 17, and the size of the circuit is 200 mm×125 mm. The PA is mounted on the aluminium heat sink, and connected to the test bench through SMA connectors at both the RF input and output ports. The signal is generated from the vector signal generator, and the input signal is boosted by a driver power amplifier before entering the RF input port. The output signal is captured and measured with a signal spectrum analyzer. Several dc power supplies are adopted to accommodate the needs for different bias of each PA. The fabricated PA is tested with continuous wave (CW) and modulated signals separately.

A. CW Measurement

The continuous wave measurement is carried out with CW power sweep inside the operating frequency band from 3.3 to

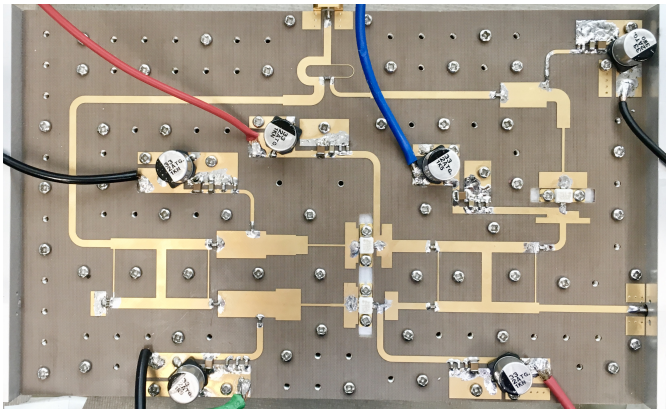


Fig. 17. Photograph of the fabricated PA.

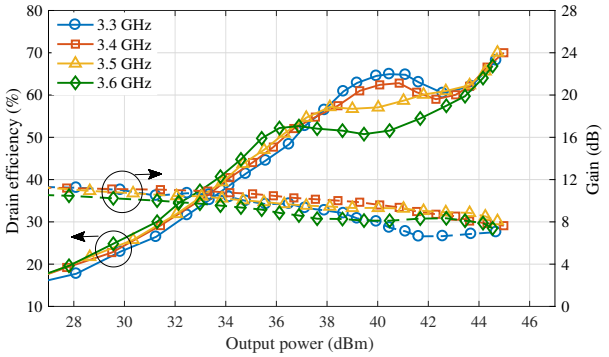


Fig. 18. Measured drain efficiency and gain versus output power from 3.3 GHz to 3.6 GHz.

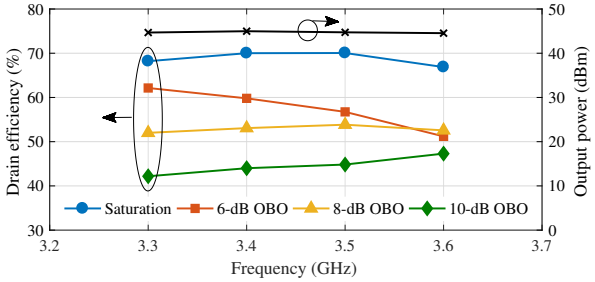


Fig. 19. Measured drain efficiency and saturated output power inside operating frequency band.

3.6 GHz. Fig. 18 shows the measured drain efficiency and gain performance versus the output power. The small signal gain is 10.6 dB to 11.4 dB across the bandwidth. The measured maximum output power is 45 dBm at 3.4 GHz, where the drain efficiency is 70% respectively. At the power saturation, the drain efficiency is all above 66.9% inside the bandwidth. Fig. 19 gives more detailed efficiency performance versus the frequency at different power back-off levels. At the 6-dB OBO, the efficiency ranges from 51.2% to 62.1%, while at the 8-dB OBO, the efficiency is in the range of 52% to 53.8%. The designed highest OBO is 10-dB, at this power level, 47.3% drain efficiency is reached, and at least 42.2% is obtained inside the bandwidth. Since the measured output power is a little bit less than that in simulation, the average efficiency

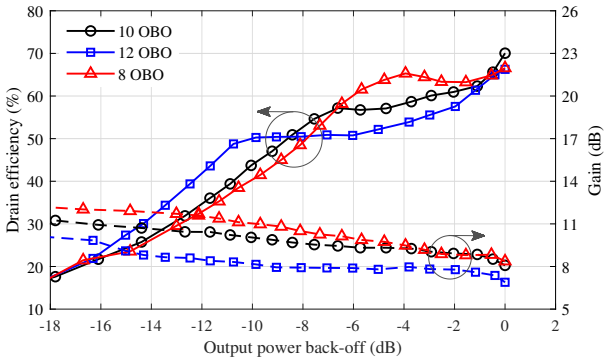


Fig. 20. Measured drain efficiency and gain performance versus output power back-off with reconfigured 8-dB and 12-dB OBO at 3.5 GHz.

performance is not as good as the simulation. Even though, the drain efficiency still maintains at a relatively high range with different back-off levels.

The measured drain efficiency and gain performance with reconfigured back-off level is presented in Fig. 20. The bias is adjusted in each case based on Table I. At 3.5 GHz, the measured saturated power for 12-dB OBO case is 44.5 dBm where the efficiency reaches 66.3%. The small signal gain decreases to 10.3 dB. The efficiency still achieves 42% at 12-dB OBO. At 10-/8-/6-dB back-off level, the efficiency is 50.3%/50.5%/52.8% respectively. In the case of 8-dB OBO, the measured saturated power is 45.1 dBm, and the average efficiency within the OBO region is higher than that in the 10-dB OBO case. The small signal gain is slightly higher and reaches 12.2 dB. At 8-/6-dB back-off level and saturation, the efficiency is 49.2%/61.5% and 66.6% respectively. The measured results prove that this fabricated PA is able to provide enhanced efficiency performance under more than one power back-off levels.

B. Modulated Signal Measurement

To evaluate the linearity and efficiency performance of the proposed PA under modulated signal stimulation, a 20 MHz and a 60 MHz OFDM signals with 7 to 9 dB PAPR are used to test the proposed PA at 3.45 GHz. Digital predisortion (DPD) is conducted to linearize the implemented PA.

Fig. 21 shows the measured output spectrum under signals with different bandwidth and PAPR settings. With 20 MHz signals, the measured adjacent channel leakage ratio (ACLR) is -25 dBc, -25.7 dBc and -27 dBc without DPD, and is improved to -55.1 dBc, -56.9 dBc and -57.7 dBc after performing DPD with 7-/8-/9-dB PAPR signals, respectively. The average efficiency reaches 51.9% /47.9%/46% in the three cases, and the respective output powers are 35.8 dBm, 34.9 dBm and 34.4 dBm.

With 60 MHz signals, the measured ACLR is 22.1/-24.8/-28.6 dBc for 7-/8-/9-dB PAPR signals, respectively, before implementing DPD. With DPD, ACLR is improved to -48.4 dBc with 34.7 dBm output power for 7 dB PAPR signals, -51.0 dBc with 34.5 dBm output power for 8 dB PAPR signals and -50.8 dBc with 34.0 dBm output power for 9-dB PAPR

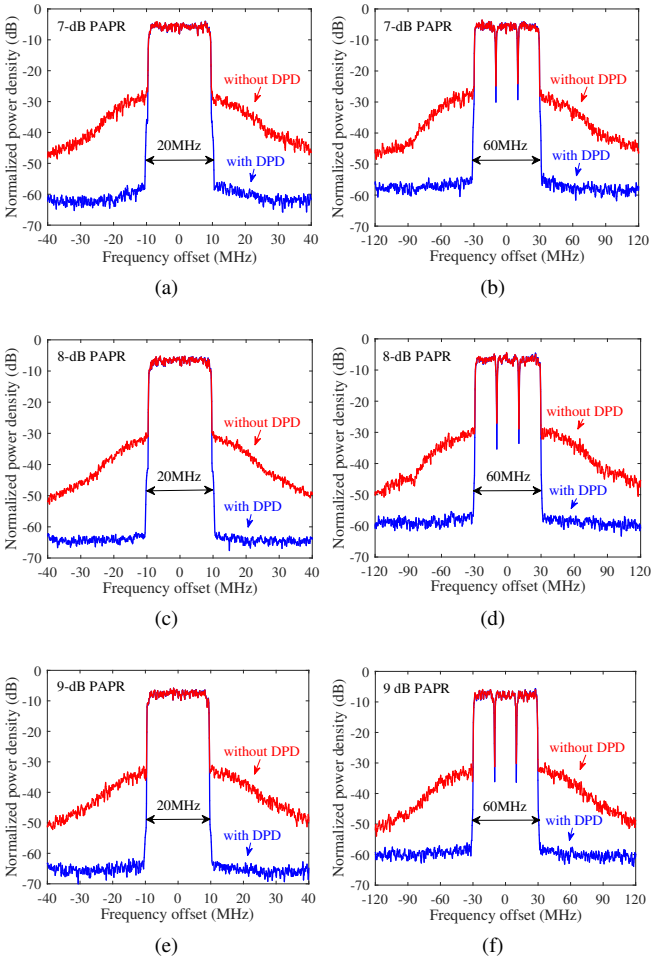


Fig. 21. Spectra plots at 3.45 GHz with (a) 20 MHz 7-dB PAPR (b) 60 MHz 8-PAPR (c) 20 MHz 8-dB PAPR (d) 60 MHz 8-dB PAPR (e) 20 MHz 9-dB PAPR (f) 60 MHz 9-dB PAPR signals with and without DPD.

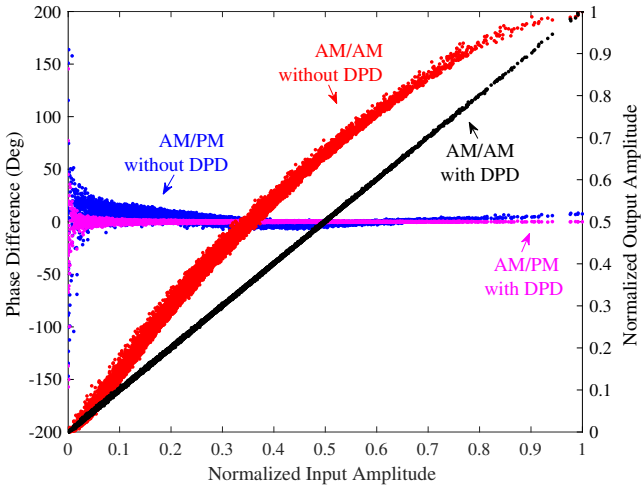


Fig. 22. Measured AM/AM and AM/PM performance at 3.45 GHz with 60 MHz 9-dB PAPR LTE signal with and without DPD.

signals. The average efficiency reaches 52.1%/45.8%/44.4% in the three cases. Fig. 22 reports the measured AM/AM

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART PAS

Ref. Year	Architecture	Freq (GHz)	P_{sat} (dBm)	$\eta@P_{sat}$ (%)	OBO (dB)	η@OBO (%)	Gain (dB)	Signal BW (MHz)	PAPR (dB)	P_{avg} (dBm)	$\eta@P_{avg}$ (%)	ACLR (dBc)
[18] 2014	3-way DPA	1.85-2.45	43.7	60-75	12-14	60-69	7-12	10	8.2	34.5	59	-45.7
[19] 2017	Sym. 3-way DPA	2.14	50	66.5	8.6	33.7	13	10	6.5	41.4	33.7	-38*
[20] 2018	Asym. 3-stage DPA	0.6-0.9	46.9-46.1	51.1-78	12	50-61.8	7-11	10	11.75	35.5	51.7	-46.8
[29] 2018	RF-input LMBA	2.4	45.6	67	6	54	12	3.84	9	38	47	-27*
[30] 2019	3-stage DPA	1.6-2.6	45.5-46	53-66	9.5	50-53	8.5-11	40	8.5	36.3	50	-50
[27] 2020	RF-input SLMBA	3.05-3.55	42.3-43.7	60.8-73.8	10	43.2-51.4	9.5-10.3	200	10	33	48.2	-43.9
[31] 2020	PD-LMBA	1.5-2.7	43	58-72	10	47-58	8	10	9.5	33.5	47-58	-25.8*
[32] 2020	Dual-band 3-way DPA	2.1/3.45	48/47.5	72/63	9	50/43	8.4/9.3**	20	7.3	40.7/40.3	56/47	-50
This Work	3-stage load modulated PA	3.3-3.6	44.5-45	66.9-70.1	6/8/10	51.2-62.1 52-53.8 42.2-47.3	10.6-11.4	60	7/8/9	35.7/34.5/34	52.1/45.8/44.4	-48.4/-51/-50.7

* ACLR without DPD, ** read from graph.

and AM/PM performance with and without DPD under 60 MHz 9-dB PAPR signals. The proposed PA shows satisfactory linearity with DPD.

C. Performance Comparison

The performance of the prototype PA is summarized and compared with other published works in Table. II. The fabricated PA shows comparable performance and the efficiency is maintained within the designed power back-off range. Moreover, the designed PA provides satisfied average efficiency performance when processing the modulated signal with wider bandwidth. It should be noticed that the power back-off level of the proposed PA can be reconfigured to accommodate different signals on demand. The proposed power amplifier aims at the efficiency enhancement at the power back-off, and operates at relatively high frequency compared to other works, the bandwidth is not the main concern in this design.

V. CONCLUSION

A new load modulated power amplifier architecture adopting the coupler as the load modulation network is proposed, and a three-stage load modulated power amplifier is demonstrated. The proposed architecture provides improved drain efficiency within the entire back-off range. The fabricated prototype achieves 70.1% drain efficiency at 45 dBm saturated power and can reach 62.1%/53.8%/47.3% drain efficiency at 6-/8-/10-dB OBO respectively. When processing modulated LTE signals, it also provides satisfied efficiency and linearity performance with DPD implementation.

The proposed architecture offers simple output combiner design to obtain high average efficiency. Furthermore, the power back-off level can be reconfigured by simply modifying the bias conditions after the circuit implementation, which shows the potential of accommodating varying signals.

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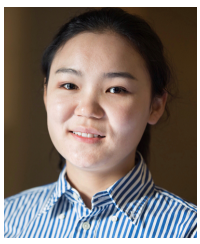

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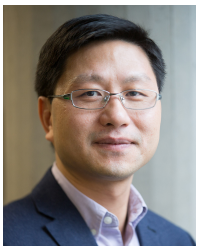

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