# A 0.5 V 0.5 mW Switching Current Source Oscillator

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***Abstract*— This paper proposes a new RF oscillator topology that is suitable for ultra-low voltage and power applications. By employing alternating current source transistors, the structure combines the benefits of low supply voltage operation of conventional NMOS cross-coupled oscillators together with high current efficiency of the complementary push-pull oscillators. In addition, the 1/f noise upconversion is also reduced. The 40 nm CMOS prototype exhibits an average FoM of 189.5 dBc/Hz over 4–5 GHz tuning range, dissipating 0.5 mW from 0.5 V power supply, while abiding by the technology manufacturing rules.**

***Index Terms*— Switching current source oscillator, VCO, DCO, transformer, ultra-low voltage/power oscillators.**

## I. Introduction

Ultra-low-power (ULP) transceivers underpin short-range communications for wireless internet-of-things (IoT) applications. However, their system lifetime is extremely limited by the transceiver's power consumption and available battery technology. On the other hand, energy harvesting technologies typically deliver supply voltages that are much lower than the standard supply of CMOS circuits; e.g., on-chip solar cells can supply only 200–800 mV. Although boost converters can bring the level up to the required ∼1 V, their poor efficiency (≤80%) wastes the harvested energy. Consequently, RF oscillators, as one of the transceiver's most power hungry circuitry, must be very power efficient and preferably operate directly at the energy harvester output. In this paper, we propose a new RF oscillator topology to address the aforementioned constraints without sacrificing manufacturability and phase purity.

## II. Oscillator Power Consumption Tradeoffs

The phase noise (PN) of the traditional oscillator (i.e., class-B) with an ideal current source at an offset frequency $\Delta\omega$ from its resonating frequency $\omega_0$ can be expressed as,

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{KT}{2\,Q_t^2\,\alpha_I\,\alpha_V\,P_{DC}}\,(1+\gamma)\left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \quad (1)$$

where, $Q_t$ is the LC-tank quality factor; $\alpha_I$ is the current efficiency, defined as ratio of the fundamental current harmonic $I_{\omega_0}$ over the oscillator DC current $I_{DC}$; and $\alpha_V$ is the voltage efficiency, defined as ratio of the drain oscillation amplitude $V_{osc}$ (single-ended) over the supply voltage $V_{DD}$ [1]. As a consequence, $V_{osc}$ can be calculated by one of the following equations,

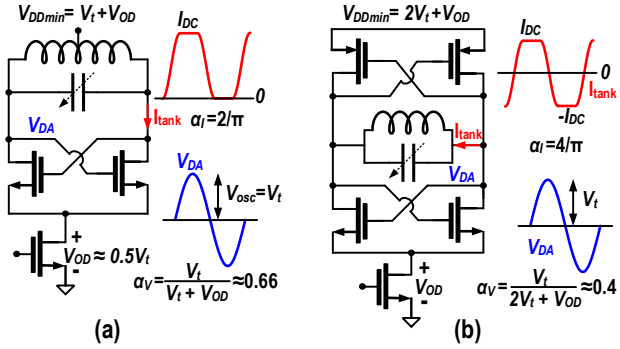


Fig. 1. $V_{DDmin}$, $\alpha_I$ and $\alpha_V$ parameters for: (a) cross-coupled NMOS; and (b) complementary push-pull oscillators.

$$V_{osc} = \alpha_V V_{DD} = R_{in} I_{\omega_0} = R_{in}\alpha_I I_{DC} \quad (2)$$

where, $R_{in}$ is an equivalent input parallel resistance of the tank's losses. Eq. (1) demonstrates a trade-off between power consumption, $P_{DC}$, and PN. The PN requirements are quite trivial for IoT applications and can be easily met by LC oscillators as long as Barkhausen start-up criterion is satisfied over process, voltage and temperature (PVT) variations. Consequently, reducing $P_{DC}$ is the ultimate goal of IoT applications. The $I_{DC}$ can be calculated by using the second and last terms of (2),

$$I_{DC} = V_{DD}\cdot\frac{\alpha_V}{\alpha_I}\cdot\frac{1}{R_{in}} \quad (3)$$

As a result, the RF oscillator's $P_{DC}$ is derived by

$$P_{DC} = V_{DD}^2\cdot\frac{\alpha_V}{\alpha_I}\cdot\frac{1}{R_{in}}. \quad (4)$$

Eq. 4 indicates that the minimum achievable $P_{DC}$ can be expressed in terms of a set of optimization parameters, such as $R_{in}$, and a set of topology dependent parameters, such as minimum supply voltage ($V_{DDmin}$), current and voltage efficiencies.

Lower $P_{DC}$ is typically achieved by scaling up $R_{in}$=$L_p\omega_0 Q_t$ simply via a large multi-turn inductor [2]. For example, by continuing increasing the inductance by 2× at constant $Q_t$, $R_{in}$ could theoretically enhance by 2×, which would reduce $P_{DC}$ by half with a 3 dB PN degradation. However, at some point, that tradeoff stops due to a dramatic drop in the inductor's self-resonant frequency and Q-factor. This constraint sets an upper limit on maximum $R_{in}$, which is a function of technology.

TABLE I
MINIMUM $P_{DC}$ FOR DIFFERENT RF OSCILLATOR TOPOLOGIES

| Topology | $V_{DDmin}$ | $\alpha_V$@$V_{DDmin}$ | $\alpha_I$ | $P_{DCmin}$ |
|---|---|---|---|---|
| $OSC_N$ | $V_t+V_{OD}\approx 1.5V_t$ | ~0.66 | $2/\pi$ | $2.35\ V_t^2/R_{in}$ |
| $OSC_{NP}$ | $2V_t+V_{OD}\approx 2.5V_t$ | ~0.4 | $4/\pi$ | $2\ V_t^2/R_{in}$ |
| This work | $V_t+V_{OD}\approx 1.5V_t$ | ~0.33 | $4/\pi$ | $0.6\ V_t^2/R_{in}$ |

The topology parameters also play an important role in the minimum achievable $P_{DC}$. Figure 1 shows such effects for the traditional cross-coupled NMOS-only ($OSC_N$) and complementary push-pull ($OSC_{NP}$) structures. The $V_{DDmin}$ of $OSC_N$ can go lower than in $OSC_{NP}$. However, the current efficiency of $OSC_{NP}$ is doubled due to the switching of tank current direction every half period. Its voltage efficiency is also smaller. Hence, $OSC_{NP}$ offers $\sim 3\times$ lower $\alpha_V/\alpha_I$. Consequently, each of these structures has its own set of advantages and drawbacks such that the minimum achievable $P_{DC}$ according to (4) is almost identical, as shown in Table I.

In this paper, we propose to convert the fixed current source of the traditional NMOS topology into a structure with alternating current sources such that the tank current direction can change every half-period. Consequently, the benefits of low supply of the $OSC_N$ topology and higher $\alpha_I$ of $OSC_{NP}$ structure are combined to reduce power consumption further than practically possible in the traditional oscillators.

## III. SWITCHING CURRENT SOURCE OSCILLATOR

Figure 2 illustrates the proposed oscillator's schematic, waveforms and various operational regions of $M_{1-4}$ transistors across the oscillation period. The two-port resonator consists of a step-up 1:2 transformer and tuning capacitors ($C_1$, $C_2$) at its primary and secondary windings. The current source transistors $M_{1,2}$ set the oscillator's DC current. These devices, along with $M_{3-4}$, play a vital role of switching the tank current direction. To realize that, both $M_{1,2}$ and $M_{3,4}$ pairs must demonstrate positive feedback mechanism. Consequently, the transformer's primary and secondary out-of-phase ports are respectively connected to the drain and gate of $M_{1,2}$ devices. The single-ended output resistance of $M_2$ is given by

$$R_d = \frac{r_{o2}}{1 - A \cdot g_{m2} r_{o2}} \overset{A\, g_{m2} r_{o2} >> 1}{\Longrightarrow} R_d = \frac{-1}{A \cdot g_{m2}} \quad (5)$$

where, $A$ is the transformer passive voltage gain between its windings. On the other hand, the transformer's in-phase signals must be applied to the source and gate of $M_{3,4}$ devices to realize positive feedback. The real part of the impedance seen at the source of $M_4$ can be expressed by

$$R_{up} = \frac{r_{o4}}{1 - (A-1) \cdot g_{m4} r_{o4}} \approx \frac{-1}{(A-1) \cdot g_{m4}} \quad (6)$$

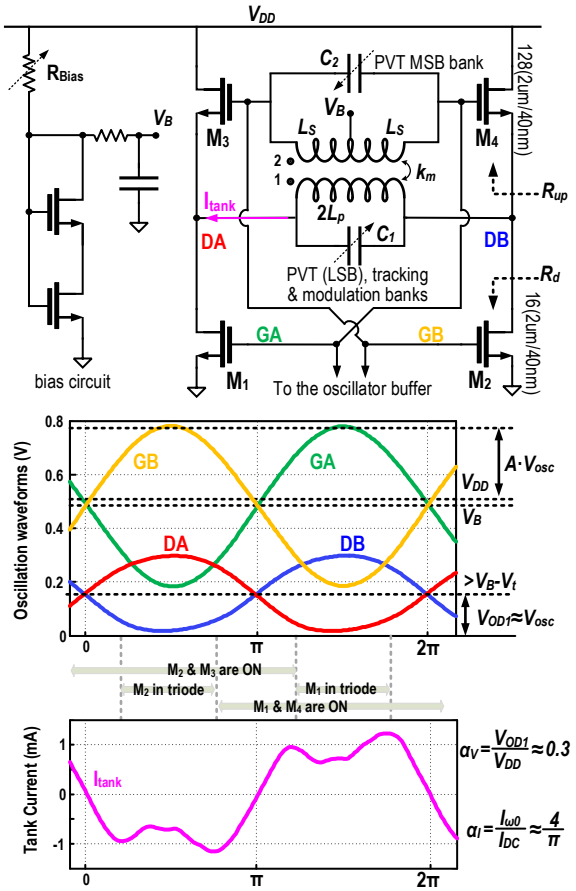


Fig. 2. Schematic and waveforms of the proposed oscillator.

Equations (5), (6) clearly indicate that $A$ must be safely larger than 1 to have positive feedback from both upper and lower sides of the tank. This justifies utilizing a 1:2 step-up transformer in the oscillator's tank.

As can be gathered from Fig. 2, $G_B$ oscillation voltage is high within the first half-period. Hence, only $M_2$ and $M_3$ transistors are on and the current flows from left to right side of the tank. However, $M_1$ and $M_4$ are turned on for the second half-period and tank's current direction is reversed. Consequently, like in the push-pull structure, the tank current flow is reversed every half-period thus doubling the oscillator's $\alpha_I$ to $4/\pi$.

The minimum $V_{DD}$ is determined by the bias voltage $V_B$,

$$V_{DDmin} \approx V_B = V_{OD1} + V_{gs3}. \quad (7)$$

Eq. (7) implies that $M_{3,4}$ should work in weak-inversion keeping $V_{gs3} < V_t$ to achieve lower $V_{DDmin}$. Since, $M_{1-4}$ have the same DC gate voltage, $M_{3,4}$ sub-threshold operation also offers enough $V_{OD}$ for the switching current source devices to operate in the saturation region at the DC operating point. Hence, unlike traditional oscillators, the dimension of $M_{3,4}$ devices must be a

few times (i.e., 8×) larger than current source devices to guarantee their weak-inversion operation. On the other hand, the oscillation swing cannot go further than $V_{OD1,2}$ at DA/DB nodes, which is chosen ∼150 mV to satisfy the system's phase noise requirement by a few dB margin. Consequently, as with $\mathrm{OSC_N}$, the proposed structure can operate at $V_{DD}$ as low as 0.5 V.

Such a low $V_{DD}$ and oscillation swing can easily lead to start-up problems in the traditional structures and increase in the oscillator buffer power consumption ($P_{buf}$) in order to provide a rail-to-rail swing of the LO output. Fortunately, the transformer gain enhances the oscillation swing at $\mathrm{M_{1,2}}$ gates to even beyond $V_{DD}$, guaranteeing the oscillator start-up and reduction of $P_{buf}$. Furthermore, $\mathrm{M_{1-4}}$ contribution to the oscillator's PN is also reduced by the transformer's voltage gain [1].

$\mathrm{M_1}$ and $\mathrm{M_2}$ transistors alternatively enter the triode region for part of the oscillation period, as shown in Fig. 2. However, $\mathrm{M_{3,4}}$ devices work only in the saturation and exhibit negative output resistance for their entire on-state operation. Consequently, only one side of the tank is connected to the ac ground when either $\mathrm{M_1/M_2}$ is in the linear region while the other side sees high impedance. Hence, this structure preserves the tank's charge and Q-factor over the entire oscillation period. Contrary to the traditional oscillators, the tank loading effect due to the low output impedance of the current source transistor is not an issue in the proposed architecture.

Dynamically switching the bias of MOS devices will reduce their flicker noise, as also demonstrated in [3]. It also lessens the DC component of their effective impulse sensitivity function. Consequently, a lower $1/f^3$ PN corner is expected than in the traditional oscillators. Furthermore, the $V_{DD}$ variation cannot directly modulate $V_{gs}$ and thus nonlinear $C_{gs}$ of $\mathrm{M_{1-4}}$ devices. An RC filter is also placed between $V_{DD}$ and $V_B$ to further reduce the deterministic noise on the bias voltage. Hence, the frequency pushing should be very small, thus making it suitable for direct connection to solar cells and integration with PA.

Larger $R_{in}$ and $A$ are desired to reduce $P_{DC}$ and $P_{buf}$, respectively. Both optimization parameters are a strong function of $X{=}L_sC_2/L_pC_1$, as shown in Fig. 3 (b) and (c). $R_{in}$ is enhanced by a factor of $(1{+}k_m)^2/2$ at $X{=}1$ for $Q_p{\approx}Q_s$, which is reasonable for monolithic transformers. However, $A$ increases by having a larger $X$-factor as gathered from Fig. 3 (c). To consider both scenarios, trans-impedance $R_{21}{=}R_{in}{\cdot}A$ term is defined and depicted in Fig. 3 (d). The $R_{21}$ also reaches its maximum at $X{=}1$. For this reason, the PVT switched-MOM-capacitor banks are distributed between the transformer's primary and secondary to roughly satisfy this criterion. We also define the maximum of $R_{21}$ as the transformer

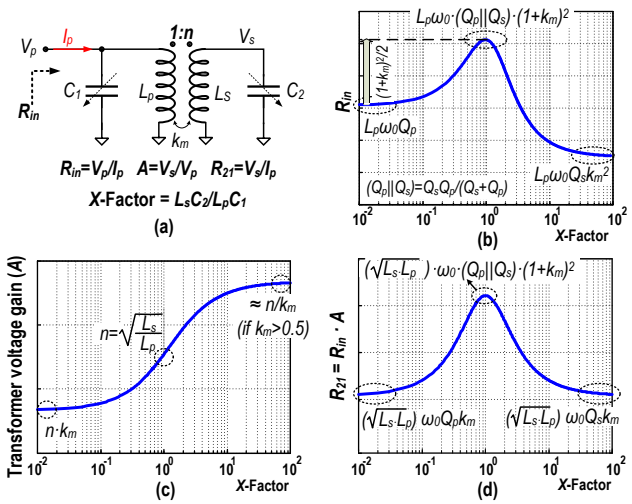


Fig. 3. Transformer-based tank: (a) schematic; (b) input parallel resistance; (c) voltage gain; and (d) $R_{21}$ versus X-factor.

$\mathrm{FoM} = (Q_p||Q_s){\cdot}(1{+}k_m)^2{\cdot}\sqrt{L_pL_s}\cdot\omega_0$. Consequently, the transformer dimension and winding spacing are chosen to maximize this term. Unfortunately, lower thin metal layers must be used for the cross connections of a step-up transformer as the number of primary turns exceeds one. That constraint increases the transformer's losses and reduces tank's Q-factor and $R_{in}$. Consequently, the maximum achievable $R_{in}$ is somewhat smaller for the transformer-based tank as compared to a simple LC resonator in the same CMOS technology.

## IV. Measurement Results

The oscillator was prototyped in TSMC 40 nm 1P7M CMOS. The chip micrograph is shown in Fig. 4 (a). $\mathrm{M_{1,2}}$ and $\mathrm{M_{3,4}}$ transistors are minimum-length low-$\mathrm{V_t}$ devices with a width of 32 $\mu$m and 256 $\mu$m, respectively. The transformer's primary and secondary differential self-inductance is only 660 pH and 2 nH, respectively, with the coupling factor $k_m$=0.76. Both transformer's winding are realized with top ultra-thick metal (3.5 $\mu$m). However, the transformer includes a floating M1-to-M6 shield to comply with the strict metal density rules (>10–20%) for manufacturability and also to alleviate the substrate loss. Note that the shield must be significantly thinner than the skin depth at the desired frequency to avoid any attenuation of the magnetic field. The skin depth of copper is ∼0.9 $\mu$m at 5 GHz. However, the thickness of M6 layer is 0.85 $\mu$m. Hence, adding M6 dummy metal reduces the transformer's magnetic field, inductance, Q-factor and thus $R_{in}$ drops by 10–20%. The simulated Q-factor is 12 and 16 for the primary and secondary windings, respectively.

Figure 5 shows the measured PN at the highest and lowest frequencies ($\mathrm{f_{max}}$, $\mathrm{f_{min}}$) with $V_{DD}$ of 0.5 V and $P_{DC}$ of 470-and-580 $\mu$W, respectively. Thanks to

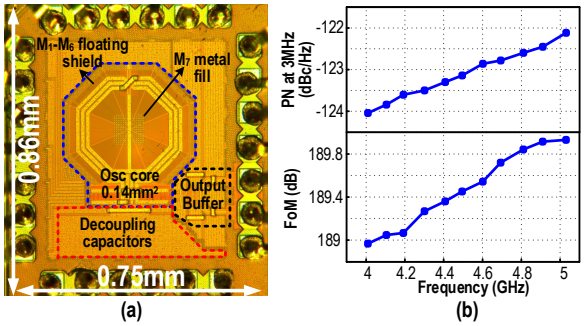


Fig. 4. (a) Chip micrograph; (b) Measured oscillator phase noise and FoM at 3 MHz offset frequency across the tuning range.

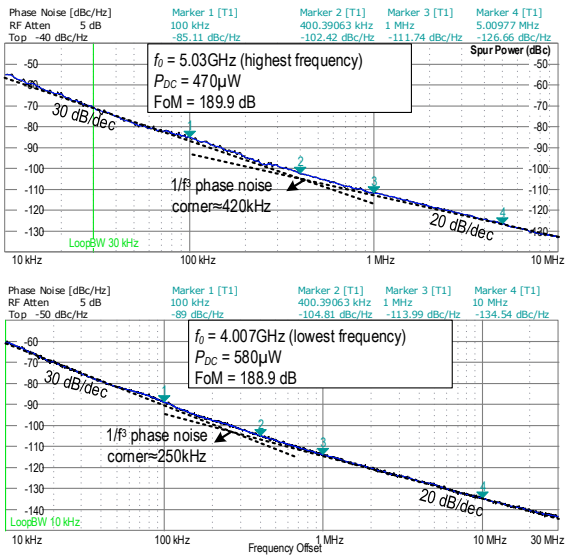


Fig. 5. Measured phase noise of the proposed oscillator.

TABLE II
COMPARISON TABLE OF LOW POWER OSCILLATORS

| | This work | [4] JSSC'05 | [5] JSSC'08 | [6] ESSCIRC'14† | [2] ISSCC'14 |
|---|---|---|---|---|---|
| **Technology** | 40nm | 0.18$\mu$m | 0.13$\mu$m | 28nm | 40nm |
| **$V_{DD}$** | 0.5V | 0.5V | 1V | 0.5V | 1V |
| **TR(%)** | 22.2 | 8.7 | 14 | N/A | 24.5 |
| **$f_0$(GHz)** | 4.8 | 3.8 | 4.9 | 2.35 | 2.44 |
| **PN (dBc/Hz)‡** | -139 | -143 | -149.5 | -125.8 | -131.1 |
| **$P_{DC}$ (mW)** | 0.48 | 0.57 | 1.4 | 0.38 | 0.4 |
| **FoM (dB)** | 189.8 | 193 | 195.5 | 187.5 | 183 |
| **$FoM_T$ (dB)*** | 196.7 | 191.7 | 198.5 | N/A | 190.8 |
| **Freq pushing** | 17MHz/V | 273MHz/V | N/A | N/A | N/A |
| **Dummy fill** | Yes | No | No | No | No |
| **Area (mm²)** | 0.14 | 0.23 | 0.11 | 0.2 | 0.15 |
| **Oscillator topology** | switching current source | TRX feedback | Class C | Class D | Tradi tional |

† including LDO. LDO also performs a start-up role.
‡at $\Delta f$=10 MHz normalized to 2.4 GHz carrier.
*$FOM_T$ = |PN|+20 $\log_{10}((f_0/\Delta f)(TR/10))$ - 10 $\log_{10}(P_{DC}(mW))$.

the switching current source technique, 1/f$^3$ PN corner of the oscillator is relatively low and varies between 250-to-420 kHz across the tuning range (TR). The oscillator has a 22.2% TR, from 4 to 5 GHz. Figure 4 (b) displays plots of phase noise and FoM across the TR. The FoM reaches maximum 189.9 dBc at $f_{max}$ and varies ~1 dB across the TR.

Table II summarizes the proposed oscillator performance and compares it with relevant state-of-the-art for $P_{DC}$<2 mW and TR>8%. It is the only one with the all-layer dummy metal fills inside the LC-tank for manufacturability. For the similar $P_{DC}$ (400–600 $\mu$W), only the transformer-feedback VCO [4] shows better FoM but with a much larger area, lower TR and extremely high frequency pushing. Class-C VCO [5] also shows better FoM but at a much higher $P_{DC}$. Furthermore, it needs additional complex biasing circuits (such as opamp) for proper operation, which can potentially limit its minimum $V_{DD}$ and thus $P_{DC}$.

## V. Conclusion

A switching current source oscillator has been proposed and analyzed, providing deep insights into beneficial circuit operation. It combines advantages of low supply voltage operation of the conventional NMOS cross-coupled oscillator with high current efficiency of the complementary push-pull oscillator to reduce the oscillator supply voltage and dissipated power without sacrificing its start-up robustness or loading tank's Q-factor. The 40 nm CMOS prototype exhibits 189.5 dBc/Hz FoM, with 22% tuning range, dissipating 0.5 mW from 0.5 V power supply, while complying with the process technology manufacturing rules.

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