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Limit Cycle Behavior in a Class-AB Second-Order Square Root Domain Filter

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Abstract— This paper shows how an unwanted limit cycle can be exhibited by a second-order CMOS companding filter. The filter employs the quasi-quadratic law of the MOS transistor in strong inversion and saturation to achieve compression together with a Class-AB topology to extend the dynamic range. In the zero-input case, the filter operates in the manner expected of an externally-linear circuit. However, when a standard linear IC design technique is applied to it, unwanted zero-input sustained oscillations may be observed. Simulations from PSpice and measurement results from a semi-custom realization in a 0.8 μ m CMOS process are used to explore this behavior. This work highlights an aspect of the behavior of such filters that must be taken into account by analog designers.

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Abstract— This paper shows how an unwanted limit cycle can be exhibited by a second-order CMOS companding filter. The filter employs the quasi-quadratic law of the MOS transistor in strong inversion and saturation to achieve compression together with a Class-AB topology to extend the dynamic range. In the zero-input case, the filter operates in the manner expected of an externally-linear circuit. However, when a standard linear IC design technique is applied to it, unwanted zero-input sustained oscillations may be observed. Simulations from PSpice and measurement results from a semi-custom realization in a 0.8 μm CMOS process are used to explore this behavior. This work highlights an aspect of the behavior of such filters that must be taken into account by analog designers.

1. Introduction

Companding filters are externally-linear internally-nonlinear circuits employing the large-signal nonlinear current-voltage characteristic of a transistor in such a way as to obtain linear input-output behavior [1]. In these filters the input voltages are compressed in a nonlinear manner, then processed, and finally expanded at the output to recover overall input-output linearity. This is achieved by connecting in a particular manner nonlinear cells, usually employing transistor circuit topologies known as translinear loops [2]-[3]. The first companding filters employed the exponential current-voltage characteristic of BJT transistors in the forward-active mode or MOS transistors in weak inversion, leading to the so called Log-Domain filters [4]-[6]. Later, in order to avoid the limited bandwidth and poor matching of MOS transistors in weak inversion, the quadratic law of MOS transistors in strong inversion and saturation was employed in square root-domain (SRD) companding filters [7]-[8]. The synthesis of these filters is the subject of ongoing research [9-12], but there is still a lack of understanding of particular effects of the nonlinearities.

Although the companding technique permits the design of filters featuring small distortion levels, large signal-to-noise ratios, low supply voltages, and wide bandwidths, it may also give rise to externally-nonlinear behavior. The occurrence

of unwanted limit-cycle behavior in log-domain filters is reported in [13] and investigated in [14], [15]. The appearance of multiple operating points in such filters is discussed in [16]. Reference [17] reported the appearance of multiple operating points in a square root domain filter and the way to avoid it from a circuit point of view. This paper shows that square root-domain filters may also suffer from external nonlinearity. To this end, a fully-differential class-AB second-order SRD filter is designed, and then modified according to the standard linear IC design technique, whereby any pair of equal-value capacitors, each connected between a node and ground, is replaced with a single half-sized floating capacitor placed between those nodes. This saves IC area, but may induce zero-input limit-cycle behavior under particular conditions. This unwanted nonlinear behavior is comprehensively analyzed through circuit simulations and confirmed by performing measurements on a semi-custom IC realization implemented in 0.8 μm CMOS technology.

The paper is organized as follows. Section II provides the Class-AB SRD filter design. Simulations and measurements of the limit cycle behavior in a fabricated prototype are introduced in Section III. Finally several conclusions are drawn in Section IV.

2. Filter Design

This section presents the SRD filter. The synthesis method is based on linear g_m - C filters as the linear prototype. Such a g_m - C filter is translated to a companding version through a nonlinear map. Thus, the prototype linear transconductors g_m are converted to nonlinear equivalents G_M leading to the companding G_M - C counterpart [18].

2.1 Second-order SRD Filter

Fig. 1 shows the second-order linear g_m - C filter chosen as basic prototype for the realization of the companding filter. The filter is implemented with four linear transconductors and two linear capacitors. The input and output voltages are v_{in} and v_2 respectively. The filter is a second-order low-pass filter with cut-off frequency ω_o , dc gain K , and Q factor given by:

$$\omega_o = \sqrt{\frac{g_{12}g_{21}}{C_1C_2}}, K = \frac{g_{10}}{g_{12}}, Q = \frac{\sqrt{g_{12}g_{21}}}{g_{22}} \sqrt{\frac{C_2}{C_1}}. \quad (1)$$

Figure 1

Let us derive the current-voltage characteristic of the nonlinear transconductor G_M , which will replace its linear equivalent g_m in the final companding filter. The defining equations of capacitors in the g_m - C filter of Fig. 1 yield:

$$\begin{cases} C_1 \dot{v}_1 = g_{10}v_{in} - g_{12}v_2 \\ C_2 \dot{v}_2 = g_{21}v_1 - g_{22}v_2 \end{cases}. \quad (2)$$

In order to derive the SRD equivalent of (2), a nonlinear mapping, based on the quadratic law of MOS transistors operating in strong inversion and saturation (I_i in equation (3)), is applied to voltages v_{in} , v_1 and v_2 :

$$\begin{cases} v_{in} = RI_{IN} = R\beta (v_{CIN} - V_T)^2 / 2 \\ v_1 = RI_1 = R\beta (v_{C1} - V_T)^2 / 2 \\ v_2 = RI_2 = R\beta (v_{C2} - V_T)^2 / 2 \end{cases}, \quad (3)$$

where R is a resistance which allows a suitable current-to-voltage conversion, and v_{Ci} , β , and V_T denote the gate-source voltage, the transconductance parameter, and the threshold voltage of a MOS transistor respectively. Substituting (3) into (2), applying the chain rule, and solving for v_{C1} and v_{C2} , the companding filter equivalent of (2) is found to be:

$$\begin{cases} C_1 \dot{v}_{C1} = g_{10} \frac{(v_{CIN} - V_T)^2}{2(v_{C1} - V_T)} - g_{12} \frac{(v_{C2} - V_T)^2}{2(v_{C1} - V_T)} \\ C_2 \dot{v}_{C2} = g_{21} \frac{(v_{C1} - V_T)^2}{2(v_{C2} - V_T)} - g_{22} \frac{(v_{C2} - V_T)^2}{2(v_{C2} - V_T)} \end{cases}. \quad (4)$$

Figure 2

Equation (4) is implemented by the SRD G_M - C filter of Fig. 2, where voltages v_{CIN} , v_{C1} , and v_{C2} are the compressed equivalents of voltages v_{in} , v_1 and v_2 ,

respectively, in the prototype of Fig. 1. Furthermore, the g_m -C prototype and the SRD filter share the same circuit topology. However, in the latter, two MOS transistors have been added so as to allow compression of the input signal ($i_{in} = v_{in}/R$) and expansion of the output one ($i_{out} = v_2/R$). Thus from (4) it follows that the current-voltage characteristic of G_M with input node i and output node j is described by:

$$i_j = g_m \frac{(v_i - V_T)^2}{2(v_j - V_T)}. \quad (5)$$

Several practical transistor-level implementations of (5) have been reported in the literature [18]-[20]. In this paper the implementation of the nonlinear transconductor G_M employs multiple coupled MOS translinear (TL) loops [20].

2.2 Implementation of the nonlinear transconductor G_M

The block G_M is based on TL loops. The MOS TL Principle [19] states that in a loop with an even number of transistors, with as many gate-to-source connections arranged clockwise (CW) as the number of gate-to-source connections in counter-clockwise (CCW) configuration, if it is assumed that all transistors operate in strong inversion and saturation, then the relationship among their currents is given by:

$$\sum_{CW} \sqrt{\frac{i}{W/L}} = \sum_{CCW} \sqrt{\frac{i}{W/L}}, \quad (6)$$

where i , W , and L are drain current, channel width and length of a MOS transistor respectively. Fig. 3 shows the implementation of the nonlinear transconductor G_M , where v_i denotes the voltage at the input node i , i_j the current flowing out of the output node j , and all MOS transistors are assumed to operate in strong inversion and saturation. The minimum supply voltage of the circuit may be as low as $v_{GS} + 2 v_{DS sat}$, fully exploiting the capacity of the companding technique. Voltage V_B is used to bias the circuit. Transistor pairs $M_{10} - M_{11}$ and $M_{11A} - M_{10A}$ are configured as simple current mirrors. In the circuit of Fig. 3 three coupled MOS translinear loops, specifically $M_1 - M_2 - M_4 - M_3$, $M_{1A} - M_{2A} - M_{4A} - M_{3A}$, and $M_1 - M_3 - M_{4A} - M_{2A}$, may be recognized. Transistor triplet $M_9 - M_8 - M_7$ ($M_{9A} - M_{8A} - M_{7A}$) is a current steering circuit necessary to inject current I_C (i_1) into

transistors M_4 and M_1 (M_{4A} and M_{1A}). Next, the nonlinear current-voltage characteristic of G_M is derived. Application of the TL Principle, expressed by (6), to MOS TL loop $M_1 - M_2 - M_4 - M_3$ yields:

$$\sqrt{i_5} + \sqrt{i_6} = 2\sqrt{I_C}. \quad (7)$$

A similar analysis is applied to MOS TL loop $M_{1A} - M_{2A} - M_{4A} - M_{3A}$, giving

$$\sqrt{i_3} + \sqrt{i_4} = 2\sqrt{i_1}, \quad (8)$$

and to MOS TL loop $M_1 - M_3 - M_{4A} - M_{2A}$, producing

$$\sqrt{I_C} + \sqrt{i_1} = \sqrt{i_4} + \sqrt{i_6}. \quad (9)$$

In each of these MOS TL loops, the transistors are assumed to be perfectly matched. Finally, Kirchhoff's Current Law is applied to the drain of M_{11A} , yielding

$$i_4 = i_2 + i_3. \quad (10)$$

Solving (7)-(10) for i_3 , i_4 , i_5 and i_6 in terms of i_1 , i_2 and I_C , the nonlinear current-voltage characteristic of the circuit of Fig. 3 turns out to be represented by:

$$i_j = i_5 - i_6 = \sqrt{\frac{I_C}{i_1}} i_2 = \sqrt{2\beta I_C} \frac{(v_i - V_T)^2}{2(v_j - V_T)}. \quad (11)$$

Thus, letting

$$g_m = \sqrt{2\beta I_C}, \quad (12)$$

the circuit shown in Fig. 3 implements the nonlinear current-voltage characteristic expressed by (5). The aspect ratios of the MOSFETs employed in the nonlinear transconductor are shown in Table 1.

Figure 3

Table 1

2.3 Class-AB SRD filter

The design of the class-AB SRD filter, employing the technique described in [21], [22], is based on the use of two identical Class-A filters of the type shown in Fig. 2, a current splitter, and a current subtraction stage, as depicted in Fig. 4. Note that we use the simplest form of a Class-AB topology i.e., without local positive feedback between capacitors in order to highlight that the appearance of the limit cycle is due to the interactions between Class-A filters through a capacitance. The

second order Class-A filter with on-chip tuning has been already reported in [23]. In Fig. 4 the splitter first converts a differential input voltage, v_{id} , into a corresponding differential input current i_{id} , and then splits the latter into two always positive currents, i_{i+} and i_{i-} , which are applied to identical class-A second-order SRD filters, thus producing output signals i_{o+} and i_{o-} respectively. The linear output current i_{od} is obtained by subtracting i_{o-} from i_{o+} .

Figure 4

The current splitter employed in the design is based on the well-known Class-AB transconductor [24] (Fig. 5). In Fig. 5 V_{CM} denotes the common-mode input voltage. The positive and negative input voltages are applied to the gates of M_2 and M_3 respectively. Transistors M_4 and M_1 set the source voltages of M_2 and M_3 respectively, thus yielding the following mathematical expressions for i_{i+} and i_{i-} :

$$i_{i+(-)} = \beta v_{id}^2 / 2 + I_o \pm \sqrt{2\beta I_o} v_{id}. \quad (13)$$

It follows that

$$i_{i+} + i_{i-} = \beta v_{id}^2 + 2I_o, \quad i_{i+} - i_{i-} = i_{id} = 2\sqrt{2\beta I_o} v_{id}. \quad (14)$$

Figure 5

Equation (14) guarantees that currents i_{i+} and i_{i-} are positive at all times [25]. Note that the current splitter of Fig. 5 has the same circuit topology as block of MOS transistor $M_1 - M_9$ in the nonlinear transconductor G_M of Fig. 3. Furthermore, the aspect ratios of transistors of Fig. 5 are equal to those of MOS transistors $M_1 - M_9$ from Table I. This convenient feature, providing the entire filter with a modular structure, serves to reduce the effect of mismatches in the layout.

Recalling (4), application of the defining equations of the capacitors in the Class-AB second-order SRD filter of Fig. 4 gives:

$$\begin{pmatrix} C_1 + C_{p1} & 0 & -C_{p1} & 0 \\ 0 & C_2 + C_{p2} & 0 & -C_{p2} \\ 0 & -C_{p1} & C_1 + C_{p1} & 0 \\ 0 & -C_{p2} & 0 & C_2 + C_{p2} \end{pmatrix} \begin{pmatrix} \dot{v}_{C1+} \\ \dot{v}_{C2+} \\ \dot{v}_{C1-} \\ \dot{v}_{C2-} \end{pmatrix} = \begin{pmatrix} g_{10} \frac{(v_{CN+} - V_T)^2}{2(v_{C1+} - V_T)} - g_{12} \frac{(v_{C2+} - V_T)^2}{2(v_{C1+} - V_T)} \\ g_{21} \frac{(v_{C1+} - V_T)^2}{2(v_{C2+} - V_T)} - g_{22} \frac{(v_{C2+} - V_T)^2}{2(v_{C2+} - V_T)} \\ g_{10} \frac{(v_{CN-} - V_T)^2}{2(v_{C1-} - V_T)} - g_{12} \frac{(v_{C2-} - V_T)^2}{2(v_{C1-} - V_T)} \\ g_{21} \frac{(v_{C1-} - V_T)^2}{2(v_{C2-} - V_T)} - g_{22} \frac{(v_{C2-} - V_T)^2}{2(v_{C2-} - V_T)} \end{pmatrix}, \quad (15)$$

where the g_m are described by (12) and C_{p1} and C_{p2} are the parasitic capacitances connected between v_{C1+} and v_{C1-} , and v_{C2+} and v_{C2-} , respectively.

3. Limit cycle behaviour: circuit simulations and measurements

The second order filter using four capacitors is formed by two class-A filters (see Fig. 4) without internal feedback except the parasitic elements. When the four capacitors are much larger, these parasitic components can be neglected and the dynamics are determined by those of the class-A filters, as examined in [23]. It is our intention here to see how the behaviour changes when the four capacitors are transformed as described below.

In internally-linear fully-differential circuits it is usual to replace any pair of equal-value capacitors, each connected between a node and ground, with a single half-sized floating capacitor, placed between those nodes. This standard linear IC design technique reduces by a factor of 4 the total area occupied by capacitors. However, when it is applied to internally-nonlinear circuits, it may lead to the emergence of externally-nonlinear behavior even for zero input. So far such unwanted behavior has been observed and investigated in the logarithmic domain [13], [15], but has not yet been explored in other forms of companding filters. It is the aim of this paper to extend these studies to SRD filters.

The floating-capacitor version of the class-AB second-order filter of Fig. 4, where the capacitors are $C_{F1} = C_1 / 2$ and $C_{F2} = C_2 / 2$ and the voltages across them are defined as $v_{CF1} = v_{C1+} - v_{C1-}$ and $v_{CF2} = v_{C2+} - v_{C2-}$, may exhibit unwanted zero-input sustained oscillations. In the following PSpice circuit simulation, the common value of the floating capacitors is set to 500 pF, while the initial conditions on the voltages across them are chosen as $v_{CF1}(0) = 0.1$ V and $v_{CF2}(0) = 0.1$ V. In each nonlinear transconductor the supply and bias voltages are respectively chosen as $V_{DD} = 1.5$ V and $V_B = 1.1$ V. The bias current $I_C = 35 \mu A$ in

all transconductors, with the exception of G_{22} , where I_C was set to $1 \mu A$. The current $I_o=0.25 \mu A$. With this choice of parameters, simulations show unwanted sustained oscillations developing across the floating capacitors. This occurs irrespective of the analytical model used by the simulator to describe the drain current of each MOS transistor. Even the simple level 1 analytical model is sufficient to capture the zero-input limit-cycle. Fig. 6 shows the zero-input limit-cycle of fundamental frequency f_{osc} equal to 3.2 MHz, projected onto the v_{C1+} - v_{C2+} plane.

Figure 6

Through PSpice simulations and then verified by measurement results, it was noted that the limit cycle frequency depends strongly on the parasitic capacitances (added by G_m input-output, layout and board) from V_{C1+} , V_{C1-} , V_{C2+} , and V_{C2-} to ground (see Fig. 4). To provide more insight, simulations were carried out using the level 1 model for MOS transistors and adding equal grounded linear capacitances of 1pF, 2pF, and 3pF to those nodes. These simulations resulted in oscillation frequencies of 1.5 MHz, 1.1 MHz, and 700 kHz, respectively.

Figure 7

A $0.8 \mu m$ CMOS technology process was used to produce a semi-custom IC realization of the floating-capacitor filter. In the measurements, circuit parameters were chosen as in the previously mentioned simulation, but capacitances $C_1=C_2=0.5 nF$ were external.

Fig. 7 shows the voltages v_{C1+} and v_{C2+} in the frequency domain whose oscillation ranges in the time domain are similar to those observed in the simulation result of Fig. 6. Note in Fig. 7 that the voltages are formed by spectral components that are not distributed uniformly, since the nonlinear dynamic of the system. Although parasitic capacitances of value equal to 50 pF were found to be present from each of nodes at voltage v_{C1+} , v_{C2+} , v_{C1-} , and v_{C2-} and ground, they do not have a crucial role on the emergence of the dynamics, since the simulation

from Fig. 6, which does not take them into account, captures the qualitative behavior under study nonetheless.

Figure 8

Fig. 8 shows the zero-input limit cycle on the plane v_{C1+} and v_{C2+} . The solid line shows measurement results from the fabricated prototype and the dashed line shows PSpice simulations using BSIMv3.3 model for MOS transistors. The waveform shapes agree qualitatively, and in both cases the frequency is approximately 100 kHz. This low frequency is due to the grounded large board parasitic capacitances in the measurement setup with values of 50pF approximately. These extra capacitances were added to the PSpice schematic to obtain the plot shown in dashed lines in Fig. 8. Both PSpice simulations and measurements also showed that the frequency and amplitude of the limit cycle could be tuned by means of the quiescent current of the input stage Fig. 5, i.e. by I_o in (14). Such a relation is nonlinear and further research needs to be done in order to model it properly. For instance, in the case of the fabricated prototype, the amplitude of the limit cycle could vary from 0 V to 1.3 V for I_o from 0.1 μ A to 10 μ A.

4. Conclusions

Companding filters have recently attracted the attention of IC designers looking for innovative approaches to meet today's tight system requirements for large signal-to-noise ratios, low distortion levels, low power consumption, and high speed. However, after the application of a standard linear IC design technique, one form of companding filters, where analog processing occurs in the logarithmic domain, was recently found to behave in an externally-nonlinear fashion. This paper showed how this flaw is also featured also by another form of companding filters, which process the signals in the square root domain. In particular, the zero-input oscillations experienced by a class-AB second-order SRD filter were investigated. Simulation and measurement results from a semi custom realization were provided to probe this nonlinear behavior that must be taken into account by analog designers when the floating parasitic capacitances are the same order of the

grounded capacitor. Regarding simulations it was shown that the level 1 model in MOS transistors is enough to predict the limit cycle behavior. Measurement results confirmed all the behavioral observations found in the simulator, but the wave shapes differ from measurement results. Thus a more detailed model of these circuits is required. Since both log-domain and SRD filters may experience external nonlinearity, it would be interesting to investigate whether this is a feature common to all forms of companding filters.

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Figure captions:

Fig. 1. Second-order linear gm-C filter.

Fig. 2. Class-A second-order SRD G_M -C filter. It is derived from the g_m -C linear prototype of Fig. 1 by substituting linear transconductors g_m with nonlinear equivalents G_M .

Fig. 3. Transistor-level implementation of the nonlinear transconductor G_M , based on multiple coupled MOS translinear loops. Its negative counterpart may be easily obtained by taking the drain of M_2 as the output node j , and connecting M_{11} rather than M_{10} as a diode.

Fig. 4. Class-AB second-order SRD filter. The circuit employs two identical class-A filters together with a current splitter and a current subtraction stage.

Fig. 5. Current splitter employed in the class-AB filter of Figure 4. It performs differential voltage-to-differential current conversion, and generates the input currents fed to the two identical class-A filters.

Fig. 6. PSpice simulation result showing the projection of the zero-input limit-cycle onto the $v_{C1+} - v_{C2+}$ plane, using level 1 model for MOS transistors.

Fig. 7. Zero-input oscillations in the frequency domain resulting from a measurement on a semi-custom IC realization of the floating-capacitor filter

Fig. 8. Zero-input oscillations. Measurement results from a semi-custom IC realization (solid line). Simulation results using 0.8um BSIMv3.3 models for MOS transistor (dashed line).

Figure 1

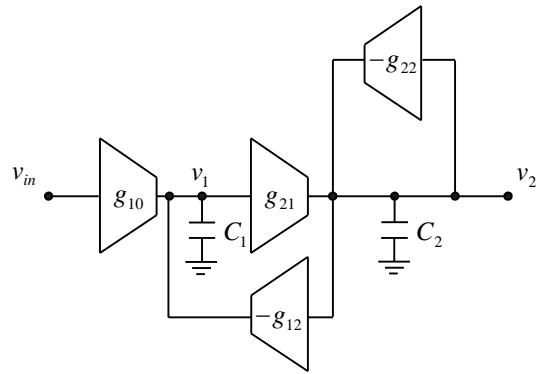


Figure 2

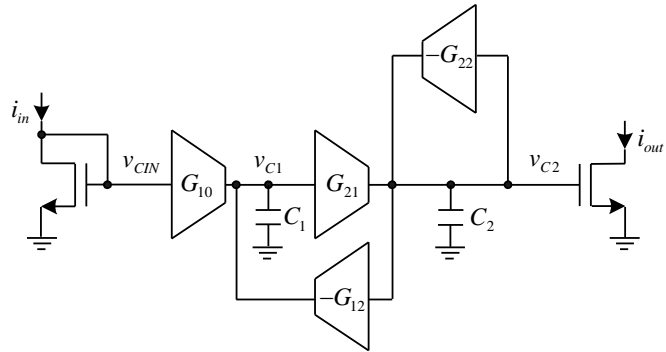


Figure 3

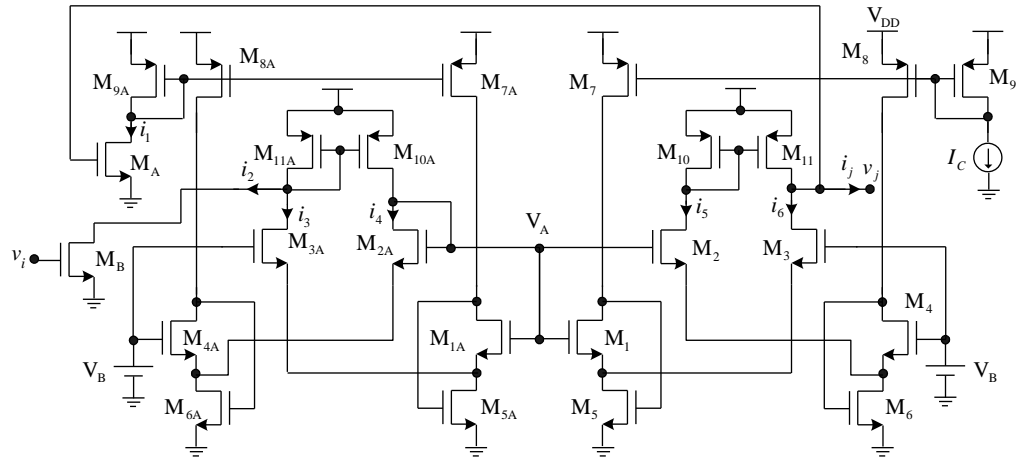


Figure 4

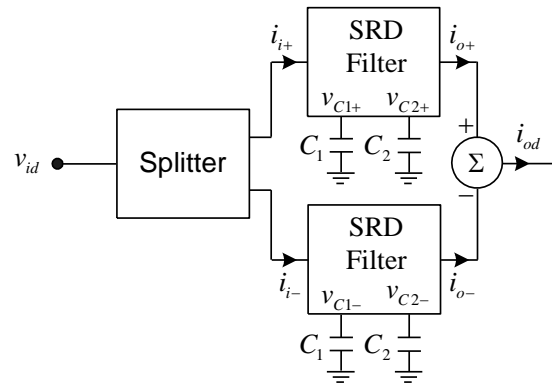


Figure 5

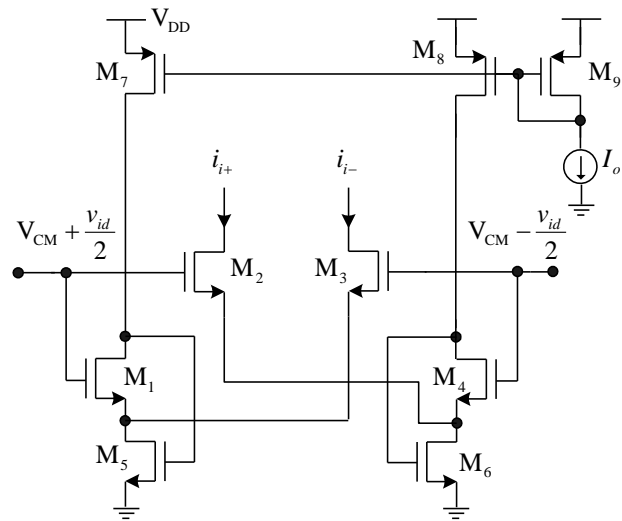


Figure 6

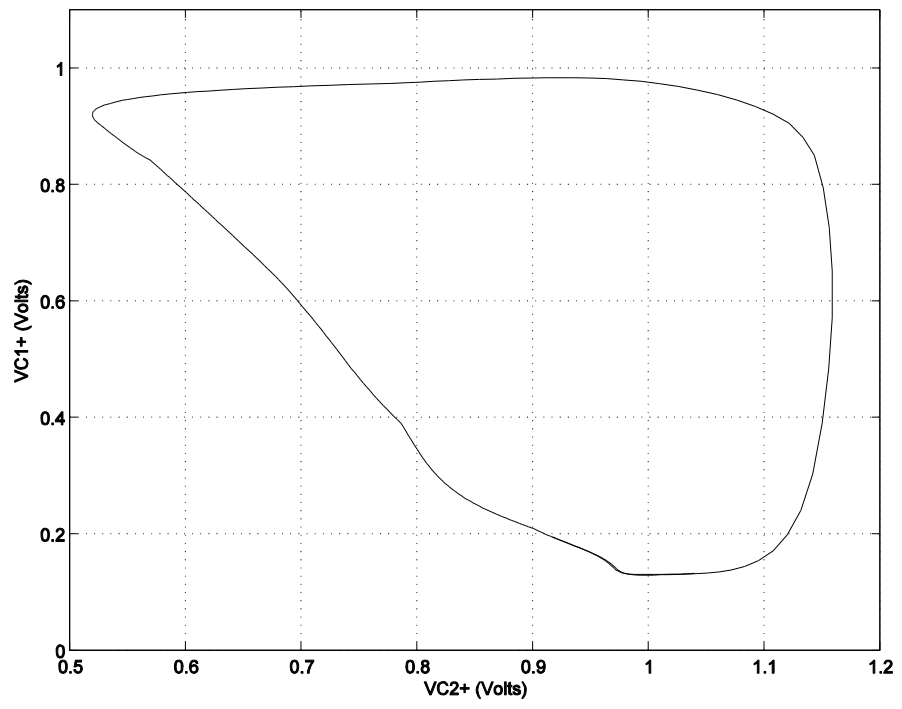


Figure 7

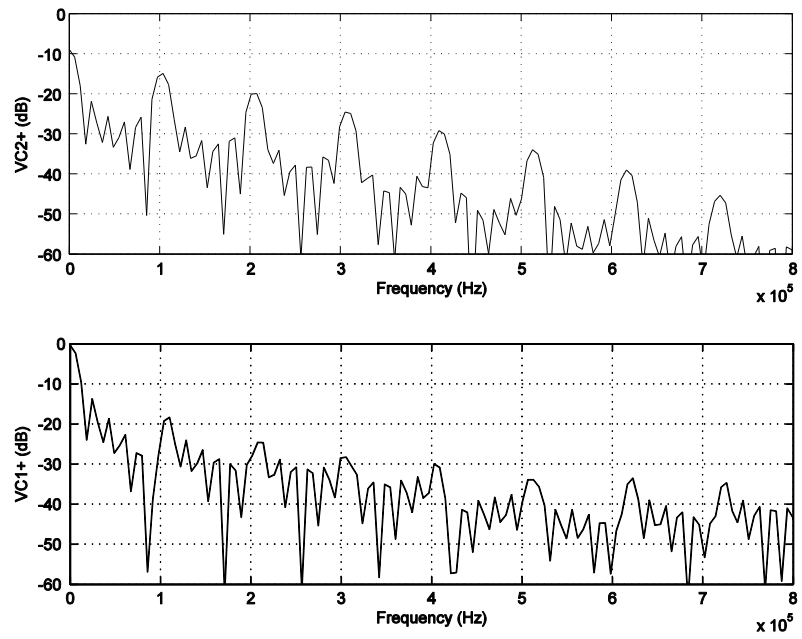


Figure 8

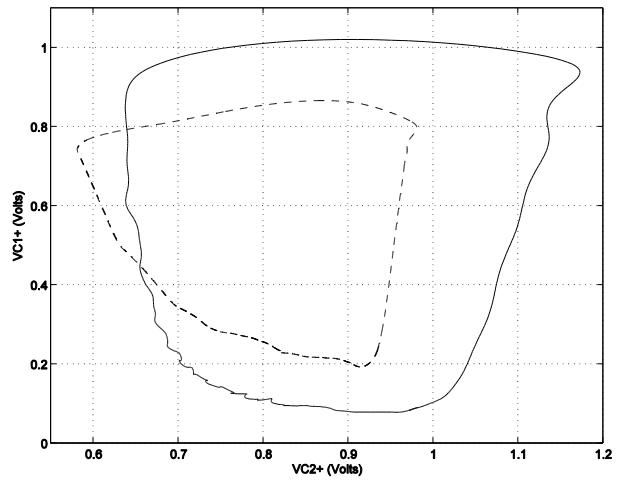


Table caption

Table 1 Aspect ratio of MOSFET transistors in the nonlinear transconductor

Table 1

	M_{1-4}	M_{5-6}	M_{7-9}	M_{10-11}	M_{A-B}
W/L	40/4	160/2.4	64/4	64/2.5	20/10

All aspect ratios are measured in μm . Width and length of transistors M_{iA} , not shown in the table, are equal to those of transistors M_i for $i = 1, \dots, 11$.