

Frequency-Domain Adaptive-Resolution Level-Crossing-Sampling ADC

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Abstract—In the framework of the large-scale wireless sensor networks involved in the Internet-of-Things (IoT), analog-to-digital converters (ADCs) must target ever increasing levels of power efficiency and amenability to ultra-scaled CMOS technologies. Digitally intensive architectures and smart conversion algorithms are therefore the fuel of future ultra-low power (ULP) designs. The minimization of the output average bit-rate is an effective way to maximize the system energy efficiency. Level-crossing-sampling (LC) ADCs are a class of converters that addresses such problem. In their conventional implementation, however, they are mainly impaired by analog blocks (i.e. the high-performance comparators), difficult to be designed in deep nanoscale CMOS. This paper describes a highly-digital frequency-domain implementation of a LC ADC, which replaces the analog comparators with an oscillator-based quantizer and simple digital logic. LC is performed in the digital frequency-domain, where the application of adaptive-resolution algorithms to further enhance power efficiency becomes straightforward. Behavioral modeling simulations demonstrate the appropriateness of the proposed topology by comparing it with the conventional designs and by evaluating the impact of the oscillator-based-quantizer nonidealities on the ADC performance.

Keywords—analog-to-digital converter; level-crossing-sampling; adaptive-resolution; VCO-based quantizer; frequency domain.

I. INTRODUCTION

Within the broad IoT hardware ecosystem, wireless sensor nodes demand the highest possible energy efficiency to extend the battery life. CMOS system-on-chips (SoCs) embed the core functionalities of any IoT device and, as such, all of their building blocks, such as analog readout front-ends, analog-to-digital converters (ADCs), radios and digital signal processors (DSPs), must comply to an ULP design approach as well as adopt nanoscale CMOS technologies to enable inexpensive large-scale integration. An emerging approach for ULP applications is event-based signal processing [1], [2] implemented with time-mode circuits and systems [3]. One of primary concepts of event-based signal processing is level-crossing sampling used in particular for design of analog-to-digital converters [4], and digital filters [5]. The level-crossing-sampling ADCs (LCS-ADCs) are suitable especially for low- to moderate-resolution ULP applications. In LCS-ADCs, an input is sampled when it crosses one of threshold levels, thus resulting in an input-dependent output bit-rate and power consumption [2]. Differently from the more conventional uniform-sampling (US) counterpart, including both Nyquist and oversampled ADCs, the input signal bandwidth in LC is not limited by any sampling clock (indeed, most of LC-ADCs are clockless), oversampling-ratio, and instead the maximum slope of the input signal is limited by the delay of the comparator.

Moreover, most of the environmental physical quantities an IoT sensor node must acquire appear sparsely in the time domain and distribute in a large frequency range. For such input signals, US-ADCs may not represent the most energy efficient alternative, given their almost constant power consumption even during time interval in which no input activity is observed. Therefore, LC-ADCs can reduce the output bit-rate, thus power consumption, for some kinds of natural signals and for a target resolution typically lower than 7 bit [6]. Two common topologies of LC-ADCs are the delta-modulator, shown in Fig. 1a [7], and the flash converter, in Fig. 1b [8].

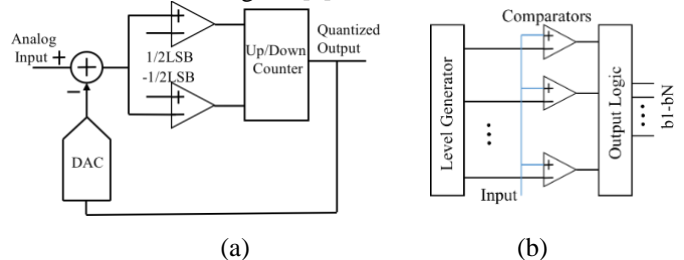


Figure 1: level-crossing sampling delta-modulator (a) and flash ADC (b).

Both of them perform level-crossing with the aid of high-performance comparators, which are often implemented by cascading three or four amplification stages to achieve enough amplification. Due to the low intrinsic gain of transistors in nanoscale CMOS technologies, it is quite hard to design high gain comparators. Furthermore, the regeneration time of such analog comparators is a nonlinear function of their input signal slope, which represents a considerable issue for the overall converter accuracy. The authors in [9] address such drawback by using neutralization capacitors in the gain stages of the comparator preamplifier, while in [7] a method is proposed to adaptively tune the bias current of the comparator in order to properly adjust its delay, which however requires quite complicated control logic and ultimately results in additional power consumption.

Methods to minimize the LC-ADCs power consumption by further reducing the output bit-rate have also been proposed in literature, such as the *derivative level-crossing-sampling* (DLC) [10] and *adaptive-resolution level-crossing-sampling* (AR-LC) [11]. Although both suitable for ULP applications, the former produces low-frequency spectral artifacts which deteriorate the in-band spectral performance of the ADC. Differently from the conventional LC scheme, in which the quantization step (alternatively called *least significant bit*, LSB) is fixed, AR-LC consists in adaptive tuning the LSB depending on the input signal slope. In the original implementation presented in [10], the ADC adopts an input voltage analog slope-detector to properly adjust the ADC quantization step.

This paper introduces for the first time a digitally-intensive implementation of adaptive-resolution level-crossing ADC in frequency domain. The novel architecture proposed, by making use of an oscillator-based quantizer embedded in a delta-modulator loop, avoids the use of analog comparators and slope detectors. Indeed, signal quantization and adaptive tuning of the ADC resolution occur in the digital domain, thus in principle greatly reducing circuit complexity, overcoming the impairments introduced by analog comparators and showing overall amenability to ultra-scaled CMOS technologies.

This work is organized as follows. Section II introduces the proposed frequency-domain AR-LC ADC architecture and discusses the impact of the adopted quantizer nonidealities. Section III describes the Verilog-A behavioural models developed and compares the obtained simulated results with those from a conventional delta-modulator LC-ADC model, so as to verify the appropriateness of the proposed idea. Finally, conclusions are drawn in Section IV.

II. ARCHITECTURE

The architecture of the proposed digitally-intensive AR-LC ADC is shown in Fig. 2.

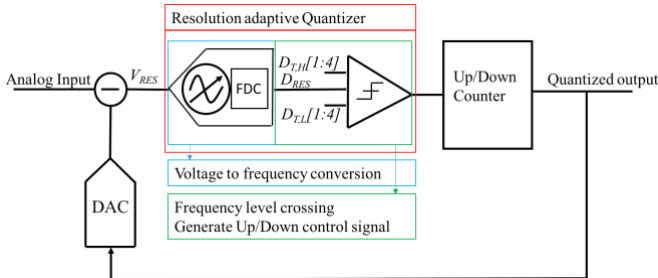


Figure 2: Proposed digitally-intensive AR-LC ADC architecture.

Differently from conventional delta-modulators, in which the voltage residue (V_{RES}) is directly processed by the analog comparators, V_{RES} is first converted into digital frequency information (D_{RES}) using an oscillator-based quantizer (cascade of a voltage-controlled-oscillator, VCO, and frequency-to-digital converter, FDC), and then processed in the digital domain, where the comparator delay is no longer a concern and where the adaptive tuning of the converter resolution is very straightforward. D_{RES} is compared with some upper and lower digital thresholds ($D_{T,H}[1:4]$ and $D_{T,L}[1:4]$ respectively) so as to generate the up/down control signal for the output counter as well as the ADC LSB value associated to the sample being converted, which is variable between 1 and 4 depending on the derivative of D_{RES} , thus exploiting the adaptive-resolution-LC conversion scheme. In the end, the up/down-counter output controls the digital-to-analog converter (DAC) in feedback.

A. VCO-Based Quantizer

The conceptual block diagram of the modelled VCO-based quantizer is shown in Fig. 3. It consists of a conventional N-stage voltage-controlled ring-oscillator (VCRO) and a frequency-to-digital converter, translating the frequency analog information from the VCRO into the digital domain. The FDC adopts the *phase-sampling* topology, first introduced in [12], made of the

cascade of two N-bit digital registers (with no reset), XOR gates and an N-bit adder. Such topology has recently become quite popular for its superior power efficiency compared to the original counter-based implementation [13]. Indeed, it only requires few digital logic cells (XOR gates and flip-flops), available from any CMOS technology standard cells library, and avoids the use high-speed, area- and power-hungry counters.

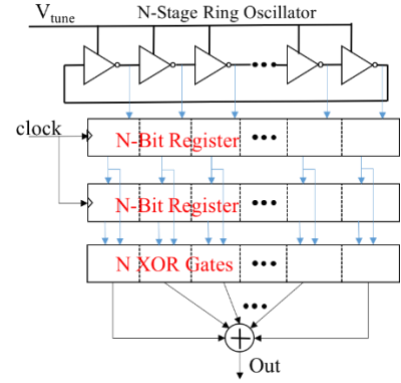


Figure 3: Multi-phase VCO-based quantizer.

The N-bit registers quantize the phase states of the VCRO outputs, while the XOR gates and adder perform a first-order difference of the current and previous phase states, therefore providing a digital representation of the oscillating frequency. It is worth noting that the VCO-based quantizer requires a clock signal, which would not classify the proposed LC ADC as a fully clockless system. However, this would be fundamentally different from a sampled data system (no sampling clock is involved) and it would still classify the proposed ADC as an event-based data converter. Rather than continuous-time (CT)[2], the system operates instead in a pseudo-CT fashion, where the time axis is quantized with a resolution equal to the VCRO clock period (T_S) [2]. Although facing an increase of the output spectrum noise floor (lower accuracy), the great advantage entailed by this topology over true CT systems is that the output data can be stored and processed by conventional mainstream discrete-time DSPs.

The VCO-quantizer output signal $Out[n]$ can be expressed as a function of the oscillator number of stages N , the sampled phase $\theta_{vco}[n]$ and the phase quantization error $\phi_{vco}[n]$ [14]:

$$Out[n] = \frac{N}{\pi} (\theta_{vco}[n] - \theta_{vco}[n-1] + \phi_{vco}[n-1] - \phi_{vco}[n]) \quad (1)$$

Since $\theta_{vco}[n]$ is a function of the VCRO free-running frequency (f_c) and gain (K_v), (1) can be expanded as:

$$\theta_{vco}[n] = 2\pi \int_0^{nT_s} f_c + K_v V_{tune}(\tau) d\tau \quad (2)$$

$$\theta_{vco}[n] - \theta_{vco}[n-1] = 2\pi T_s (f_c + K_v V_{tune}[n]) \quad (3)$$

$$Out[n] = 2NT_s \left(f_c + K_v V_{tune}[n] + \frac{N}{\pi} (\phi_{vco}[n-1] - \phi_{vco}[n]) \right) \quad (4)$$

Apart from the offset contribution given by f_c , the VCO-quantizer conversion gain can be obtained as:

$$A_V = \frac{\partial Out}{\partial V_{tune}} = 2NK_v T_s \quad (5)$$

from which the LSB of the system can be deduced, i.e. the voltage shift of V_{RES} required to increment/decrement by one

count D_{RES} , that indeed is equal to $1/A_V$. Eq. (4) also shows, from the first-order difference of the phase quantization noise in the second term, the inherent quantization noise shaping property of VCO-based quantizers.

The contribution of the VCRO phase quantization noise on the VCO-based quantizer in-band noise power P_n (calculated on a frequency bandwidth equal to f_b) is expressed by Eq. (6) [14]. Although conventional CT LC ADCs that, by design, are not affected by quantization noise, the output spectrum of the proposed frequency-domain LC converter, as mentioned above, exhibits an increase in the noise floor due to the quantization noise power falling in-band. However, as confirmed by simulations in Section III, such quantization noise adds almost insignificantly to the overall converter accuracy (to its *signal to noise and distortion ratio*, SNDR).

$$P_n = 8 \frac{\pi^2 f_b^3 T_s^3}{36} \quad (6)$$

B. Frequency-domain adaptive-resolution LC control logic

In its conventional implementation [10], shown in the block diagram of Fig. 4, the adaptive-resolution LC scheme is exploited using an analog slope detector, whose task is to adjust the quantizer resolution according to which slope threshold has been crossed. AR-LC is instead implemented in [7] using variable comparison windows, i.e. having a wide comparison interval (coarse LSB) immediately after a level is crossed, and decreasing this interval progressively if no further level crossings occur (finer LSB). In our proposed design the residue voltage is converted into a digital frequency information by the VCO-based quantizer, thus allowing the application of the AR-LC scheme by simply increasing the number of comparison thresholds, which is a straightforward and costless operation in the digital domain, requiring only a few control logic gates.

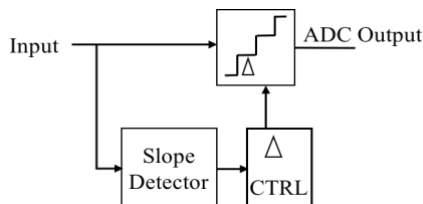


Figure 4: Conceptual block diagram of an AR-LC ADC.

The control logic proposed to exploit adaptive-resolution LC in the digital domain works as follow. The digital frequency information from the VCO-based quantizer is first compared with multiple different levels simultaneously (the above-mentioned digital thresholds $D_{T,H}[1:4]$ and $D_{T,L}[1:4]$ which corresponds to $\pm 1\text{LSB}$, $\pm 2\text{LSB}$, $\pm 3\text{LSB}$ and $\pm 4\text{LSB}$) so as to generate both the up/down control signal and modify the resolution of the 6-bit output counter. For example, if the digital frequency information D_{RES} is equal to 18, an *up* control signal will be generated and the counter incremented by 1 LSB, while if D_{RES} is equal to 20, the counter control signals will make the counter value increment by 2 LSB instead.

III. VERILOG-A BEHAVIORAL MODELING

The Verilog-A behavioral model of the proposed frequency-domain AR-LC ADC has first been compared with that of a

conventional voltage-domain LC delta-modulator (Fig. 1) so as to validate the appropriateness of the proposed idea in terms of accuracy. Afterwards, the impact of the VCO-based quantizer nonidealities (transfer curve nonlinearity and oscillator phase noise) on the performance of the proposed ADC have been assessed, as well as the benefit of the adaptive-resolution algorithm in reducing the output bit-rate.

A. Comparison between voltage- and frequency-domain LC

The model of the conventional voltage-domain LC delta-modulator includes an ideal comparator without delay dispersion, 6-bit up/down counter and ideal 6-bit DAC. The input test signal applied is a 1 V_{pp} 10 MHz sinewave. The simulated output power spectral density (PSD) is presented in Fig. 5, showing an SFDR of 41.04 dB and SNDR of 40.24 dB calculated on a signal bandwidth of 50MHz.

The model of the proposed frequency-domain LC ADC consists of a 31-stage VCRO and the same 6-bit counter and feedback DAC. The outlined parameter set is as follows: $K_v = 1.2 \text{ GHz/V}$, $f_c = 300 \text{ MHz}$ and $T_s = 830 \text{ ps}$. Based on Eq. (5), we can deduce the VCO-quantizer conversion gain to be 62 V^{-1} , which corresponds to 6-bit resolution based on what discussed in section II. The applied input test signal is the same as before, and the output spectrum is also shown in Figure 5.

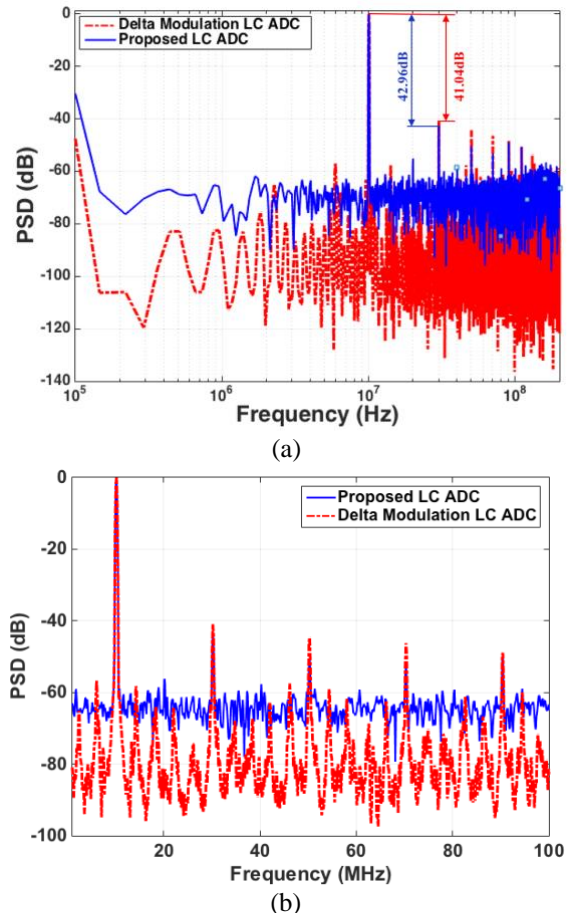


Figure 5: Power spectral density of the digital output of the LC delta-modulator and the proposed LC ADC in log (a) and linear scale (b).

The SFDR of the proposed converter is 42.96 dB, while the SNDR in a 50MHz signal bandwidth is 39 dB. It is worth noting that the noise floor of the conventional LC delta-modulator output spectrum is significantly lower than that of the proposed ADC, because of its true CT operation. Indeed, no discrete-time quantization occurs (which instead involves the phases of the VCRO in our proposed topology) and thus almost no spectral components are present between the signal harmonics. Despite this, the SNDR of both the converters is dominated by harmonic distortion, which ultimately results in comparable performance in terms of SNDR (thus effective resolution).

B. Effect of the VCO-base quantizer nonidealities

To study the impact of the VCO-quantizer voltage-to-frequency (V -to- f) nonlinearity (which is the dominant issue of this class of quantizers) on the performance of the LC ADC, the VCRO V -to- f characteristic is modelled as an 8th order polynomial, whose coefficients are chosen in such a way that HD2 and HD3 are respectively set to -50 and -30 dB, which is a realistic approximation of actual CMOS implementations. Accounting only for the V -to- f nonlinearity, and using the same 1 V_{pp} 10 MHz input test signal, the converter output PSD, shown in Figure 6, exhibits an SFDR of 43.17 dB and SNDR of 38.68dB in a signal bandwidth of 50MHz, thus less than 0.5 dB worse than the case with ideal oscillator (noiseless and perfectly linear VCRO) presented in Fig. 5.

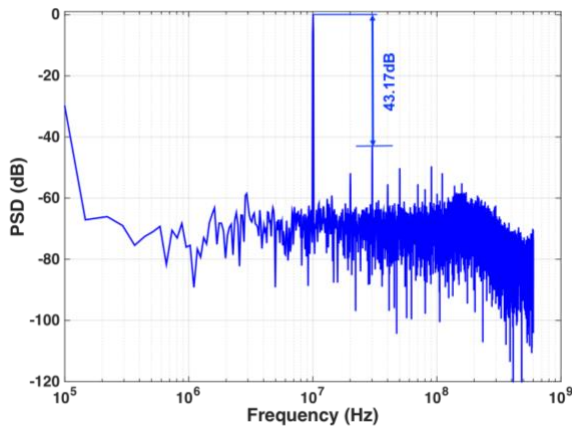


Figure 6: Power spectral density of the LC ADC output accounting for the nonlinear V -to- f oscillator characteristic.

The negligible effect of the VCRO nonlinearity is explained by the fact that the input voltage residue is quite small, thus only a narrow, more linear range of the V -to- f transfer curve is exercised.

In order to assess the impact of the VCRO phase noise (PN) on the performance of the proposed LC ADC, the PN has been modelled as in [14] and [15], considering a single-sided phase-noise PSD of -60 and -90 dBc/Hz at an offset frequency of 100 kHz and 1 MHz respectively, which are also realistic values for actual CMOS implementations of a low-power ring-oscillator. Accounting for only the VCRO PN (perfectly linear VCRO) the ADC output spectrum appears as in Fig. 7. The SNDR in a

signal bandwidth of 50MHz is 38.88dB, which is also less than 0.5 dB worse than the case with ideal oscillator.

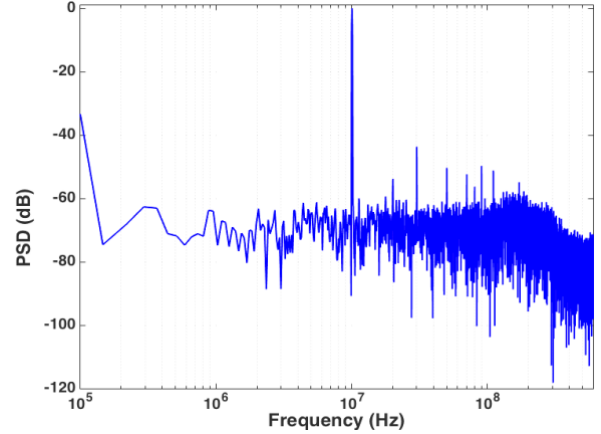


Figure 7: Power spectral density of the LC ADC output accounting for VCRO phase noise.

C. Effectiveness of the AR-LC scheme in the proposed ADC

In order to verify the effectiveness of the adaptive-resolution LC algorithm in reducing the output bit-rate (thus the expected power consumption in a CMOS implementation) without any significant performance degradation, the proposed ADC has been simulated with four different input test signals (same 1 V_{pp} amplitude but frequency of 5, 10, 15 and 20 MHz) with and without the adaptive-resolution LC algorithm enabled. A comparison example between the two cases is shown in Fig. 8 for the 5 MHz input sinewave. As expected, only out-of-band spurious tones are generated by the AR LC scheme. The SNDR in a signal bandwidth of 50MHz is 37.51 and 37.44 dB in the case of adaptive- and fixed- resolution respectively. In the end, Table 1 provides a comparison in terms of output bit-rate of the fixed- and adaptive-resolution LC ADC at the different simulated input frequencies. It can be seen how the AR algorithm improves the system ability to deal with high slew-rate input signals by reducing, for instance, the output bit-rate more than 50% in the case of the highest simulated frequency of 20 MHz.

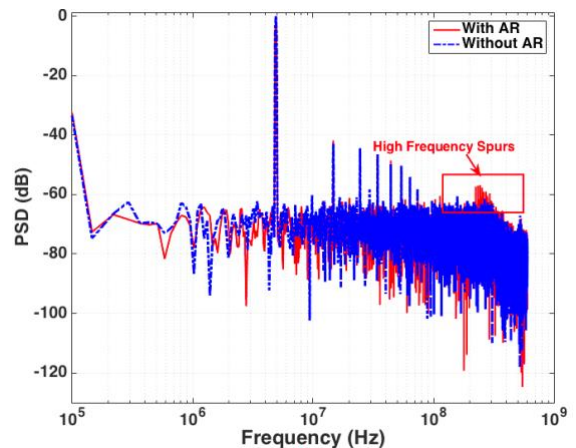


Figure 8: Power spectral density of the LC ADC output with and without the adaptive-resolution algorithm enabled, for a 5 MHz input sinewave.

Table 1: Output bit-rate comparison table

Input frequency [MHz]	Bit-rate without AR [Mbit/s]	Bit-rate with AR [Mbit/s]
5	610	540
10	1220	920
15	1830	1020
20	2400	1000

IV. CONCLUSION

A novel digitally-intensive adaptive-resolution level-crossing-sampling ADC has been proposed, which replaces the analog comparators of conventional voltage-domain LC delta-modulators with a VCO-based quantizer and simple digital logic, thus exploiting AR-LC in the digital frequency domain. In such a paradigm, the ADC resolution can easily be adapted without the need of slope detectors, additional comparators or sophisticated digital logic. It is worth noting that the proposed ADC consumes power even when no signal thresholds are crossed, given the free-running nature of the embedded oscillator. This is however similar to conventional LC-ADCs, in which static power is dissipated because of the comparator reference bias current. Verilog-A behavioral models both of a conventional voltage-domain LC ADC and of the proposed converter have been developed, simulated and compared in order to validate the feasibility of the idea in terms of performance. The effect of the VCO-quantizer nonidealities (V -to- f nonlinearity and oscillator phase noise) on the overall ADC performance has been assessed, suggesting that this architecture is reasonably immune to both (less than 0.5 dB SNDR degradation for the simulated conditions). The application of the AR algorithm has also proved to effectively reduce the converter output bit-rate without any significant in-band performance degradation. We can therefore conclude that, thanks also to its digitally-intensive nature, the proposed frequency-domain AR-LC ADC represents an appealing candidate for nanoscale ULP IoT SoCs, spurring interest in its future CMOS implementation.

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