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Title	A Digitally Controlled Injection-Locked Oscillator With Fine Frequency Resolution
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Publication date	2016-04-13
Publication information	Bashir, Imran, Robert Bogdan Staszewski, and Poras T. Balsara. "A Digitally Controlled Injection-Locked Oscillator With Fine Frequency Resolution." IEEE, April 13, 2016. https://doi.org/10.1109/JSSC.2016.2539342.
Publisher	IEEE
Item record/more information	http://hdl.handle.net/10197/8501
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A Digitally Controlled Injection-Locked Oscillator With Fine Frequency Resolution

Imran Bashir, *Member, IEEE*, Robert Bogdan Staszewski, *Fellow, IEEE*, and Poras T. Balsara, *Fellow, IEEE*

***Abstract*—We propose a digitally controlled injection-locked RF oscillator with an auxiliary loop as an alternative to the conventional capacitive fine-tuning of an LC-tank. The oscillator is injection locked to a time-delayed version of its resonating voltage and its frequency is modulated by manipulating the phase and amplitude of injected current. The injection strength can be programmed for the DCO step size to be as fine as 9 kHz at 4 GHz. Alternatively, with large injection strength, the tuning range can reach up to 200 MHz. The proposed oscillator is experimentally verified in TSMC 40 nm digital CMOS.**

***Index Terms*—All-digital PLL (ADPLL), digital phase rotator (DPR), digital-to-frequency converter (DFC), digitally controlled delay (DCD), digitally controlled oscillator (DCO), multi-stage noise ΣΔ (MASH).**

I. Introduction

RF FREQUENCY modulation that is linear, wideband, and of fine precision, while consuming low power, is an area of intensive research. It is used in many applications, including cellular mobile polar transmitters [1], [2]. Polar transmitters, however, suffer from a unique set of challenges. The frequency modulated (FM) clock is generated by the phase-locked loop (PLL), whose frequency is controlled by analog voltage on a varactor [3] or a digitally controlled capacitor in the LC-tank of a digitally controlled oscillator (DCO) [4]. Irrespective of the implementation, the frequency gain as a function of the input control (continuous or discrete) has to be precisely known or, better yet, constant over the entire FM range for a distortion-free transmission.

One of the earliest implementations of a DCO-based RF digital-to-frequency converter (DFC) is detailed in [4], [20], in which the frequency is modulated by digitally controlling the LC-tank capacitance C. This architecture splits the tracking tuning word, which controls the finest capacitor bank, into integer and fractional parts. The integer part comprises an array of unit-weighted MOS capacitors (unit cells) selected by thermometer row and column decoders. The integer tuning word drives these capacitors directly, after the binary-to-thermometer encoding, while the fractional tuning word is input to a multi-stage noise shaping (MASH) $\Sigma\Delta$ modulator ($\Sigma\Delta$M), which drives one or several unit cells in the capacitor array. The published FM tuning range is 5 MHz at 4 GHz while the finest frequency step size without and with $\Sigma\Delta$M is 40 kHz and 200 Hz, respectively, given the 8 bit fractional tuning word input to the $\Sigma\Delta$M and an $\mathrm{OSR} \geq 16$.

In the above switchable-capacitor implementations, the challenging aspect is keeping the DCO quantization noise low while achieving moderately wide linear FM range. One approach in addressing this challenge is to increase the number of smallest capacitor cells in the array. This complicates the array implementation because increasing the matrix size will require high-order decoders, which in turn would increase routing complexity and would also impact the Q of the LC-tank. The other approach is to increase the unit cell size while shifting the quantization noise away from the carrier into far-out frequencies using the $\Sigma\Delta$ modulator. In this scenario, the peak of the quantization noise ("noise bump") at the DCO output is located at $f_{\Sigma\Delta}/2$ which is half the $\Sigma\Delta$ clock frequency. This noise bump may end up in the receive band or, worst case, at the duplex receiver channel, if implemented for a full duplex system, and therefore will limit the local receiver sensitivity [5]. Because the noise bump increases with the unit cell or the smallest capacitor size, this issue will only get exacerbated.

Kodama *et al*. [7] offers a possible solution to this challenge by applying a pulse width modulation (PWM) to the capacitor on/off control signal. In that topology, the effective capacitance seen by the LC-tank can be reduced by controlling the duty cycle of the control signal. Compared to [4], the architecture in [7] can achieve wider FM tuning range with fewer cells in the capacitor array, thus reducing the impact on Q of the LC-tank while the extra resolution gained with the PWM scheme can eliminate the need for a $\Sigma\Delta$ dithering of the unit capacitor. However, the reported frequency resolution of 270 kHz is not adequate for most wireless applications. This issue was addressed in [8], which achieves very fine frequency resolution with capacitive degeneration while avoiding the need for the $\Sigma\Delta$ dithering. Compared to [7], that architecture can achieve a resolution of 150 Hz and total tuning range of 12 MHz. However, there is a strong trade-off between the step size, linearity, and tuning range.

Another approach for attaining reasonable DFC quantization and total FM range is through segmented capacitor banks, as demonstrated in [9]. In that design, the capacitor bank for FM

Manuscript received June 29, 2015; revised February 28, 2016; accepted March 01, 2016. Date of publication April 13, 2016; date of current version June 09, 2016. This paper was approved by Associate Editor Jack Kenney. This work was supported in part by European Union ERC Consolidator Grant 307624.

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Digital Object Identifier 10.1109/JSSC.2016.2539342

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is split into three segments. The most significant bit (MSB) of coarse segment consists of 128 thermometer coded capacitors each having a step size of 1.95 MHz/LSB. These capacitors are laid out in a 16 by 8 array and cover a frequency range of 250 MHz. The next segment has 16 thermometer coded elements that are 1/16th the size of the coarse unit cell and therefore have a step size of 120 kHz/LSB. The last segment has three additional capacitors driven by a 6 bit MASH $\Sigma\Delta$ to increase the resolution of the frequency modulator to 1.875 kHz. While [9] demonstrates a DCO capable of achieving wide FM range, the published data also shows high differential non-linearity (DNL) among capacitors and between coarse and fine segments of the capacitor banks. If not designed properly, the DCO frequency step can be non-monotonic (or overlap) over the segment boundary. All these impairments will impact the spectral purity of the FM signal.

Another variant of a switched-capacitor array implementation [10] uses incrementally sized capacitors instead of binary or thermometer weighted capacitors. While [4] and [9] employ thermometer encoding to select the number of capacitors in an array, this topology uses a one-hot coding in the fine capacitor bank to select only one capacitor at a time. The capacitor bank comprises 32 unit cells with capacitance of $C_0 + i \cdot \Delta C$ and transistor size of $W_0 + i \cdot \Delta W$ where i is the capacitor index. The limit on the smallest transistor size W_0 is far more stringent than the limit on the increment to the transistor size ΔW, and therefore the capacitor bank can be designed to achieve a very small step size. The coarse capacitor bank is also designed by incrementally changing capacitance in the LC-tank by a factor $N \cdot \Delta C$. Therefore, between the consecutive tuning codes, the capacitance increases monotonically and any discontinuity or overlap between the coarse and fine banks is avoided. The published fine frequency step size in [10] is 5 kHz with a total tuning range of 10.24 MHz. While the fine frequency step size is competitive, the published results show poor DNL.

So far, the discussion has been focused around DCOs with the switched capacitor array. Another class of DFC uses the injection-locking technique to tune oscillator frequency. One such implementation is detailed in [11]. That circuit is also known as a quadrature VCO in which two oscillators are cross coupled such that once the system is injection locked, the pair generates quadrature phases. In this implementation, the frequency tuning is generated by modulating the coupling strength between the two oscillator cores through an analog voltage. That continuous-time and continuous-amplitude architecture can achieve linear tuning range of 60 MHz. However, any mismatches in the two oscillators also limit the performance by introducing quadrature phase error. Lastly, [12] employs injection locking for frequency generation at millimeter wave frequencies. However, that solution is not practical for digitally intensive transmitters operating at RF frequencies.

II. Proposed Solution

In this work, we propose to exploit injection locking of an oscillator using an auxiliary loop[1] to perform the frequency modulation. As shown in Fig. 1, the LC-tank of the DCO,

[1]It could also be viewed as *self* injection locking.

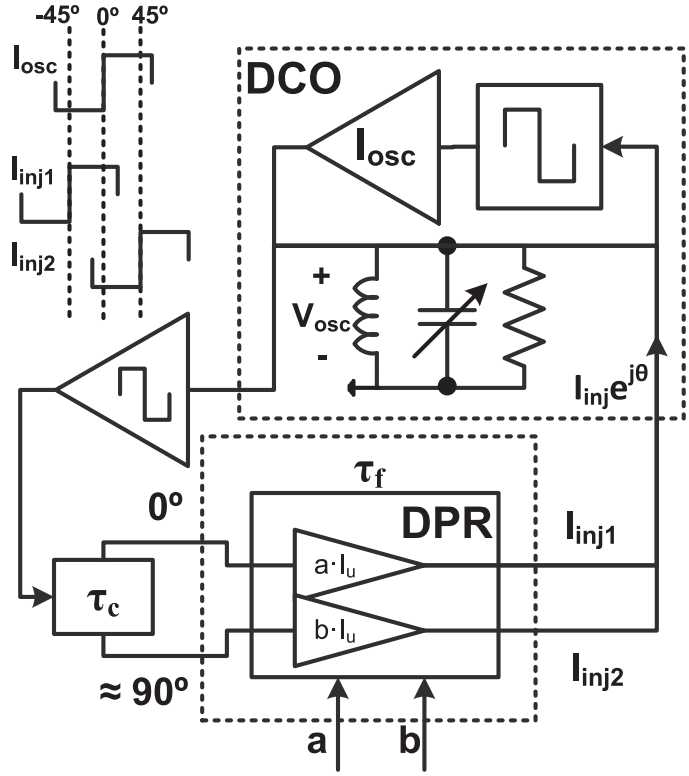


Fig. 1. Principle of wideband frequency modulation through injection locking and block diagram of its realization.

whose free-running frequency $\omega_0 = 2\pi f_0 = 1/\sqrt{LC}$ is set by the switchable capacitor C and the fixed inductor L, is injected with a delayed version of its own resonating waveform. The resulting frequency $\omega_{\text{out}} = 2\pi f_{\text{out}}$ under such conditions is given by Adler's equation [13]:

$$\begin{aligned}\omega_{\text{out}}\left[n \cdot t_{sH}\right] &= -\frac{\omega_0}{2Q} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \sin\left(\theta\left[n \cdot t_{sH}\right]\right) + \omega_0 \\ &= -\frac{\omega_0}{2Q} \cdot I_r \cdot \sin\left(\theta\left[n \cdot t_{sH}\right]\right) + \omega_0 \qquad (1)\end{aligned}$$

where Q is the LC-tank quality factor, I_{osc} is the peak oscillator current, I_{inj} is the peak injected current into the LC-tank, and t_{sH} is the sampling time interval of the DFC (determined by f_{sH}). For notational simplicity, $I_r \equiv I_{\text{inj}}/I_{\text{osc}}$. θ is the steady-state phase between I_{osc} and I_{inj} which implies that the system is injection locked. By dynamically manipulating the delay of the injected signal and consequently $\theta[n \cdot t_{sH}]$, the steady-state oscillator frequency $\omega_{\text{out}}[n \cdot t_{sH}]$ varies according to (1). Within a reasonable range of θ around 0°, ω_{out} increases linearly with θ.

The oscillation frequency ω_{out} sensitivity to the injecting phase θ is a partial derivative of (1):

$$\frac{\partial \omega_{\text{out}}}{\partial \theta} = -\omega_0 \cdot \frac{I_r}{2Q} \cdot \cos(\theta). \qquad (2)$$

If θ is controlled in finite steps $\Delta\theta$, then the frequency control will be quantized with steps $\Delta f_{\text{out}} = \Delta\omega_{\text{out}}/2\pi$:

$$\frac{\Delta f_{\text{out}}}{\Delta \theta} = -f_0 \cdot \frac{I_r}{2Q} \cdot \cos(\theta). \qquad (3)$$

We can safely assume $\cos(\theta) \approx 1$. The objective of our work is to make $\Delta\theta$ uniform and fine enough such that $\Delta f_{\rm out}$ is on the order of kHz, which will make it attractive for RF wireless systems as a practical replacement of the aforementioned $\Sigma\Delta$ dithering of DCO varactors [20], [4]. Note that $\Delta f_{\rm out}$ step size is also termed the DCO gain, $K_{\rm DCO}$ [4], [9], [18], [20]. The step size $\Delta f_{\rm out}$ is directly proportional to $I_r = I_{\rm inj}/I_{\rm osc}$ and inversely proportional to Q. Considering Q typically in the range of 8–30 in practical wireless systems (here, $Q = 12$), a kHz level resolution of a GHz level carrier implies the phase step $\Delta\theta$ must be about 5 orders of magnitude below its full extent (i.e., 360°), which is quite feasible by using Cartesian addition of two orthogonal vectors, as will be elaborated later.

The maximum variation of $\omega_{\rm out}$ about ω_0, for which the DCO is injection locked, is limited by the injection-locking range ω_L given by the following equation:

$$\omega_L = \omega_0 \cdot \frac{I_r}{2Q}. \tag{4}$$

Consequently, to support wideband (WB) modulation, I_r should be maximized, especially when Q is high, in order to reach the sufficient ω_L. For narrowband (NB) modulation, I_r needs to be scaled down in order to obtain the sufficiently fine $\Delta f_{\rm out}$, as per (3), while keeping the adequate ω_L, as per (4). It should be emphasized that the tank-Q is highly constrained in the CMOS technology and can maximally reach 8–30 depending on metallization and substrate properties as well as area and power constraints in practical transceivers. For this reason, the foremost objective should be to maximize the tank-Q within the above constrains in order to obtain the best phase noise for the lowest current consumption. Then, I_r can be freely adjusted for the required locking range and step size.

The phase adjustment θ of the injected signal is performed in two steps. The first step is coarse and performed by the phase generator block represented by τ_c in the block diagram in Fig. 1. This circuitry also generates approximately quadrature signals that are used by the digital phase rotator (DPR), represented by τ_f, to perform a fine phase adjustment via Cartesian vector addition. The DPR generates two orthogonal currents $I_{\rm inj1}$ and $I_{\rm inj2}$ that are injected directly into the oscillator core while the interpolation is performed by the LC-tank such that $I_{\rm inj}$, the Euclidean vector sum of $I_{\rm inj1}$ and $I_{\rm inj2}$, is injected at a phase θ with respect to the DCO current $I_{\rm osc}$. The phase delay due to τ_f varies about a mean phase which is determined by the blocks in the auxiliary feedback path including τ_c and is typically set to 0° (i.e., equivalent to 360° or multiples thereof). The signals that steer the injected currents are derived from the DCO, so the system is fully synchronous to $\omega_{\rm out}$. The interpolated phase is a function of the ratio of currents $I_{\rm inj1}$ and $I_{\rm inj2}$, which is controlled by the digital codes a and b. The magnitude of the injected current $I_{\rm inj}$ is controlled by the unit cell current I_u and the digital code a and b. The linear frequency tuning range is determined by ω_L, which is proportional to I_r. Both $I_{\rm osc}$ and $I_{\rm inj}$ are digitally controlled and therefore the DCO gain (Hz/LSB) and the linear FM tuning range can be scaled according to the desired application. This is the strongest feature of this architecture when compared to [4], [7], [8], and [11]. However, the linear FM range is inversely proportional to Q which has to be high (i.e., 8–30) for reasonable phase noise performance and consequently I_r has to be scaled to achieve the desired tuning range.

III. FM Modulation Using Injection-Locking

A. Numerical Model of a Conventional Injection-Locked Oscillator

The various modes of an oscillator tank under the influence of an external signal, as detailed in [13], can be studied by numerically modeling the circuit shown in Fig. 2(a) [14]. We will use this model to study important trends before describing the main idea behind our work. Of particular interest is the behavior of the oscillator signals, shown in Fig. 2(b), when the injected signal is within the injection-locking range. The model is developed in Simulink and the following parameters are used: $I_{\rm osc} = 1$ mA, $f_o = 4.5$ GHz, $Q = 10.6$, $L = 0.85$ nH, $C = 1.5$ pF.

In that regime, the oscillator injection-locks to the incident signal and so $\phi(t)$ and $\theta(t)$ become constant after a short settling time. In Fig. 2(d), the phases $\phi(t)$ and $\theta(t)$ are plotted as the injection frequency $f_{\rm inj}$ is varied over and beyond the injection-locking range. The injection strength I_r is set to 0.8. The regions when the oscillator is injection locked or injection pulled are annotated on the plot. Notice that when the oscillator is injection locked, the phases $\phi(t)$ and $\theta(t)$ vary linearly as a function of $f_{\rm inj}$. Both $\phi(t)$ and $\theta(t)$ cross the origin around $\omega_0/2\pi = 4.5$ GHz which is the resonance frequency of the LC-tank. The oscillator is injection locked over a range of 400 MHz around 4.5 GHz. The next step is to study the effect of I_r and variation of $\theta(t)$ over this lock range.

As shown in Fig. 2(c), θ varies linearly with $f_{\rm inj}$ over a range determined by ω_L which is proportional to I_r. The slope of θ with respect to $f_{\rm inj}$ decreases with increasing I_r. The injection-lock range varies from 200 MHz, 400 MHz, and 600 MHz for I_r values of 0.5, 0.8, and 1.0, respectively. This plot is very critical in understanding the main concept behind this work. In Fig. 2(c), $f_{\rm inj}$ is the independent variable that determines θ, while in our work, θ is the independent variable or forcing condition that determines the steady-state frequency of the oscillator. The values for I_r and Q are chosen arbitrarily to show the extent of FM bandwidth theoretically possible with an injection-locked oscillator. The trends observed from this model are the same for the targeted value of $I_r = 0.15$ which results in a narrower linear FM range.

B. Numerical Model of a Self Injection-Locked Oscillator

After the brief overview of the injection-locking theory, the next step is to describe the self injection-locked oscillator. It is an extension of our work presented earlier in [15], which can be used as a proof of concept of our main idea. As shown in Fig. 3, a digitally controlled delay (DCD) is inserted between the oscillator and pre-power amplifier (PPA) to mitigate the parasitic FM modulation due to injection pulling induced by amplitude modulation (AM) applied to the PPA. In this case, the argument in the sine function in (1) is adjusted to 0° or multiples of

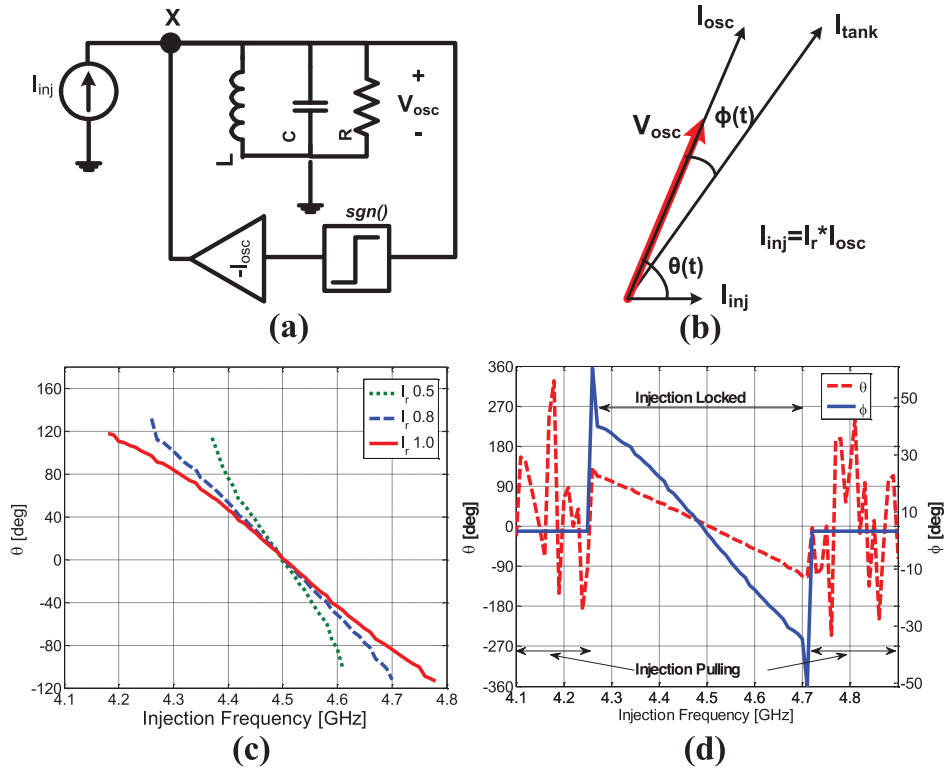


Fig. 2. (a) Numerical model of an injection-locked oscillator [14]. (b) Phasor representation of the signals. (c) θ versus injection frequency $f_{\rm inj}$ at various I_r settings. (d) $\phi(t)$ and $\theta(t)$ versus injection frequency $f_{\rm inj}$.

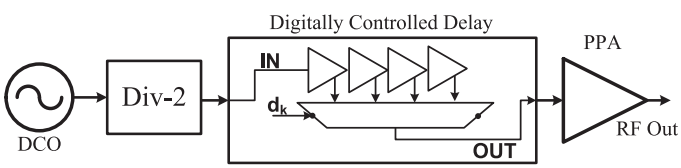


Fig. 3. Digitally controlled delay to mitigate injection pulling due to amplitude modulation (AM) of the pre-power amplifier [15].

180° in order to reduce the injection pulling and to ultimately improve the transmitter performance. The same argument can be used backwards, i.e., if a system can be designed such that the extent of injection pulling can be decreased by adjusting the phase between the aggressor (PPA) and the victim (DCO), then it should also be feasible to control the extent of frequency modulation (not parasitic but purposefully induced in this case) by adjusting the phase between the aggressor and victim. The aggressor need not be a power amplifier and can be the oscillator signal itself. In [15], the injection path was parasitic. In this work, the injection is induced by directly coupling the injected signal in a controllable way.

Fig. 4(a) shows a Simulink model of an injection-locked oscillator based on [14] with a critical difference denoted by the dash-line box labelled "Auxiliary Loop." Four currents are summed at the input of block $R_{\rm tank}$. These currents are from the capacitor, inductor, commutating transistor pair, and injecting circuit. The modification in this model compared to [14] exploits the injection-locking phenomenon as a way to generate FM. Instead of using an independent signal source, the injected signal is directed from the oscillator output and phase delayed by a certain time interval. This essentially creates a auxiliary feedback path in the oscillator, the delay of which is varied in order to change the oscillating frequency. I_r in Fig. 4(a) scales the peak injection current $I_{\rm inj}$ with respect to $I_{\rm osc}$ and can also be used to vary the linear FM range or ω_L.

C. Simulation Results from Numerical Model

Given that the oscillator is injection locked, the final oscillating frequency is given by (1). The argument θ in that equation will be modulated in the model shown in Fig. 4(a). A transient simulation with 500k samples is run in small increments over a range of θ that exceeds $\pm 100°$. $I_{\rm osc}$ is 1 mA, $Q_{\rm tank}$ is 10.6, $L_{\rm tank}$ is 0.9 nH, and $C_{\rm tank}$ is 1.4 pF.

Fig. 4(b) shows the simulation results with $I_r = 0.5$. A few important observations are noted here. The oscillating peak voltage $V_{\rm osc,pk}$ reduces as the oscillator is steered away from the resonant frequency ω_0. This loss of amplitude will result in a degradation of the DCO phase noise. The variation in $V_{\rm osc,pk}$ increases with the injection strength. The auxiliary feedback path that is phase delayed by θ in Fig. 4(a) will act as a positive feedback and hence augment or amplify the oscillation signal only when θ is $\sim 0°$. At other values of θ, the feedback will impede the main oscillation. When θ approaches 180°, this feedback becomes negative and, if strong enough, it can stop the oscillation altogether. This is especially true for the cases when I_r is close to 1. This limitation, however, is not a cause for concern here for two main reasons. First, I_r targeted in this work is around 0.15. Also, the target range for θ is $\pm 45°$, which,

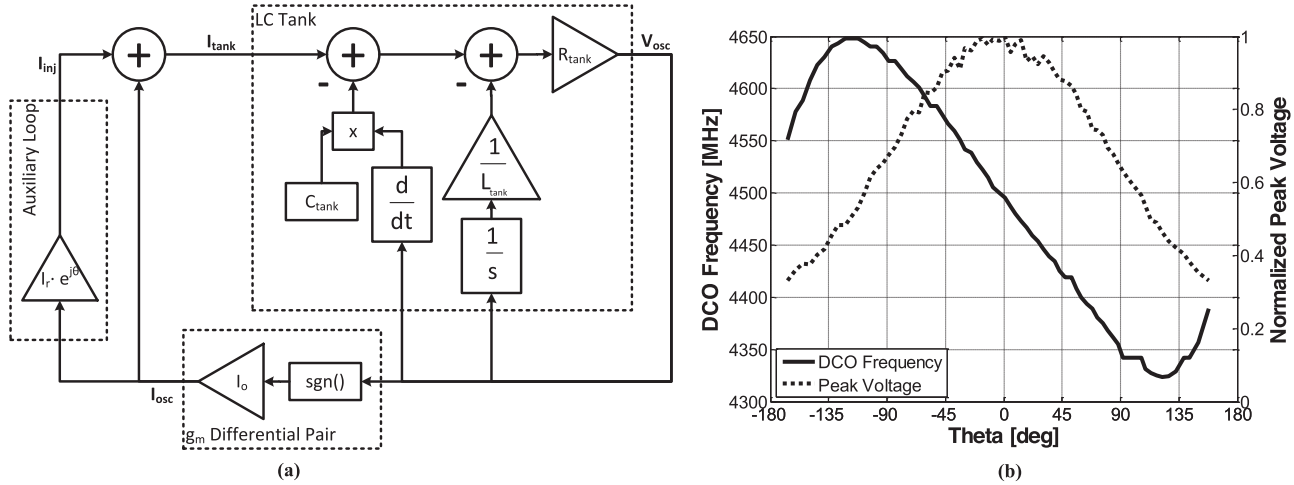


Fig. 4. (a) Numerical model of an injection locked oscillator with an auxiliary loop. (b) Simulation results of injection-locked DCO frequency and peak voltage versus θ.

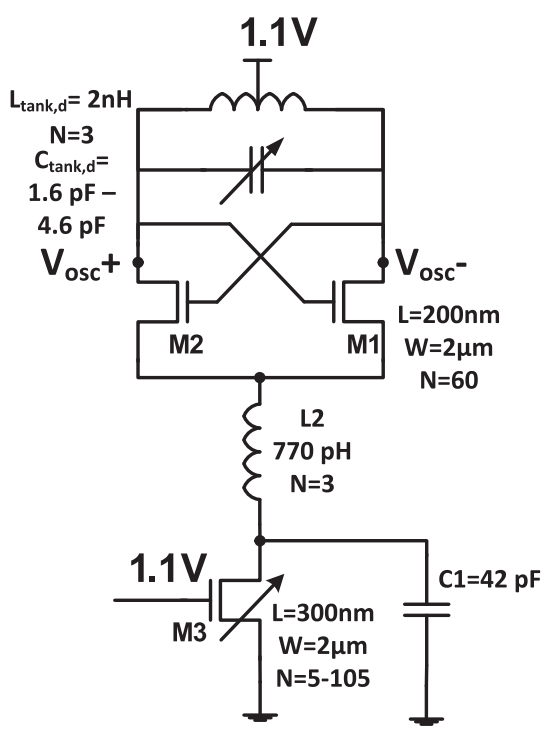


Fig. 5. Digitally controlled oscillator core.

according to Fig. 4(b), is where the oscillator tuning range is linear and the variation in $V_{\mathrm{osc,pk}}$ is small. The output of the DCO is sourced from the preceding buffer stage which acts like a hard limiter and therefore any parasitic AM due to "peak voltage" curve in Fig. 4(b) will be removed.

IV. Circuit Design

A. Digitally Controlled Oscillator

The top-level circuit diagram of the DCO is shown in Fig. 5. The DCO core supply is 1.1 V. The differential tank inductance is 2 nH while the differential tank capacitance is digitally controlled between 1.6 pF and 4.6 pF. The M3 NMOS transistor operates in a triode region with channel resistance digitally controlled based on the number of transistors turned on. The fact that M3 operates in triode necessitates the placement of L2 [16]. Capacitor C1 is maximized in order to filter any noise from the current sink that can up-convert due to the switching action of M1 and M2 and degrade oscillator phase noise. The LC-tank comprises the inductor and binary weighted MOM capacitors controlled via an 8 bit digital input.

B. Phase Generator

The block diagram shown in Fig. 6(a) is the auxiliary loop that comprises the phase generator and the DPR. Proper design of the auxiliary loop is essential for the frequency tuning of the DCO. The principle function of this auxiliary path is to generate a phase delayed version of the oscillator output such that I_{inj} forms an angle θ with I_{osc} as shown in Fig. 4(a). The angle θ is generated by the delay stages in the phase generator block and the DPR and is described by

$$\theta(n \cdot t_{sH}) = \theta_c(\tau_c) + \theta_f(n \cdot t_{sH}) \tag{5}$$

$$\theta(n \cdot t_{sH}) = \theta_c(\tau_c) + tan^{-1}\left(\frac{b(n \cdot t_{sH})}{a(n \cdot t_{sH})}\right) \tag{6}$$

where θ_c (coarse phase) is generated by the delay stage τ_c in the phase generator block and the θ_f (fine phase) is adjusted by the DPR through control words a and b (to be covered in Section V). As shown in Fig. 6(a), the oscillator voltage V_{osc} is converted to a square-wave clock by the oscillator buffer. The clock is controllably delayed by the coarse delay circuit τ_c, which produces two output clocks VI0 and VI90 with approximately quadrature phase relationship. These two clocks are then fed to the DPR, which creates synchronous current pulses I_{inj1} and I_{inj2} with gains controlled by the digital steering signals a and b. The two currents are summed and injected as I_{inj}, with phase θ, back into the oscillator tank. Fig. 6(b) shows the waveforms of the I_{inj1} and I_{inj2} currents injected into the LC-tank. The pedestal in $I_{\mathrm{inj}} = I_{\mathrm{inj1}} + I_{\mathrm{inj2}}$ is due to the phase shift between VI0 and VI90 signals. The level of the pedestal

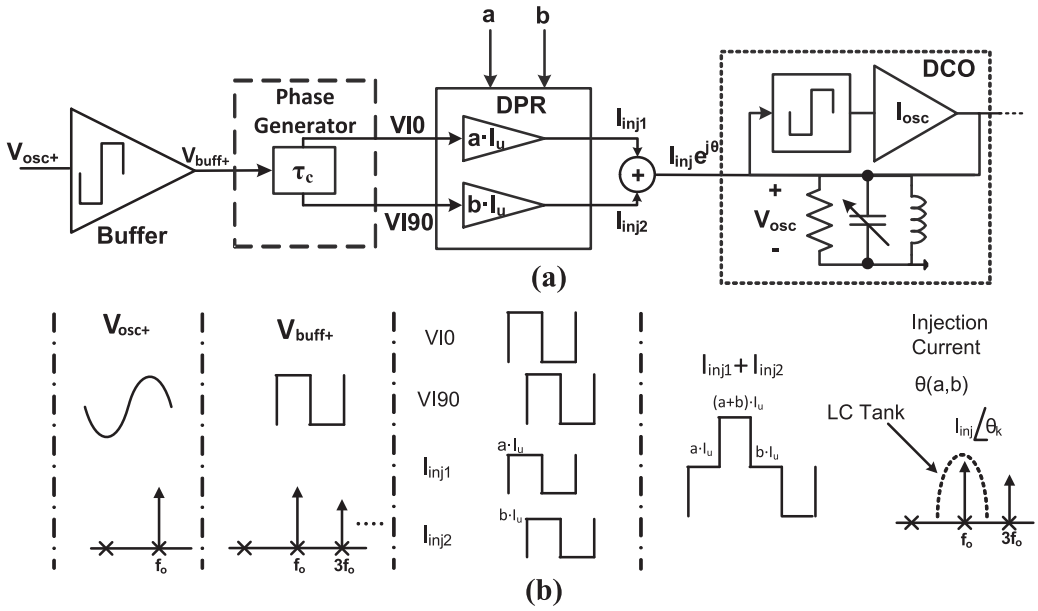
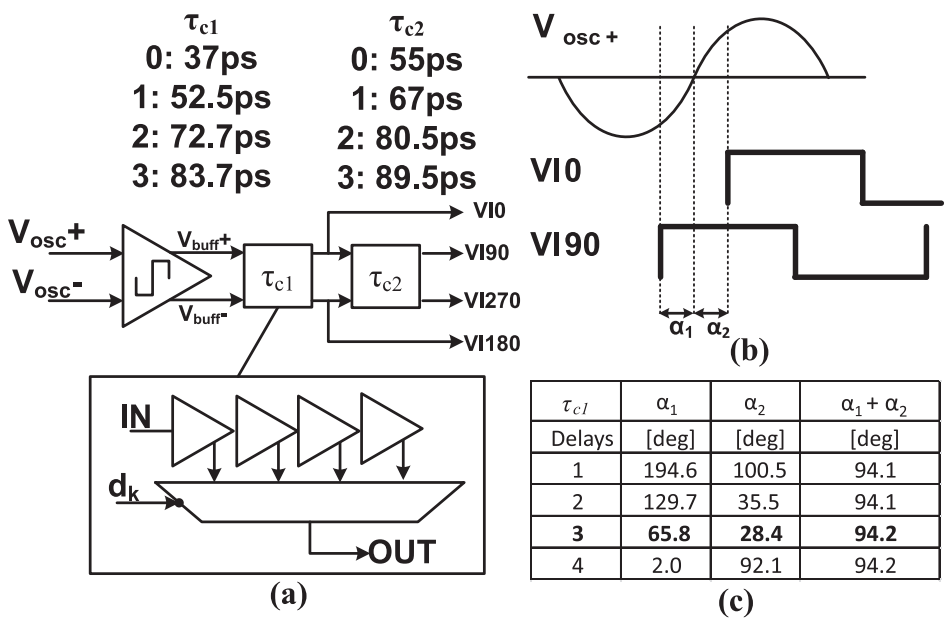


Fig. 6. (a) Block diagram of the auxiliary loop. (b) Time and frequency domain representation of various signals in the circuit.



τ_{cl} Delays	α_1 [deg]	α_2 [deg]	$\alpha_1 + \alpha_2$ [deg]
1	194.6	100.5	94.1
2	129.7	35.5	94.1
3	**65.8**	**28.4**	**94.2**
4	2.0	92.1	94.2

Fig. 7. (a) Phase generator schematic diagram. (b) Phase relationships between various signals. (c) Transient simulation results.

is determined by the number of current cells turned on in the DPR array via a and b. The current injected into the DCO is band-pass filtered by the LC-tank. Therefore, higher harmonics injected into the DCO do not severely impact the circuit's operation. The LC-tank also serves as the interpolator that averages between the VI0 and VI90 phases based on the weights determined by controls a and b.

Now, assume that the LC-tank of the oscillator is tuned to a frequency of 4.2 GHz. According to Fig. 6(a), the auxiliary path delay comprises the oscillator buffer, phase generator, DPR, and interconnects. The delay due to interconnecting wires can be ignored since the entire circuitry is located within a small area. At a frequency of 4.2 GHz, the simulated oscillator buffer delay is 17.3 ps (26.2°). The delay of the phase generator is 72 ps (108.8°). A 180° phase arises due to inversion inside the DPR current steering cell. At mid code setting of the DPR DAC, the current controls a and b are equal and therefore θ_f from (6) is 45°. This brings the total phase delay in the auxiliary path to 360°. Consequently, θ is zero, $I_{\rm inj}$ is in phase with $I_{\rm osc}$, and according to (1), the oscillator frequency ($\omega_{\rm out}$) is ω_0. In order to vary $\omega_{\rm out}$ around ω_0, θ_f is tuned between 0° to 90° by adjusting control words a and b in the DPR while the maximum possible variation of $\omega_{\rm out}$ is defined by ω_L in (4). Under such condition, τ_c is considered to be proper set and it also ensures that the low-to-high transitions on VI0 and VI90 happen around the 0° phase of oscillator output voltage $V_{\rm osc+}$ as shown in Fig. 7(b). The upper and lower limit of the interpolated phase (θ_f) is determined by VI0 and VI90 signals and

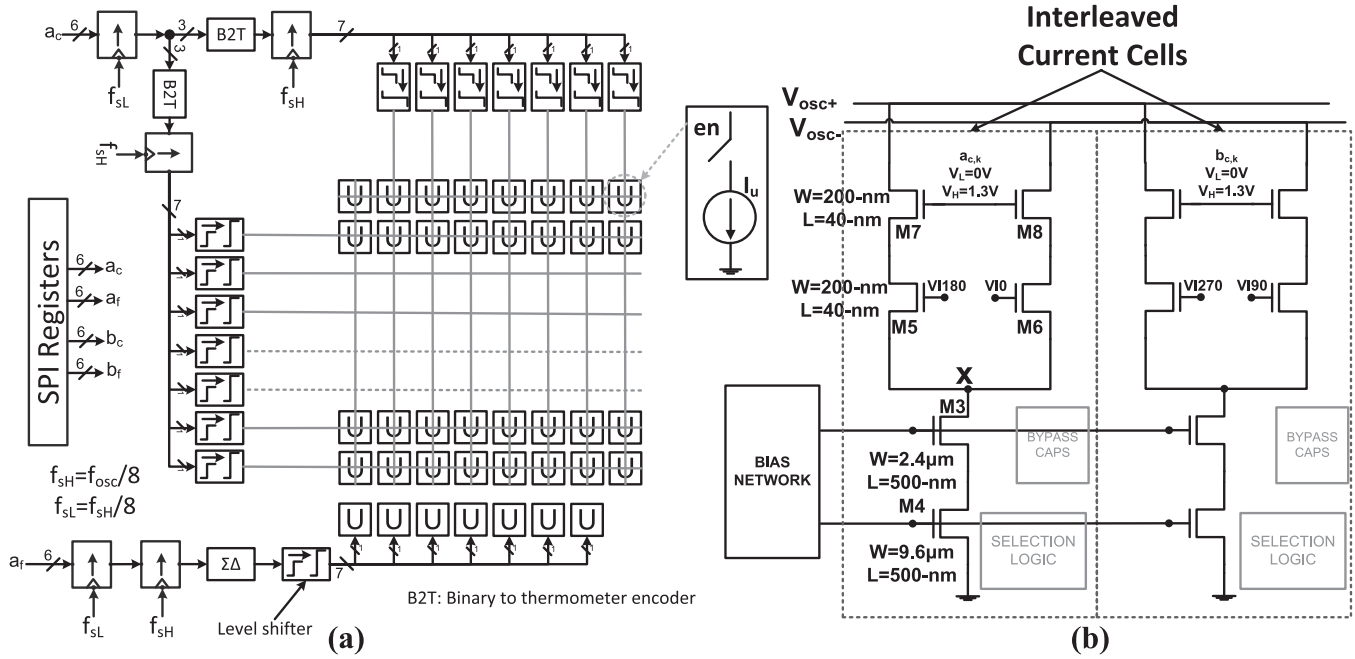


Fig. 8. (a) DPR diagram and signal flow for the current control word a. (b) DPR unit current cell schematic diagram.

with proper setting of τ_c, the injected phase lands in the linear θ-to-ω_{out} conversion region shown in Fig. 4(b). Also note that the discussion so far has been in the context of NB FM modulation because θ is a linear function of θ_f only under such condition.

Details of the coarse delay line are shown in Fig. 7(a). It cascades two digitally controlled coarse delay lines τ_{c1} and τ_{c2}. The phase delay in the auxiliary feedback loop has to be 360° across the DCO LC tank tuning range. If the LC tank is tuned for lower frequencies, additional delay stages within τ_{c1} are engaged and vice versa. τ_{c2} is designed to generate the 90° phase shift between VI0 and VI90 signals. The phase delay will vary over the oscillator's frequency range, process, supply, and temperature. Therefore, τ_{c1} has to be calibrated. A well-regulated circuit supply will ensure limited voltage variation over time. Simulations show a 2 ps delay variation in each stage over temperature (−40°C to 85°C), which implies, according to (4), that θ will have an offset (from 0°) when DPR DACs are at mid code. Consequently, the linear FM range may be reduced, however, the behavior of inverter delay with respect to temperature is linear and well characterized. Therefore, such offsets can be removed by monitoring the IC temperature and adjusting the number of delay stages τ_{c1} based on an empirical model. Fig. 7(c) shows the simulated phase difference between VI0/VI90 and $V_{\text{osc}+}$ signals. For proper operation of the DPR, the phase difference between VI0 and VI90 should be approximately 90°. The aforementioned conditions are satisfied according to the simulation result in Fig. 7(c) when three delay stages at 4 GHz are engaged in the τ_{c1} block.

C. Digital Phase Rotator

The DPR [17] interpolates between the signals generated by the phase generator block discussed in Section IV-B. A simplified top-level diagram of the DPR block is shown in Fig. 8(a). The DPR circuit is essentially two interleaved current-steering DACs with mutually exclusive selection of current sources. Interleaving the current cells minimizes the mismatch between the two DACs; however, the routing becomes more complex. The DPR array comprises 64 unit cells controlled by coarse control words a_c and b_c and 7 unit cells controlled by fractional control word a_f and b_f through a MASH ΣΔ stage. Each unit cell contains two current-steering cells, one for each interpolating vector VI0 and VI90 (and their respective differential phases). The output currents are summed at nodes $V_{\text{osc}+}$ and $V_{\text{osc}-}$ and injected into the LC-tank of the DCO.

The current control word a is split into a 6 bit integer word a_c and a 6 bit fractional word a_f. The control word a_c is further split in the DPR array into 3 bits for row selection and 3 bits for column selection. These portions are thermometer encoded and passed through a level shifter before being passed into the unit cell U of the DPR array. The fractional word a_f is applied to a MASH ΣΔ converter. The 7 bit output of the ΣΔ converter is level shifted and then applied to the DPR unit cells. Current control word b is configured in the same manner. For the NB FM case, if the DCO frequency resolution is high enough to meet the spectral mask requirements, the ΣΔ converter may not be needed. Therefore, any impairments originating from ΣΔ processing, such as mismatch between coarse and fine unit cells, etc., may not be relevant.

The digital portion of DPR block samples the current control settings a and b from the SPI registers. The SPI registers are latched by an external clock, which is asynchronous to any clocks derived from the DCO. Therefore, in the first stage, the a and b integer and fractional words are sampled by f_{sL} which is derived from DCO clock. The integer control bits are then split and thermometer encoded. In the next stage, the integer and fractional words are up-sampled by f_{sH}. This clock also drives the MASH sigma-delta converters and the DPR array.

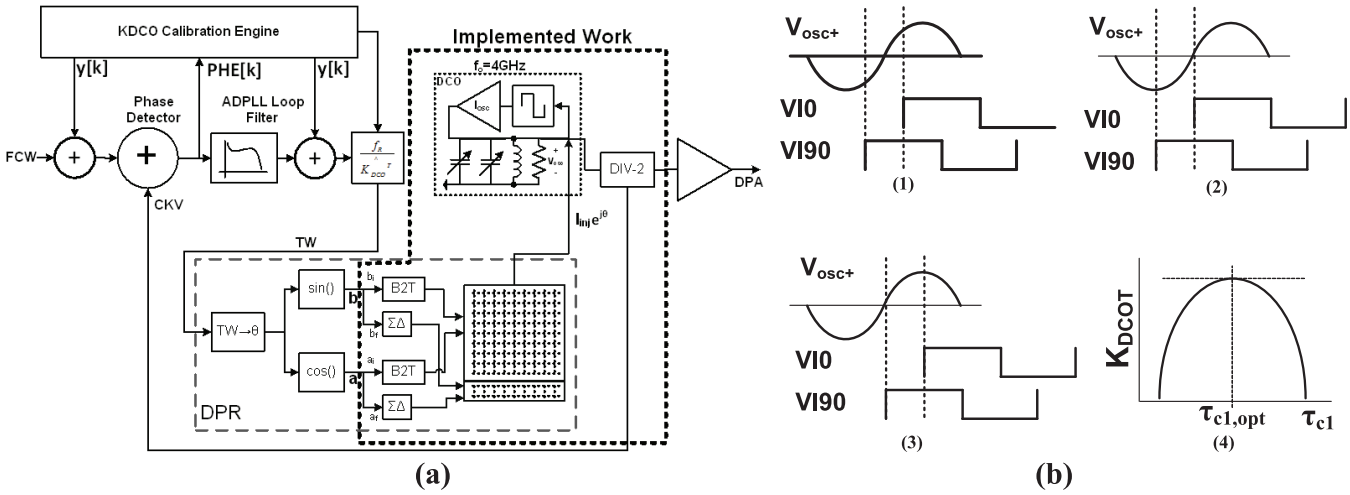


Fig. 9. (a) K_{DCOT} calibration engine monitoring PHE signal to optimize τ_{c1}. (b) Calibration of τ_{c1} delay line: (1) proper timing between VI0/90 and $V_{\mathrm{osc}+}$; (2) VI0/90 leading $V_{\mathrm{osc}+}$; (3) VI0/90 lagging $V_{\mathrm{osc}+}$; (4) illustration of K_{DCOT} as a function of τ_{c1}.

D. DPR Unit Cell

The DPR unit current cell, shown in Fig. 8(b), comprises a cascode current source $(\mathrm{M}_3, \mathrm{M}_4)$, differential pair $(\mathrm{M}_5, \mathrm{M}_6)$, the enable switch, selection logic, and bypass capacitors. A current reference circuit supplies bias to the cascode current mirror in each cell. The typical current in each unit cell is 30 μA. The cascode current source topology increases the output impedance looking into node 'X.' This is important because the remaining transistors in that cell, M5–M8, operate in a triode region when turned on and offer very little resistance to ground. The differential output node of each current cell is connected to the DCO. This will result in some loading of the DCO output.

V. Calibration

As mentioned in Section IV-B, the quadrature phases for the DPR block generated by the phase generator have to be aligned with the oscillator voltage waveform V_{osc}, as shown in Fig. 9(b)(1). Any misalignment will result in a non-linear and limited frequency tuning range and step size. The proper alignment is attained by setting the τ_{c1} coarse delay line. Note that DCO frequency tuning range and step size are related to Q according to (4) which is sensitive to temperature. Therefore, these parameters are also sensitive to temperature.

The method of calibrating the τ_{c1} delay line is illustrated in Fig. 9(a). The detection part and the top-level algorithm are based on an RF built-in self-test (RF-BIST) technique developed by the authors for a high-volume commercial transceiver described in [19]. It exploits an idea of observing a key digital signal of an all-digital PLL (ADPLL) (e.g., phase error) to ascertain an RF performance of the ADPLL or a transmitter. That idea was further developed in [18], [19], [21], [22].

The main idea here is to apply a small time-varying FM signal $y[k]$ which is then translated into the DPR current control word through a normalization factor represented by the term f_R/K_{DCOT}. The extent of current control word variation is such that the injected signal phase θ into the LC-tank varies between $\pm 5^\circ$ around a mean phase set by τ_{c1} delay line code.

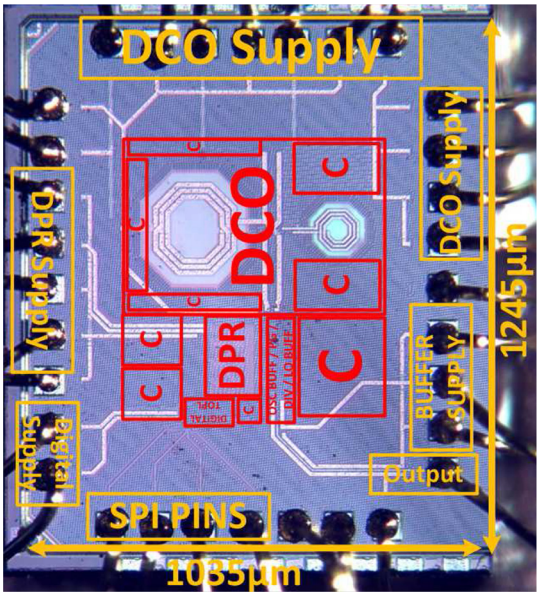


Fig. 10. Die photograph of proposed RF digital-to-frequency converter (DFC).

K_{DCOT} can be determined by an algorithm described in [18], [19], [21], while the DCO is frequency locked by the ADPLL. According to the LMS-based DCO gain estimation algorithm in [18], due to the closed-loop operation of the ADPLL, any mismatches between the digitally estimated DCO gain K_{DCOT} and the actual DCO gain will result in perturbation on the filtered digital phase error (PHE) signal. In the proposed regime, K_{DCOT} is adjusted until the variance of PHE signal is minimized and the final value is then stored in a local memory. Fig. 9(b)(1), (2), and (3) show the relationship of the oscillator signal with respect to VI0 and VI90 signals at the DPR input for three different settings of τ_{c1}. The resulting K_{DCOT} for each value of τ_{c1} is plotted in Fig. 9(b)(4). Fig. 9(b)(2) and (3) show a scenario where τ_{c1} is not set to the optimal value, which results in the average phase between VI0 and VI90 signals being far away from the zero crossing of the $V_{\mathrm{osc}+}$ signal. Consequently, the K_{DCOT} is low. Fig. 9(b)(1) shows the

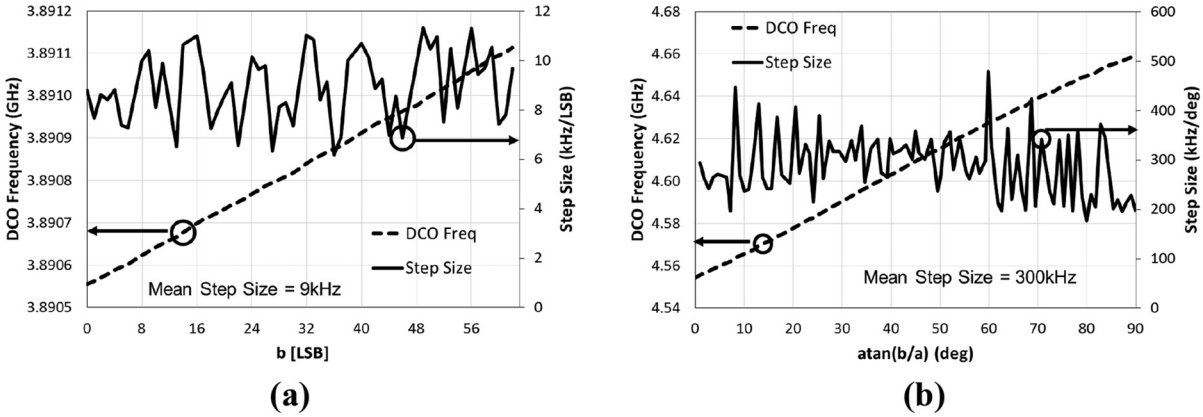


Fig. 11. Measured tuning ranges: (a) with $I_r = 0.15$, DNL $= \pm 0.6$ LSB; (b) with $I_r = 0.32$, DNL $= \pm 0.5$ LSB.

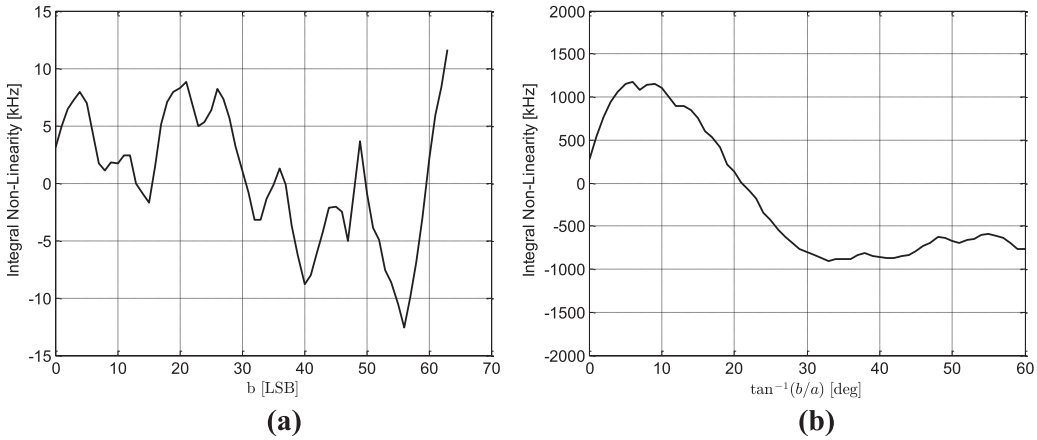


Fig. 12. Measured INL (a) with $I_r = 0.15$; (b) with $I_r = 0.32$.

scenario where τ_{c1} is properly calibrated and K_{DCOT} is maximum. Therefore, the optimum setting of τ_{c1} is determined by performing the calibration algorithm over all settings of τ_{c1} and then storing the setting of the maximum K_{DCOT} to be used during payload transmission. The proposed calibration scheme was verified manually on fabricated silicon and without an on-chip state machine [18] to perform the operation. The extensive measurement results in [22] prove that estimating the DCO step size accuracy to within 1% (i.e., 200 Hz) is feasible.

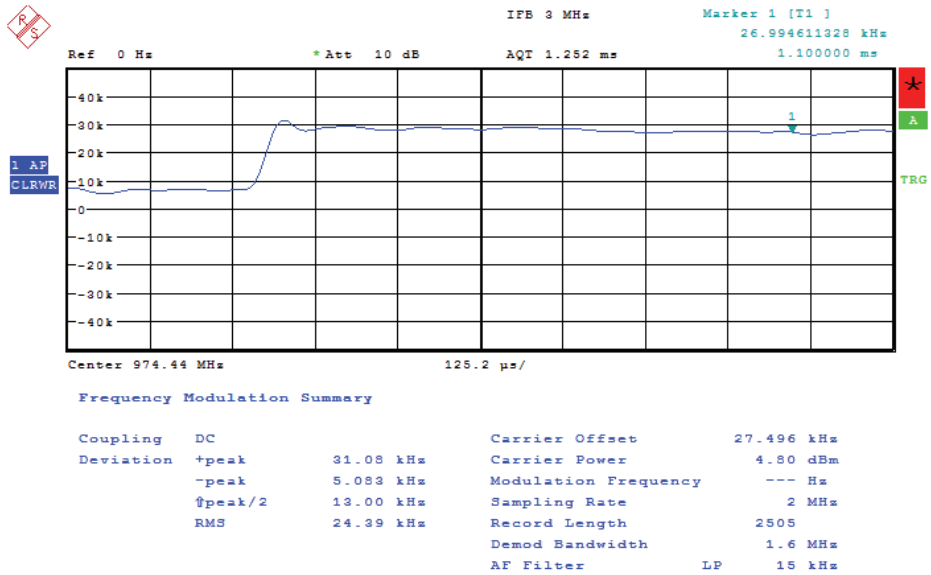
VI. Experimental Results

The proposed DCO was implemented and fabricated in TSMC 40 nm 1.1 V 1P7M LP CMOS technology. Fig. 10 shows the chip micrograph. In the narrowband (NB) configuration, the $\Sigma\Delta$ dithering is turned off. The τ_{c1} delay line is *manually* calibrated according to the procedure described in Section V since the digital system required for the automatic calibration was not implemented on the fabricated silicon. The τ_{c2} setting was determined through simulations and was verified to be optimum through lab measurements. Like τ_{c1}, an optimum τ_{c2} would result in the highest DCO gain. The DCO step size is measured in units of Hz per degree change in θ since the transfer function is more conveniently expressed in this manner instead of the digital inputs a and b.[2]

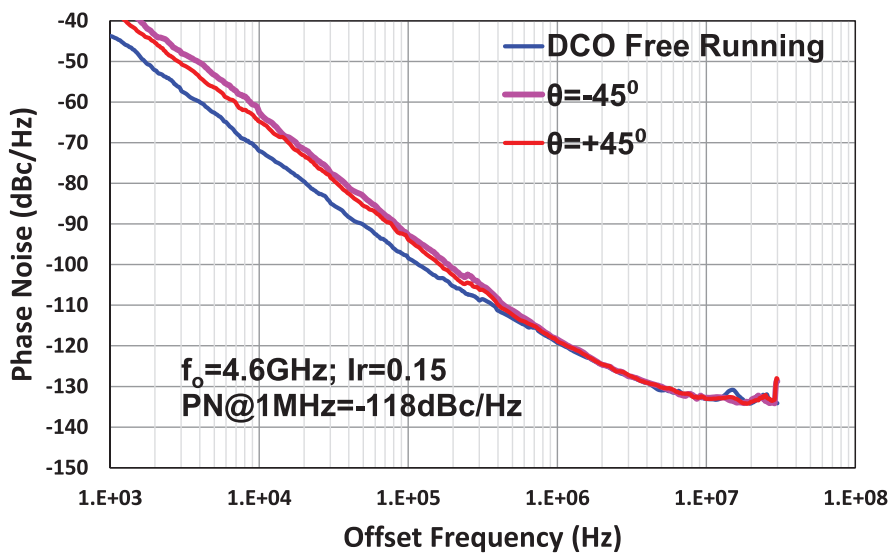
[2]For a 6 bit word length of a and b, the approximate step size is 1°, since $\tan^{-1}(1/63) < 1^\circ$.

In the NB modulation configuration, the DPR unit cell current is 31 μA which brings the total injected current to 1.97 mA. The ratio between injection current and oscillator current I_r is 0.15. A more efficient way for generating FM in this configuration is to shut off one of the interleaved DACs in the DPR and one of the quadrature phases from the phase generator. In this configuration, the frequency of the DCO is varied by modulating the amplitude of the injected signal I_{inj} instead of the phase θ. This results in a substantial current savings from the DPR and the phase generator. Since the DPR unit cell current is limited by design, in order to reduce the injection strength I_r, I_{osc} has to be increased to 12.8 mA. I_{inj} can be varied through either control words a or b. The results with NB modulation are captured in Fig. 11(a). The mean step size is 9 kHz while the total tuning range over all the DPR settings is 550 kHz. Fig. 11(b) shows the tuning range measurement when I_r is 0.32. In this setting, the measured tuning range is 80 MHz while the step size is 300 kHz. In this case, both of the interleaved DACs are enabled in order to sweep the injected phase θ from -45° to 45° by setting appropriate values of the control words a and b. The measured INL data is shown in Fig. 12.

Measuring the step size of the DCO can be challenging especially in the NB configuration due to oscillator drift and phase noise. For the data shown in Fig. 11, a time domain method was used in which the DPR DAC control word is toggled between two consecutive settings. The resulting frequency-shift keying



(a)



(b)

Fig. 13. (a) Method of measuring DCO step size for NB configuration mode. (b) DCO phase noise in NB configuration with $\theta = \pm 45°$ compared with free-running mode.

(FSK) spectrum is demodulated on a vector spectrum analyzer (VSA) to measure the time-varying frequency of the DCO as shown in Fig. 13(a). The VSA capture window is set so that the DCO frequency is captured before and after the new DAC settings are applied. The bandwidth and filter settings of the VSA are set to reduce in-band frequency noise, and the frequency step is measured by averaging the trace captured in Fig. 13(a) many times.

The phase noise performance in the NB configuration is shown in Fig. 13(b) at minimum and maximum values of θ. The phase noise profile is compared with that in the free-running mode. The DCO phase noise at 1 MHz is -118 dBc/Hz which is still reasonably competitive with other architectures. The far-out noise is limited by the output buffer and therefore a phase noise of better than -132 dBc/Hz cannot be measured at those frequencies. The measured $1/f^3$ corner (the point along the x-axis where the slope of phase noise changes from 30dB/dec to 20 dB/dec) is around 600 kHz.

As mentioned earlier, the state machine of the proposed calibration scheme detailed in Section V was not implemented in the fabricated silicon and therefore it is important to verify the technique *manually* as shown in Fig. 14. The DCO is set in the WB configuration and θ is swept from a minimum to maximum setting. The DCO transfer function is measured for all

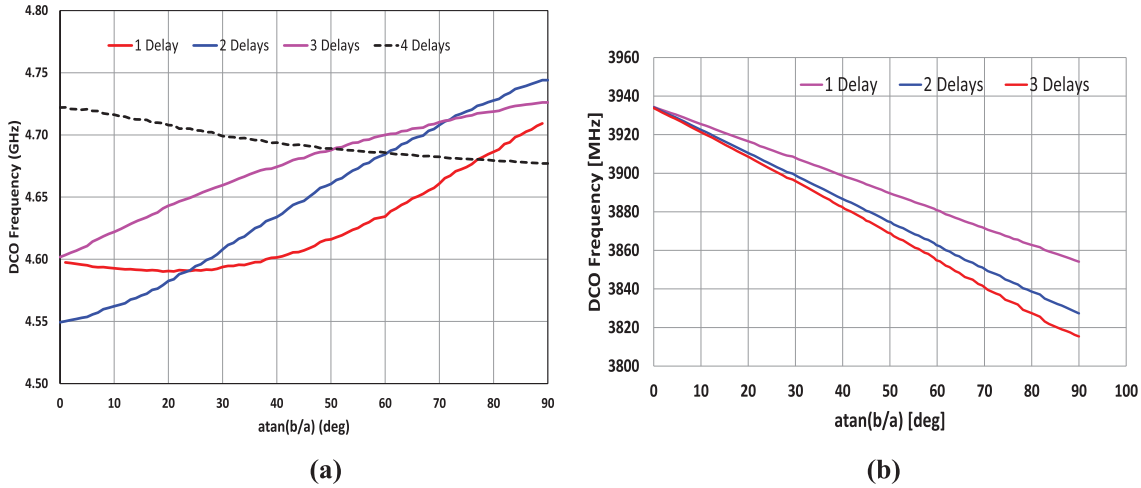


Fig. 14. (a) Measured DCO transfer function versus various τ_{c1} delay line settings. (b) Measured DCO transfer function versus various τ_{c2} delay line settings.

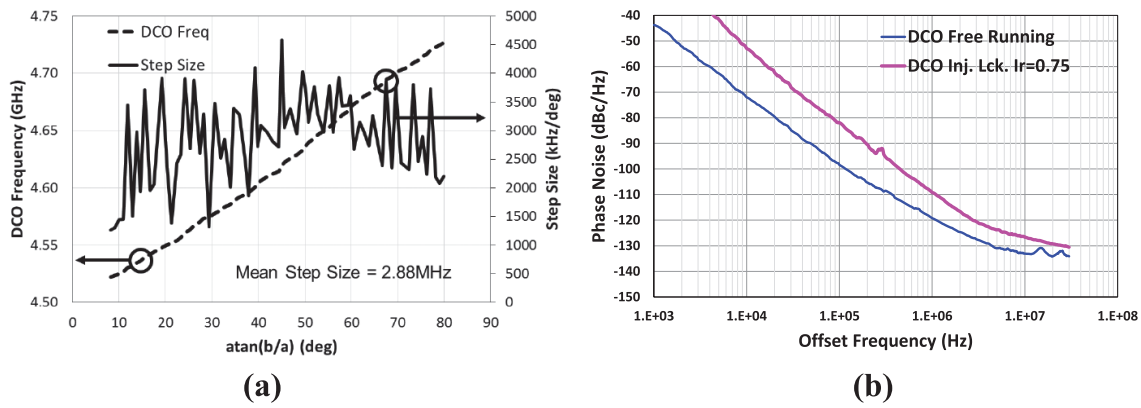


Fig. 15. (a) Measured tuning ranges in wide-band modulation setting ($I_r = 0.75$) DNL $= \pm 1.5$ LSB. (b) DCO phase noise in wideband configuration compared with free-running mode.

the possible delay settings. The appropriate τ_{c1} setting is the one that results in the maximum DCO gain, which is attained with two delays according to Fig. 14(a). A similar approach can be used to calibrate the τ_{c2} delay line. For a given setting of τ_{c1}, the optimum τ_{c2} setting is the one that results in the largest DCO gain, which is the setting of three delays according to Fig. 14(b).

A. Further Experiments in Wideband Mode

In order to determine the feasibility of the proposed solution outside the targeted application space, the IC was futher tested in WB mode. The results from the numerical model discussed in Section III show that injection-locking range beyond 100 MHz is possible if the injection current is strong enough in spite of the high Q of the resonant tank that is required in order to meet the out-of-band noise requirements. The DCO peak voltage curve in Fig. 4(b) represents another headwind for such task, as it underscores the fact that $V_{\mathrm{osc,pk}}$ decreases as the oscillator is steered away from the resonant frequency of the LC-tank, which will consequently degrade the DCO phase noise. However, the extent of that degradation is somewhat dependent on the spectral density of the FM signal itself [6].

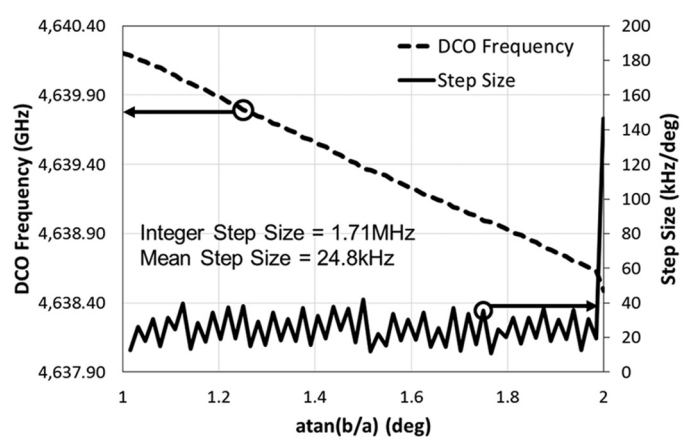


Fig. 16. Measured step size with MASH $\Sigma\Delta$.

Typically, a significant population of discrete frequencies of the modulated signal is concentrated around the carrier Therefore, the injection-locked DCO, for the most part, operates close to the resonance frequency of the LC-tank. Consequently, the system scarcely operates in the region of low $V_{\mathrm{osc,pk}}$. Operating in such a way will reduce risks and will prevent additional distortions that will limit the DCO performance.

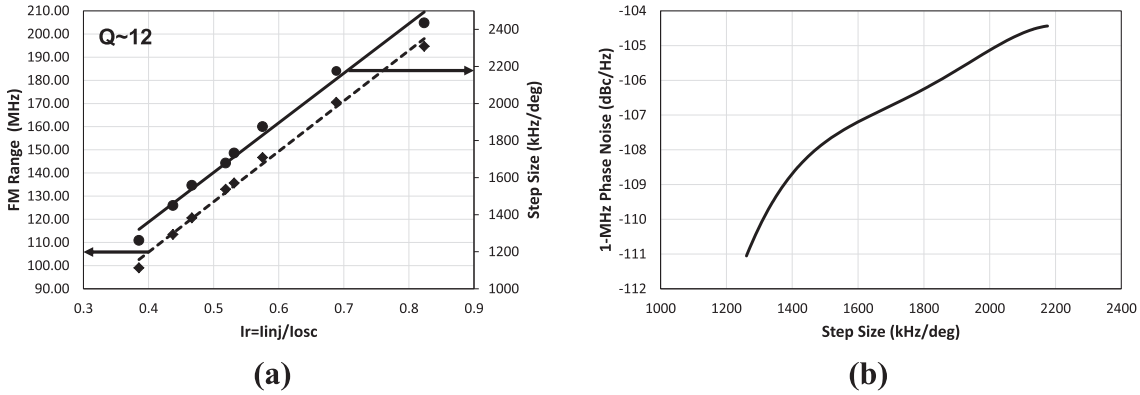


Fig. 17. (a) Injection-locking range or FM range vs. injection strength I_r. (b) DCO phase noise at 1 MHz offset versus step size. The natural phase noise (i.e., $I_r = 0$) at 1 MHz offset is -119 dBc/Hz.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

		This Work		[7]	[6]	[10]	[9]
Technology		40nm		65nm	65nm	65nm	90nm
Supply Voltage (V)		1.1		1.25		1.2	1.2
Frequency (GHz)		4.6		3	2.5	8	3.3
Tuning Range (Capacitive)	Coarse (MHz)	2100		780	140		600
	Fine (MHz)			2-12[a]			
Mode		NB	WB				
Tuning Range (Injection Locked) (MHz)		0.558[a]	200[a]			60	
Fine Freq Resolution (kHz)		9[a]	2280[a]	0.15-1.5[a]	270		5
Phase noise (dBc/Hz)[b]	1MHz	-118	-103	-127.5		-115.1	-118
	20MHz	-130[c]	-130[c]			-138	
Current consumption (mA)		26.9	16.7	16		10	2
Oscillator core area (mm^2)		0.27	0.27	0.32	0.18	0.18	
Oscillator description		Injection Locked		Capacitive Tuning	Capacitive Tuning	Injection Locked	Capacitive Tuning

(a) Without $\Sigma\Delta$ dithering.
(b) All phase noise data at DCO output.
(c) Output buffer limited.

In the WB configuration, the DPR unit cell current is 61 μA, which brings the total injected current to 3.9 mA. The oscillator current is 5.1 mA, therefore I_r is 0.75. The results are captured in Fig. 15(a). The mean step size is 2.88 MHz while the minimum and maximum DCO frequencies are 4.522 GHz and 4.729 GHz, respectively, which brings the total FM range just over 200 MHz over the injected phase range of 70°. The DCO phase noise in the WB configuration is shown in Fig. 15(b). Based on the phase noise comparison between the injection-locked and free-running mode, it is evident that DCO suffers from phase noise degradation due to the loading from DPR which is exacerbated as more DPR cells are engaged with higher current.

In addition, $\Sigma\Delta$ processing is required in this configuration if the frequency resolution is not adequate. The transfer function of the MASH $\Sigma\Delta$ is shown in Fig. 16 which shows the step size measured with $\Sigma\Delta$ dithering. The 6 bit input of the $\Sigma\Delta$ is swept from 0 to 63 while the integer phase boundary is between 1° and 2°. The integer step size is measured to be 1.71 MHz while the step size with $\Sigma\Delta$ is 24.8 kHz, which is 2^{-6} times the integer step size. The reduction of step size with $\Sigma\Delta$ also improves the in-band quantization noise by 37 dB.

It is of interest to understand how the injection strength I_r can be scaled to attain an increased FM range that is proportional to ω_L. In Fig. 17(a), we have measured the FM range over θ as a function of I_r. Note that the slopes of two curves correspond to the estimated $Q = 12$ from (3) and (4). With the proposed technique for the NB modulation using the amplitude of injected signal, the FM range can be reduced to less than 1 MHz while the upper limit with WB configuration can be as high as 200 MHz. Fig. 17(b) shows the phase noise performance versus step size, which is the left-hand side of (3) when properly adjusted for the units. The increased FM range comes at a cost of degraded phase noise performance. As shown in Fig. 8(b), the DPR DAC loads and unbalances the $V_{\mathrm{osc}+}$ and $V_{\mathrm{osc}-}$ nodes of LC tank as more DPR current cells with dynamic r_o resistance are engaged. r_o is inversely proportional to the number of active cells and to the bias current.

Table I summarizes the measured performance of the proposed DFC and compares it with state-of-the-art solutions. This work realizes a DFC which can be dynamically programmed

between the WB mode with high tuning range and NB mode with fine frequency resolution, while not particularly addressing the pure RF performance. All results are translated to the DCO output frequency. The measured tuning range of the DFC ranges from 550 kHz to 200 MHz at the DCO output. The step sizes in the WB and NB configurations are 2.88 MHz and 9 kHz, respectively, without $\Sigma\Delta$ processing, and 45 kHz and 140 Hz with $\Sigma\Delta$ processing. The frequency resolution in the WB configuration could be improved by increasing the DPR array size to 256 elements, which would bring the step size down to 11 kHz.

VII. Conclusion

We have proposed and demonstrated a method to achieve a fine step size of an LC-tank based digitally controlled oscillator (DCO). The DCO gets first tuned to its center frequency by means of a conventional switchable-capacitor array. Then, the fine frequency tuning is achieved via a new method of digitally controlling the phase and amplitude of injected current into the LC-tank generated from its own resonating voltage. In this way, a linear deviation from the center frequency with a DNL of ± 0.6 LSB can be achieved with a low DCO step size without resorting to an oversampled noise-shaped dithering. Alternatively, the system can be configured in wideband mode for potential application in future wideband digital polar transmitter architectures. The measured trend of injection strength and tuning range is in line with observations from numerical models. Thus, we conclude that the self injection locking could be a viable means of generating frequency modulation for various wireless applications.

Acknowledgment

The authors would like to thank the TSMC University Shuttle Program for chip fabrication, Dr. Chih-Ming Hung for useful discussions, and the technical staff at Delft University of Technology for their outstanding support during the IC chip tapeout and measurements, in particular Masoud Babaie, Amir Reza Ahmadi Mehr, Atef Akhnoukh, and Will Straver.

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