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Analysis and Design of a High-Order Discrete-Time Passive IIR Low-Pass Filter

Massoud Tohidian, *Student Member, IEEE*, Iman Madadi, *Student Member, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

Abstract—In this paper, we propose a discrete-time IIR low-pass filter that achieves a high-order of filtering through a charge-sharing rotation. Its sampling rate is then multiplied through pipelining. The first stage of the filter can operate in either a voltage-sampling or charge-sampling mode. It uses switches, capacitors and a simple gm-cell, rather than opamps, thus being compatible with digital nanoscale technology. In the voltage-sampling mode, the gm-cell is bypassed so the filter is fully passive. A 7th-order filter prototype operating at 800 MS/s sampling rate is implemented in TSMC 65 nm CMOS. Bandwidth of this filter is programmable between 400 kHz to 30 MHz with 100 dB maximum stop-band rejection. Its IIP3 is +21 dBm and the averaged spot noise is 4.57 nV/ $\sqrt{\text{Hz}}$. It consumes 2 mW at 1.2 V and occupies 0.42 mm².

Index Terms—CMOS, digital equalization, discrete time, high linearity, high order, IIR, low noise, low-pass filter, low power, passive, real pole, reconfigurable, switched capacitor.

I. INTRODUCTION

INTEGRATED low-pass filters (LPFs) are key building blocks in various types of applications, such as wireless communications [1]–[7], hard-disk drive read channel [8], [9], video signal processing [10], smoothing filtering in a DAC [11], and anti-aliasing filtering before a sampling system. Noise of these filters is one of the key system-level concerns. This noise can be usually traded off with the total filter capacitance and, consequently, total power and area. Therefore, for a given system-level noise budget, a filter with a lower noise coefficient reduces the area and power consumption. On the other hand, linearity of the filter should be high enough to maintain fidelity of the wanted signal.

As shown in Fig. 1, three types of commonly used analog filters are Gm - C , active RC , and active switched-capacitor (SC) filters [12]–[17]. In Gm - C and active RC filters, pole/zero locations are set by g_m value, capacitance (C), and resistance (R). Due to the poor matching of g_m/C and R/C values,

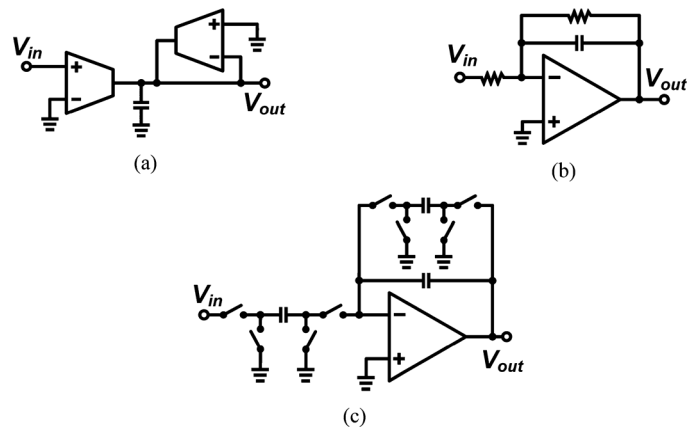


Fig. 1. Conventional analog filters: (a) Gm - C , (b) active- RC , and (c) active switched-capacitor.

process-voltage-temperature (PVT) variations have considerable impact on filter transfer function. Therefore, many applications require component (i.e., g_m , R , and C) calibration/tuning [16], [17]. However, pole/zero locations of active SC filters are accurately set by capacitor ratio, thus minimizing the effect of PVT variations.

Implementation of such filters in deep nanoscale CMOS is becoming increasingly difficult, especially due to the design challenges of high-quality opamps and high-linearity gm-cells. In contrast, switching performance of MOS transistors is improving due to the technology scaling. Consequently, passive switched-capacitor filters are expected to work at much higher sampling rates than do the active SC filters, where the speed is limited to opamp settling. Also, the passive filters will consume much less power. However, it might not be possible to synthesize complex poles in a fully passive structure.

The passive LPF proposed in this paper benefits from these advantages. Using a sampling capacitor to rotate charge between several history capacitors, a high-order IIR low-pass filter is created. To further increase sampling rate, a pipelining technique of the sampling capacitor is introduced. Using these techniques, a 7th-order LPF is implemented, that operates up to 1 GS/s [18]. In [1]–[5], passive switched-capacitor FIR/IIR filters have been used for baseband signal processing of an RF receiver. However, none of the prior publications have proposed such a high-order passive filtering in one stage. A somewhat similar structure resembling the charge rotating filter has been reported in [19]. However, a 3rd-order LPF filter is used in an N-path filter to form a band-pass transfer function. Furthermore,

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its LPF does not exploit any pipeline techniques such as one introduced in this work.

The proposed filter has a very low input-referred noise, because of using only one sampling capacitor for all the filtering stages. Thanks to the passive operation, it has an extremely high linearity. A simple inverter-based gm-cell might be used in front of this filter to provide gain. This filter consists of only switches, capacitors, a clock waveform generator, and a simple gm-cell. Therefore, it is amenable to the digital deep nanoscale CMOS technology. The proposed filter has been successfully verified at the system level in a discrete-time superheterodyne receiver [6]: The 6th-order charge-rotating filter is employed there as the first baseband channel selection filter.

The rest of this paper is organized as follows. Section II provides an overview of basic DT passive LPF. Section III describes the proposed high-order DT filter. Design and implementation of the filter are described in Section IV. Section V summarizes measurement results. Section VI provides the conclusion.

II. BASIC DISCRETE-TIME LOW-PASS IIR FILTERS

A. First-Order Filter

Perhaps the simplest analog discrete-time (DT) filter is a passive 1st-order IIR low-pass filter, as depicted in Fig. 2(a) [20]. In each cycle at ϕ_1 , a sampling capacitor C_S samples a continuous-time input voltage $V_{in}(t)$. Hence, we call it a *voltage sampling filter*. Then at ϕ_2 , C_S shares its stored charge with a history capacitor C_H . At the end of ϕ_2 , we have the following equation for the discrete-time output voltage:

$$V_{out}[n] = \frac{C_H}{C_H + C_S} V_{out}[n-1] + \frac{C_S}{C_H + C_S} V_{in}[n-0.5]. \quad (1)$$

Hence, its transfer function can be written in z-domain as

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{(1-\alpha)z^{-0.5}}{1-\alpha z^{-1}} \quad (2)$$

where coefficient α is $C_H/(C_H + C_S)$. This is a standard form of a DT LPF with unity dc gain and half-a-cycle delay, $T_s/2$. Switch driving clock waveforms are shown in Fig. 2(c).

The step response of this filter is shown in Fig. 3(a). C_S and C_H are chosen 1 pF each, just for illustration's sake. Discrete-time output samples are available in each cycle at the end of ϕ_2 .

Fig. 2(b) shows an alternative 1st-order DT LPF (IIR1) exploiting *charge sampling* [2], [20], [21]. At first, the continuous-time input voltage is converted into current by the gm-cell of transconductance gain g_m . This current is integrated over a time window T_s on C_H and C_S during ϕ_1 and on C_H during ϕ_2 . However, we can assume for simplicity that discrete-time input charge packets arrive only at ϕ_1 :

$$q_{in}[n] = \int_{(n-1)T_s}^{nT_s} g_m V_{in}(t) \cdot dt. \quad (3)$$

Although this assumption slightly changes transient waveforms of C_H and C_S voltages, it leads to exactly the same values of the output samples while simplifying the analysis of the filter.

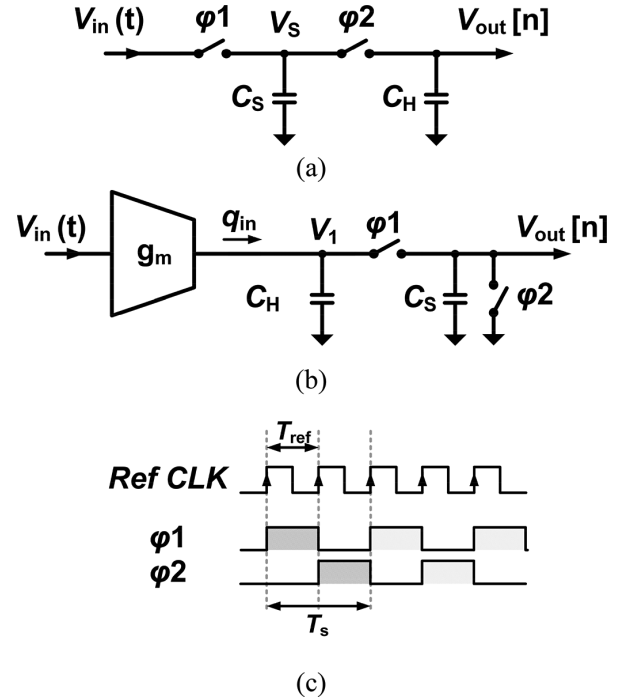


Fig. 2. (a) Voltage sampling and (b) charge sampling 1st-order DT IIR filter with (c) their clock waveforms.

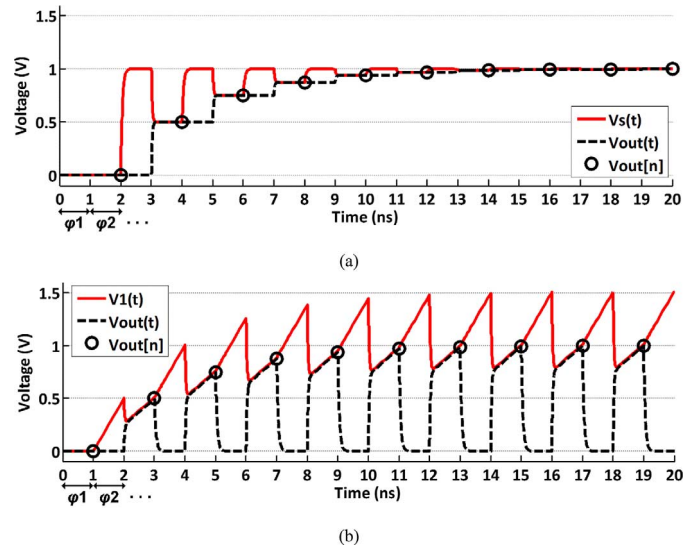


Fig. 3. Step response of (a) the voltage sampling, and (b) charge sampling 1st-order DT filter ($C_H = C_S = 1$ pF, $g_m = 0.5$ mS, $f_{ref} = 1$ GHz, and $f_s = 500$ MS/s).

During ϕ_1 , C_H shares its charge with C_S and a new charge is input. Consequently, we have the DT output samples at the end of ϕ_1 :

$$V_{out}[n] = \frac{C_H}{C_H + C_S} V_{out}[n-1] + \frac{1}{C_H + C_S} q_{in}[n], \quad (4)$$

$$\frac{V_{out}(z)}{q_{in}(z)} = \frac{1}{C_S} \times \frac{1-\alpha}{1-\alpha z^{-1}}. \quad (5)$$

The step response of this filter is shown in Fig. 3(b). In this example, C_S and C_H are 1 pF and g_m is 0.5 mS.

Fig. 4 shows top-level behavioral models of the IIR1 filters. In the voltage-sampling structure of Fig. 4(a), the sampler first

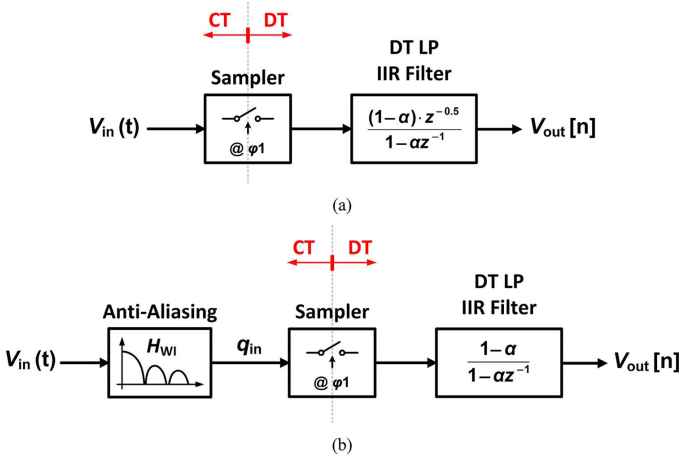


Fig. 4. Top-level block diagram model of (a) voltage sampling, and (b) charge sampling IIR1.

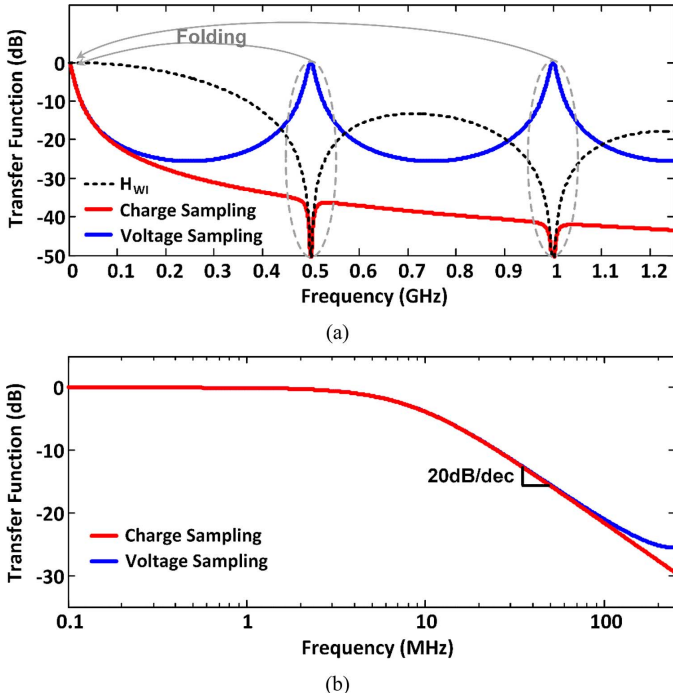


Fig. 5. (a) Wideband transfer function, and (b) Bode plot frequency response of IIR1 ($C_S = 1$ pF, $C_H = 9$ pF, $g_m = 0.5$ mS, $f_{ref} = 1$ GHz, and $f_s = 500$ MS/s).

samples the continuous-time (CT) analog input voltage $V_{in}(t)$ at φ_1 and converts it into a DT analog voltage. Then, this signal is fed to a 1st-order LPF with half-a-cycle delay ($z^{-1/2}$) and the output comes out every cycle at φ_2 . DC voltage gain of this filter is unity. Based on the Nyquist sampling theory, sampling of a CT signal folds frequencies around $k \times f_s$ (for $k = 1, 2, 3, \dots$) into around dc, where f_s is the sampling frequency. As depicted in Fig. 5(a), we observe the folding image frequencies at f_s , $2f_s$, and so on. Fig. 5(b) shows the transfer function, which has a roll-off of 20 dB/dec.

A behavioral model of the charge-sampling IIR1 is depicted in Fig. 4(b). Integrating the gm-cell current in the time window, as described in (3), forms a CT *sinc*-type antialiasing filter prior

to sampling [2], [20]–[22]. The transfer function of this windowed integration (WI) from the input voltage to the output charge is

$$H_{WI}(f) = g_m T_s \times \frac{\sin(\pi f T_s)}{\pi f T_s}. \quad (6)$$

This *sinc*-shape filter has notch frequencies at k/T_i ($k = 1, 2, 3, \dots$). Assuming ideal clock waveforms, T_i is the same as $T_s = 1/f_s$. In the next step, the sampler converts the CT signal to a DT signal and, at the end, a 1st-order DT LPF performs the main filtering. As shown in Fig. 5(a), notch frequencies of the antialiasing filter are on top of the folding image frequencies, thus offering some protection. DC voltage gain is calculated by multiplying the dc gain of the antialiasing filter by the dc gain of the DT filter:

$$A_V = \frac{V_{out}}{V_{in}} = g_m T_i \times \frac{1}{C_S} = g_m \times \frac{1}{C_S f_s}. \quad (7)$$

In this equation, $1/(C_S f_s)$ is an equivalent DT resistance of the sampling capacitor.

B. Second-Order Filter

As shown in Fig. 6(a), a 2nd-order DT low-pass filter (IIR2) can be synthesized by adding a second history capacitor to the charge sampling 1st-order LPF [1], [3], [7], [20]. The previously analyzed charge sampling filter, IIR1, is indicated here within the blue dotted box.

At the end of φ_1 , C_S contains the output sample of the IIR1. Then, by connecting C_S to a second history capacitor C_{H2} at φ_2 , another 1st-order LPF is formed, whose structure is indicated within the red dashed box in Fig. 6(a). Then at φ_3 , the remaining history of C_S is cleared by discharging it to ground. This ensures proper operation of the first IIR1. The transfer function of this filter is plotted in Fig. 6(b). The 2nd-order IIR filter has a 2x steeper slope of 40 dB/dec compared to the IIR1 with 20 dB/dec.

III. PROPOSED HIGH-ORDER DT IIR LOW-PASS FILTER

Many applications require higher orders of filtering. The easiest way to build a high-order filter is to cascade two or more 1st and/or 2nd order filters. A similar approach has been used in [2] and [4], where two gm-cells and passive filters are cascaded. However, extending the IIR filter order using the conventional approach carries two serious disadvantages: First, the active buffers between the stages worsen both the noise and linearity. Second, the increased reset-induced charge loss on each stage of filter lowers signal-to-noise ratio. We propose a new structure that does not suffer from these handicaps.

A. Charge Rotating DT Filter

Before introducing a new high-order filter, the IIR2 is redrawn in Fig. 7(a). C_S is placed at the center of the (as yet incomplete) circle. In each cycle, C_S is “rotating” clockwise and is sequentially connecting to C_{H1} , C_{H2} , and then ground.

To extend this idea, we add in Fig. 7(b) a few phase slots between φ_2 and the last reset phase, together with more history capacitors. By moving to the next new phase, φ_3 , C_S which

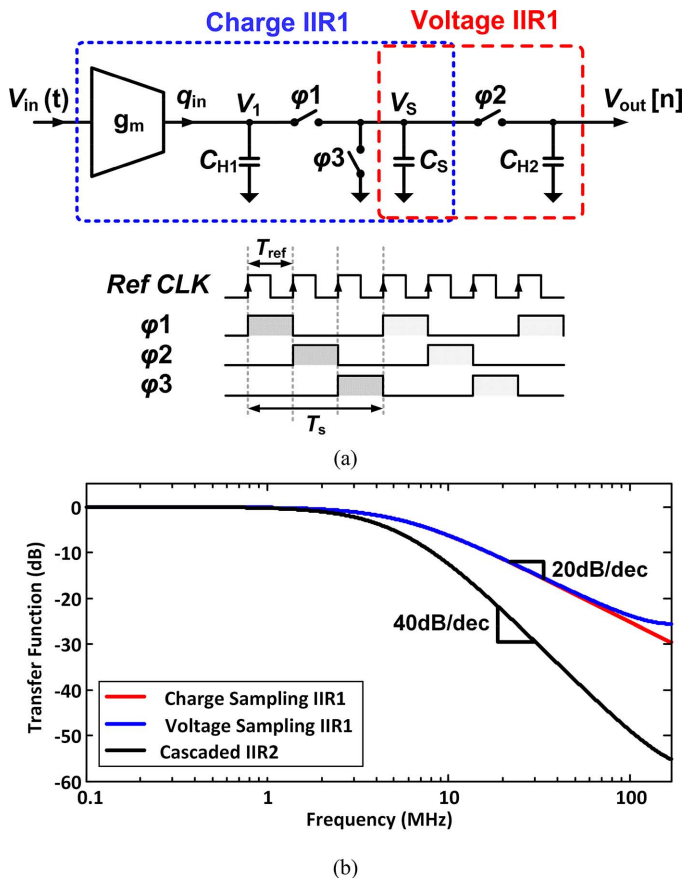


Fig. 6. (a) Second-order DT low-pass filter and (b) its frequency response ($C_H = C_S = 1$ pF, $g_m = 0.33$ mS, $f_{ref} = 1$ GHz, and $f_s = 333$ MS/s).

now holds the sample of the 2nd-order filter, shares its charge with a third history capacitor C_{H3} . This charge sharing creates another IIR1, cascaded with the previous IIR2. Hence, we now have a 3rd-order filtering function on C_{H3} that can be read out at the end of ϕ_3 . We can continue doing so until the seventh history capacitor C_{H7} (or arbitrarily higher), in order to make a 7th-order filter. In the last phase ϕ_8 , C_S is finally reset. Since the C_S capacitor rotates charge between the history capacitors, we call this structure a “charge rotating” DT filter. As shown at the bottom of Fig. 7(c), required multiphase clock waveforms to drive the switches can be generated from a reference clock.

Compared to the IIR2 structure in Fig. 6(a), the new charge rotating (CR) structure preserves its gain and linearity even at much higher filtering orders. The gain remains the same simply because no additional charge loss occurs in the system. In this filter structure, the switched-capacitor circuit is remarkably linear and so the gm-cell appears to be the bottleneck of the linearity.

B. Step Response

To better understand the operation of the filter, its step response is plotted in Fig. 8. At first, suppose all the capacitors are empty. For simplicity, we choose $C_S = C_H = 1$ pF. Also, we suppose that the input charge packet $q_{in}[n] = 1$ pC arrives every cycle at ϕ_1 . A zoom-in of the step response is plotted in Fig. 8(a). At ϕ_1 , the input charge is transferred to C_{H1} and C_S that sets the 0.5 V potential on both capacitors. C_S , which contains a sample of the 1st-order filter at the end of ϕ_1 , is then

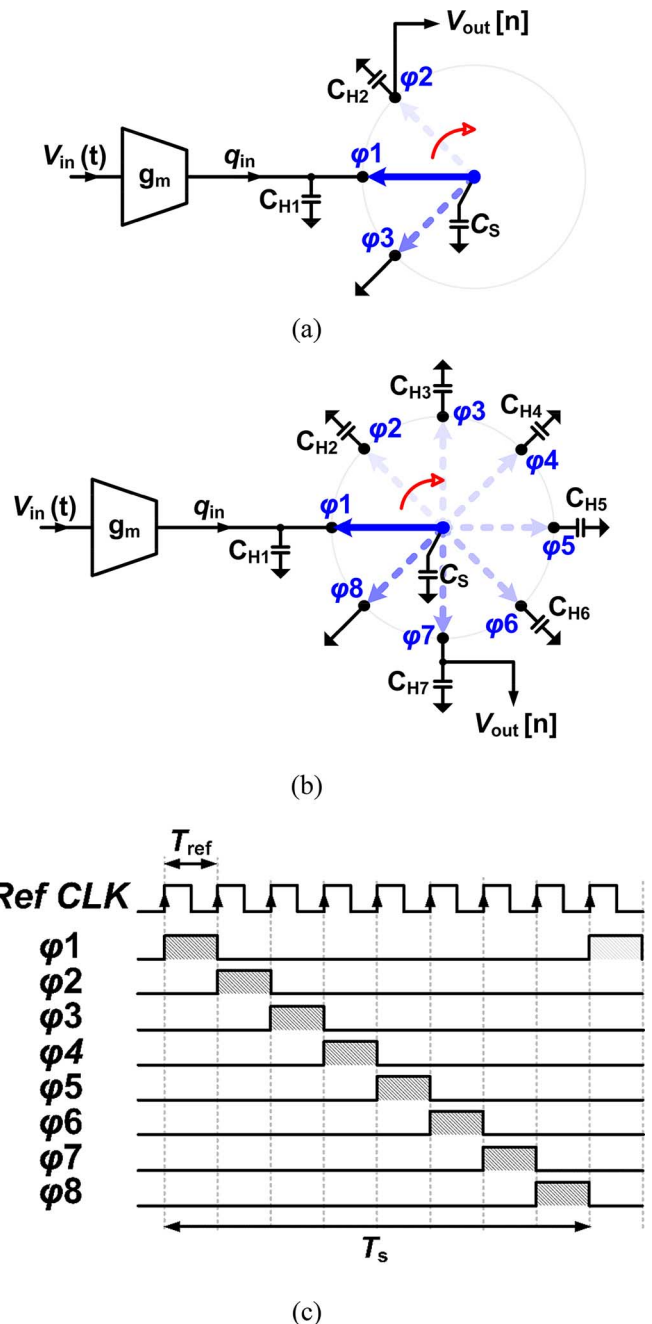


Fig. 7. (a) The IIR2 is redrawn. (b) Charge rotating 7th-order filter with (c) its clock waveforms. A closed switch is shown with a solid arrow, and an open switch is shown with a dimmed dashed arrow.

connected to C_{H2} at ϕ_2 . The result is 0.25 V on both capacitors. Next at ϕ_3 , C_S , containing the sample of the 2nd-order filter, is connected to C_{H3} and the result is 0.125 V. In this way, C_S transfers charge from one history capacitor to the next until C_{H7} . Then, it gets reset at ϕ_8 . As plotted in Fig. 8(b), the outputs of higher-order stages are growing more slowly. This is because their respective input samples have been accumulated several times earlier, meaning slower but longer and smoother integration.

C. Transfer Function

Considering that samples of the main output $V_{out} = V_7$ are ready at the end of ϕ_7 , we have (8), shown at the bottom of

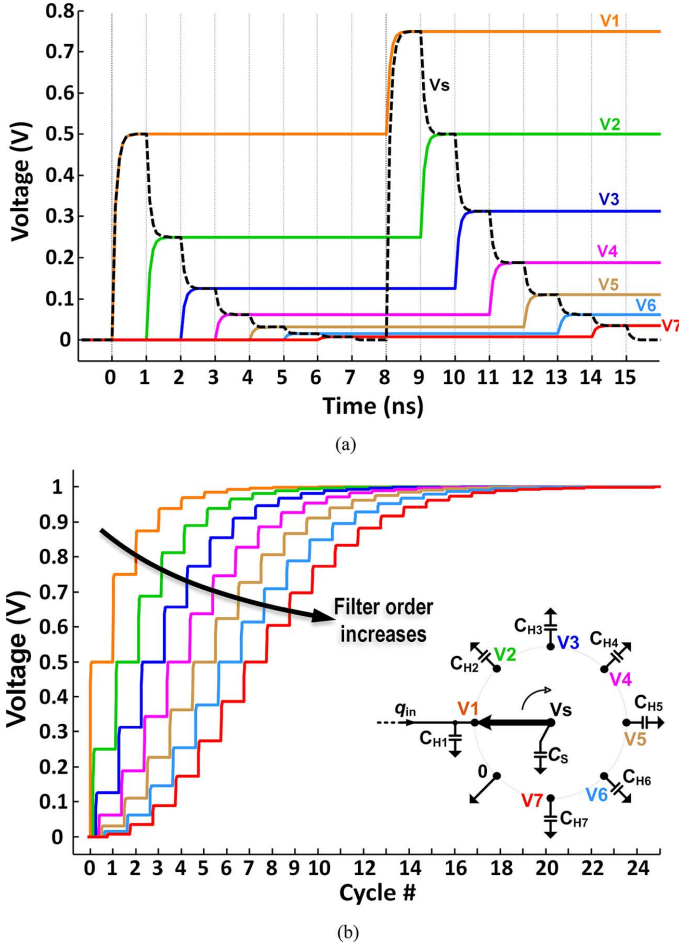


Fig. 8. (a) A zoom-in and (b) the whole step response of the charge rotating IIR7 ($C_H = C_S = 1$ pF, $g_m = 0.125$ mS, $f_{ref} = 1$ GHz, and $f_s = 125$ MS/s).

the page. In these equations, each $-1/8$ in the discrete-time argument means one phase delay. At φ_7 , V_7 is a function of its value at previous cycle (-1 delay) and a sample V_6 that comes from the previous phase ($-1/8$ delay). Likewise, charge sharing equations from φ_1 to φ_6 are derived. Converting all these equations into z -domain, we can derive the following general equation for different outputs:

$$H_k(z) = \frac{V_k}{q_{in}} = \frac{1}{C_S} \cdot z^{-\frac{k-1}{8}} \cdot \prod_{i=1}^k \frac{1 - \alpha_i}{1 - \alpha_i z^{-1}} \quad (9)$$

for $k = 1, 2, \dots, 7$. In this equation, $\alpha_i = C_{H,i}/(C_{H,i} + C_S)$. Normally, we prefer to have all the poles identical and so we choose all the history capacitors of the same size $C_{H1-7} = C_H$. Then the transfer function of the main output (i.e., V_7) is simplified to

$$H(z) = \frac{V_{out}}{q_{in}} = \frac{1}{C_S} \cdot z^{-\frac{6}{8}} \cdot \left(\frac{1 - \alpha}{1 - \alpha z^{-1}} \right)^7 \quad (10)$$

From this equation, dc gain of V_{out} from the input charge, q_{in} , is $1/C_S$. Then, by using (6), the overall dc gain of this filter from the input voltage to its output is

$$A_V = \frac{V_{out}}{V_{in}} = g_m T_i \times \frac{1}{C_S} = g_m \times \frac{1}{C_S f_s} \quad (11)$$

In this equation, $T_i = T_s$ is the time period of the cycle, i.e., the 8 phases. Also, $1/(C_S f_s)$ is an equivalent dc resistance of the sampling capacitor. This filter has the same dc gain as the IIR2 filter in (7).

For frequencies much lower than f_s , we can use bilinear transform to obtain the continuous-time transfer function of the filter:

$$\frac{V_k(s)}{V_{in}(s)} = A_V \times \frac{1}{\left(1 + \frac{1}{C_S f_s} \cdot C_H \cdot s \right)^k} \quad (12)$$

This equation is similar to a transfer function of an RC LPF, i.e., $1/(1 + RCs)$. Poles of this equation are all located at $s = -C_S f_s / C_H$. It indicates that bandwidth of this filter only depends on the ratio of capacitors and the sampling frequency, thus making it much less sensitive to PVT variations. This salient feature eliminates any need of calibration, which is necessary for other filter types [12]–[17].

Transfer functions at the outputs of different orders are shown in Fig. 9. The slope of the 7th-order output transfer function reaches a maximum of 140 dB/dec for far-out frequencies.

D. Equalization of the Transfer Function

In many applications, the wanted signal could be accompanied by a strong interferer. Analog-intensive receivers traditionally use continuous-time (CT) Butterworth or Chebyshev type of filters with complex conjugate poles to select the wanted channel out of adjacent channels while filtering out interferers and blockers. In this way, most of the filtering is done in the CT

$$\begin{cases} @\varphi_7 : V_7[n] = \frac{C_{H7}}{C_{H7} + C_S} V_7[n-1] + \frac{C_S}{C_{H7} + C_S} V_6 \left[n - \frac{1}{8} \right] \\ @\varphi_6 : V_6 \left[n - \frac{1}{8} \right] = \frac{C_{H6}}{C_{H6} + C_S} V_6 \left[n - \frac{1}{8} - 1 \right] + \frac{C_S}{C_{H6} + C_S} V_5 \left[n - \frac{2}{8} \right] \\ \vdots \\ @\varphi_2 : V_2 \left[n - \frac{5}{8} \right] = \frac{C_{H2}}{C_{H2} + C_S} V_2 \left[n - \frac{5}{8} - 1 \right] + \frac{C_S}{C_{H2} + C_S} V_1 \left[n - \frac{6}{8} \right] \\ @\varphi_1 : V_1 \left[n - \frac{6}{8} \right] = \frac{C_{H1}}{C_{H1} + C_S} V_1 \left[n - \frac{6}{8} - 1 \right] + \frac{1}{C_{H1} + C_S} q_{in} \left[n - \frac{6}{8} \right] \end{cases} \quad (8)$$

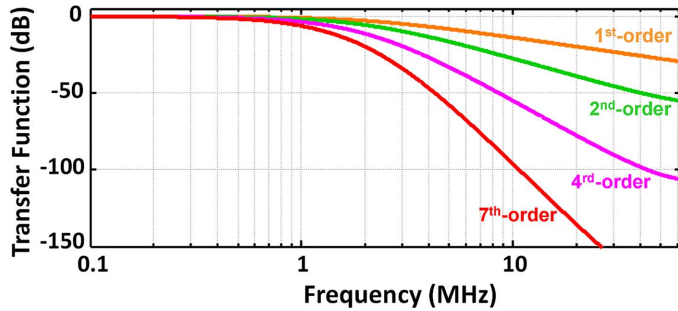


Fig. 9. Bode plot frequency response of the CR IIR7 ($C_S = 1$ pF, $C_H = 9$ pF, $g_m = 0.125$ mS, $f_{ref} = 1$ GHz, and $f_s = 125$ MS/s).

analog domain, and a low dynamic range ADC can be used afterwards. However, digitally intensive DT receivers distribute the channel select filtering between the pre-ADC analog filter and post-ADC digital filter. In [1]–[7], 2nd/3rd/6th-order real-pole analog filters are used before the ADC, and the rest of the filtering is done in digital domain with minimum power consumption. Considering a 3 dB BW, the transfer function of real-pole filters exhibits a gradual and smooth transition region between the flat pass-band into the sharp roll-off (see Fig. 10(b)). Therefore, the real-pole filters are used mostly to filter far-out interferers/blockers, while they have a moderate selectivity between wanted and adjacent channels.

The proposed DT CR filter could be converted *at the system level* to a sharp high selectivity filter (e.g., Butterworth) with digital assistance in the form of post-emphasis equalizer. The idea is to “pull in” the 3 dB cutoff frequency transition region of the analog filter to well within the channel and digitally compensate for the extra droop at the channel edges. The gradual roll-off region of the analog filter is masked by flattening it out in digital domain such that only the sharp roll-off remains. Fig. 10(a) shows the concept. The digital equalizer can be an all-pass IIR filter with 0 dB gain and a small peaking at a certain frequency, thus of insignificant incremental area and power penalty, especially in scaled CMOS. Transfer function of this filter is easily calculated by dividing the targeted total transfer function by the transfer function of the analog CR filter. In practice, its transfer function is merged with the existing digital part of the channel select filtering, sample-rate decimation, VGA, offset cancellation, I/Q mismatch compensation and demodulation [1], [3], [7].

An example is shown in Fig. 10(b). The equalizer is designed to map the 7th-order real-pole transfer function of the CR filter to a 5th-order Butterworth filter. The goal of this mapping is to flatten the passband of the overall transfer function, while keeping it unchanged or better for far-out frequencies. To maximally reduce power consumption, the digital equalizer operates in this example at a decimated rate of 10 MS/s while the analog CR filter runs at 800 MS/s. Note that the CR filter also serves as an effective anti-aliasing filter for the decimation.

The overall transfer function (including the analog filter and the digital equalizer), has a higher 3-dB bandwidth ($BW_{overall}$) than the real-pole analog filter itself (BW_{analog}). Consequently, the input signal undergoes some attenuation by the analog filter inside the overall passband, which is compensated by the small peaking of the digital equalizer. While the signal experiences an overall flat transfer function within the passband, the peaking

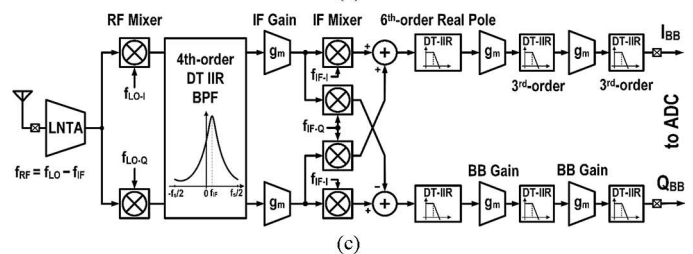
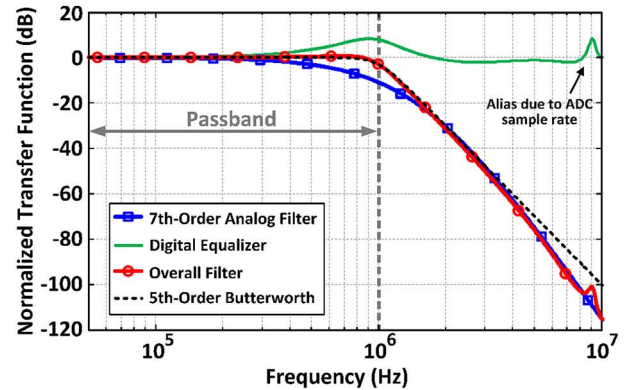
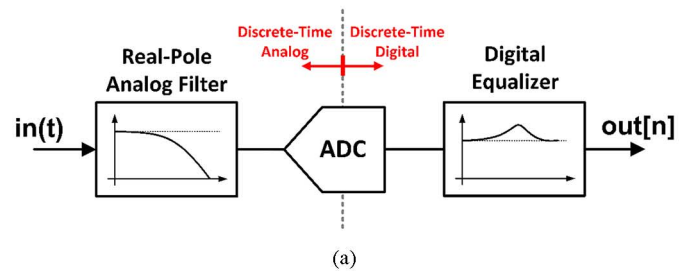


Fig. 10. (a) Proposed system for digital equalization of the filter transfer function. (b) An example of equalizing transfer function of a 7th-order real-poles DT CR filter and comparison with a 5th-order Butterworth. (c) An example implementation of a receiver utilizing a 6th-order charge rotating real-pole filter at the baseband [6].

increases noise at the transition region frequencies of both the analog filter and the ADC to some extent. To be able to compare the overall filter with a stand-alone CT analog filter, we consider that the overall filter transfer function is lumped before the ADC, but with a gain loss caused by the analog filter. This loss is equal to the RMS averaged value of transfer function of the digital equalizer within $BW_{overall}$.

Table I summarizes the analog gain loss for three different digital equalizers that map the 7th-order real-pole IIR filter to the 5th- to 7th-order Butterworth filters with a target 3-dB $BW_{overall}$ of 1 MHz. Due to large over-sampling ratio, the reported gain losses remain almost the same in case BW_{analog} and $BW_{overall}$ are scaled proportionally. Depending on the application, the order of the analog filter and the mapped transfer function should be chosen in a way that provides enough analog stopband attenuation and minimizes gain loss. In case when the ideal Butterworth filter characteristic is desired for the proposed real-pole filter, it might be necessary to increase the ADC dynamic range to compensate for the filter’s droop. For example, the ADC could require 0.8 to 1.8 extra ENOB, when the transfer function is mapped to the 5th- to 7th-order Butterworth, respectively.

TABLE I
MAPPING OF THE 7TH-ORDER REAL-POLE IIR FILTER TO THE OVERALL
(I.E., ANALOG AND DIGITAL) 5TH- TO 7TH-ORDER BUTTERWORTH FILTER OF
1 MHz 3 dB BANDWIDTH

Order of mapped Butterworth (1 MHz BW)	5th	6th	7th
3dB BW of analog filter (7 th -order, real-pole)	490 kHz	415 kHz	340 kHz
Gain loss (RMS averaged within 1MHz BW)	4.9 dB	7.2 dB	11.2 dB
Attenuation of analog filter @ 2 / 4 MHz	31 / 64 dB	37 / 75 dB	43 / 85 dB

System functionality of the proposed charge rotating filter has been verified in a discrete-time superheterodyne receiver [6], where the identical 6th-order version is employed as the first baseband channel selection filter. The simplified receiver structure is shown in Fig. 10(c). Thanks to the low noise characteristic of this filter, the total receiver has achieved a noise figure of only 3.2 dB, in addition to a good linearity of IIP3 = -7 dBm that is by no means limited by the high linearity of the baseband filter.

E. Sampling Rate Increase

Sampling rate of the Fig. 7(b) CR filter is one sample per cycle, with each cycle comprising 8 phases. Therefore, the sampling frequency f_s is $f_{ref}/8$. By increasing the sampling rate, the frequency folding would be pushed higher, thus making it less of a concern. Also, the filter can achieve a wider bandwidth.

Operation of the CR IIR7 filter as shown in Fig. 7(b) can be considered as 8 different stages in series. As new data arrives at φ_1 , it is sequentially processed at each stage until φ_8 . Only then the next data sample arrives. As history capacitors C_{H1-7} are holding the data between different stages, we are able to readily increase the data rate by *pipelining*.

Suppose that instead of only one C_S , we have now 8 sampling capacitors, each of them connected to one of the “history” nodes. Then, by going to the next phase, all of them are moving to the next node in the clockwise direction. At each new phase of this pipeline structure, a new data ($q_{in}[n]$) comes into C_{H1} , a new data is transferred from C_{H1} to C_{H2} , from C_{H2} to C_{H3} and so on until C_{H7} , and one sampling capacitor is reset to ground. Therefore, a new data comes in and a new data comes out at each phase (instead of each cycle). In this way, functionality of the filter has not changed while its sampling rate has increased by 8 times ($f_s = f_{ref}$). Schematic of this full-rate CR IIR7 filter is shown in Fig. 11. For each sampling capacitor and its rotation network, a separate switch bank is used.

The pipeline SC structure has the same charge sharing, transfer function and gain equations as (8)–(11), but with replacing each 1/8 delay with a unit delay and considering the new f_s .

In this filter, if there is a mismatch between different C_H , it would slightly shift the pole locations. Since these capacitors have typically a large value and are of the same type, they are very well matched, thus removing the matching concern. However, if the mismatch exists between the different C_S in the pipeline structure, it could alias some amount of signal from harmonics of $f_{ref}/8$ inside the passband. However, any signal

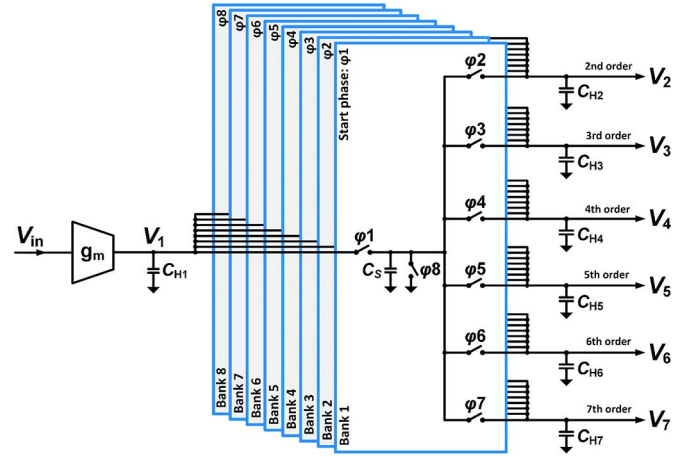


Fig. 11. Full-rate CR IIR7 filter using pipelining ($f_s = f_{ref}$).

around the harmonics is filtered before the aliasing. In practice, this non-ideal effect is too small to be observed.

F. Noise

Output noise of the charge rotating 7th-order DT filter contains two main contributors: noise of the input gm-cell and noise of the passive switched-capacitor network. In a process similar to Fig. 4(a), noise of the gm-cell is shaped by the anti-aliasing filter, sampled and then shaped by the filter transfer function. Higher order filtering leads to more noise filtering outside the passband.

Although it is beyond the scope of this paper, it can be shown through hand calculations, and verified through noise simulations, that the in-band noise of the proposed passive switched-capacitor circuit is $4kT/(C_S f_s)$ for $C_H \gg C_S$, and remains the same irrespective of the filtering order. Consequently, one can arbitrarily increase the filtering order without increasing its output noise, which is a key advantage over the conventional filters, where each order increase implies more noise (e.g., more resistors and opamps in an active-RC filter).

G. Robustness to PVT Variations

Active-RC and *Gm-C* filters are quite sensitive to PVT variations because of poor matching between different types of elements (i.e., resistor, capacitor and gm-cell). However, switched-capacitor filters are quite robust to PVT variations. Transfer function and BW of SC filters are set by capacitor ratio, which are normally implemented of the same device type (e.g., MOS, MiM, or MoM capacitor). Active-SC filters are very robust to PVT, especially when parasitic capacitance cancellation techniques (e.g., correlated double sampling) are used.

In the proposed passive SC filter, the effective C_S is provided by MoM type of capacitor and also parasitic capacitance of 8 MOS switches connected to it (see Fig. 11). In this design, 8% to 26% of C_S is the MOS parasitic capacitance, depending on a C_S value selection code. On the other hand, C_H has also some switches to select its value. In this design, MOS parasitic capacitance connected to C_H ranges from 0.5% to 20%, depending on the C_H selection code. Being subject to the PVT variation, MoM part of the effective C_S and C_H track each other very well. Also, their common percentage part of the remaining MOS parasitic capacitance matches well (they are of the same type).

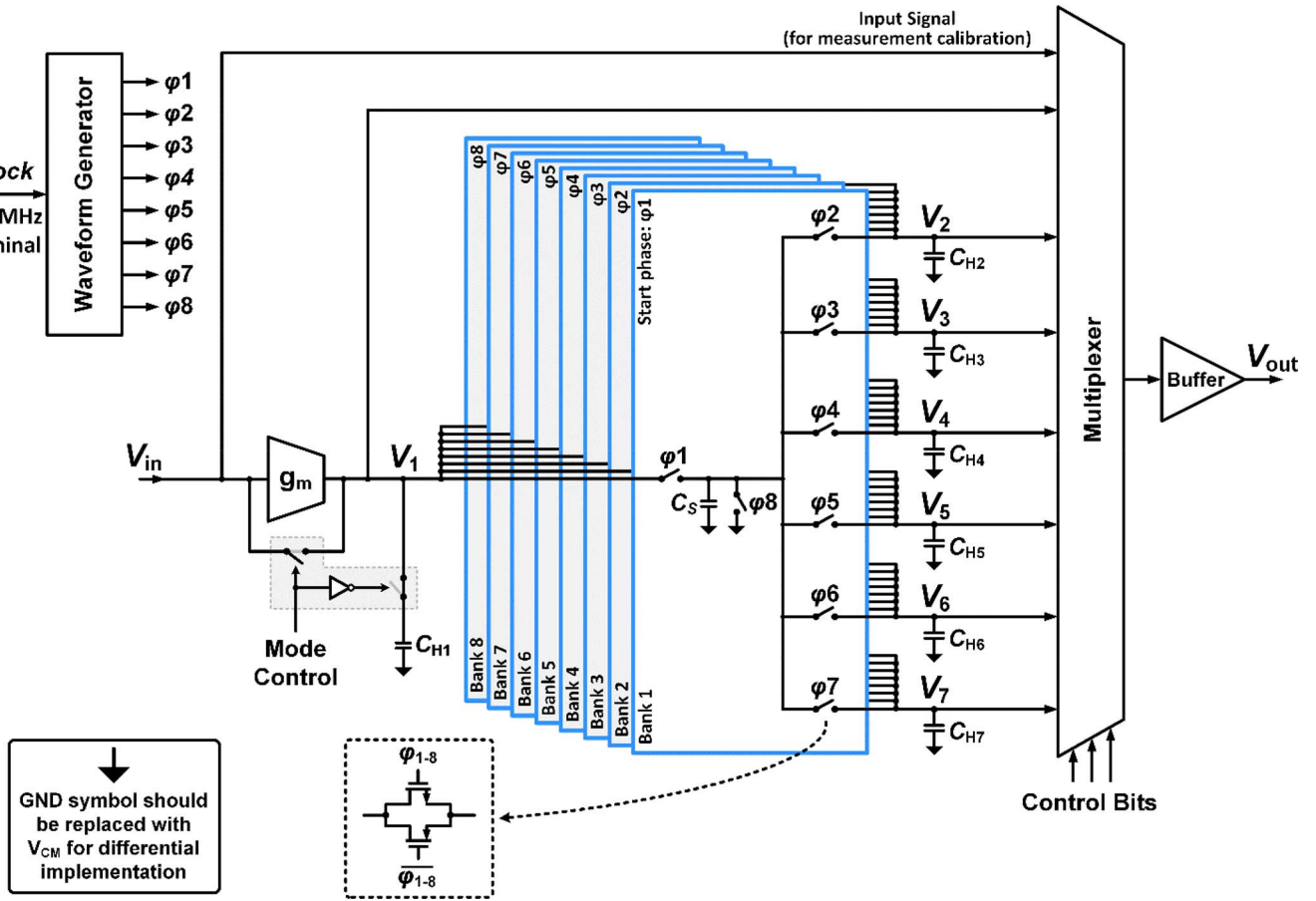


Fig. 12. Implementation of the full-rate CR IIR7. The circuit has been implemented differentially while it has been shown single-ended here for simplicity.

The only part that could be affected by PVT variation is the difference between the MOS parasitic capacitance percentages of C_S and C_H . Depending on the selected C_S and C_H codes, this difference is limited to a few percent of the whole capacitance. In this way, PVT variation effect is reduced, but still somewhat higher than an active-SC filter.

IV. DESIGN AND IMPLEMENTATION

The proposed high-order charge-rotating DT filter consists of a gm-cell, switches, capacitors and a clock waveform generator circuit. Therefore, it is amenable to the digital deep nanoscale CMOS technology. If we implement this filter in a finer process, area of the capacitors, switches and the waveform generator reduces while preserving or improving the performance according to Moore's law of scaling.

A. Design of the 7th-Order Charge Rotating DT Filter

The final design is implemented differentially while, for the sake of simplicity, it is shown single-ended in Fig. 12. The designed filter is software-controlled to operate in one of the two modes: 1) charge-sampling or 2) voltage-sampling. Although in the charge-sampling mode we have an active gm-cell, the filtering network is fully passive, making the overall filter semi-passive. In the voltage-sampling mode, the gm-cell is bypassed and disconnected from the power supply, resulting in a fully passive filter. Also, C_{H1} is disconnected via "Mode Control"

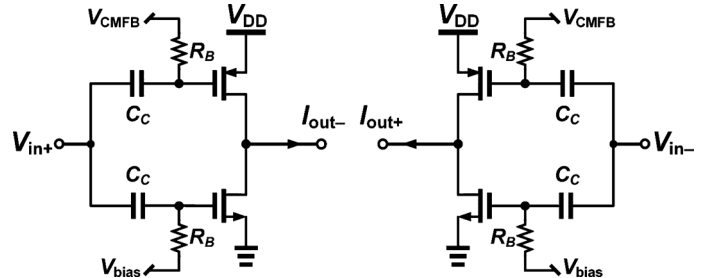


Fig. 13. Inverter-based pseudo-differential gm-cell.

to prevent loading the input. The removal of C_{H1} lowers the filtering order by one to 6th.¹ In this mode, the input voltage (instead of the input charge) is directly sampled by C_S capacitors.

The simple inverter-based gm-cell (Fig. 13) makes the filter amenable to process scaling. In this pseudo-differential gm-cell, a bias voltage V_{bias} comes from a diode-connected NMOS and mirrors a bias current into the gm-cell. Also, a feedback circuit sets the common-mode output voltage to $V_{DD}/2$ by adjusting V_{CMFB} . Coupling capacitors C_C and bias resistors R_B set a lower limit in frequency response. By using large C_C and R_B , this limit is pulled down to a few kHz, which is acceptable for most applications. As the gm-cell, a simple inverter is used to be amenable to scaling and provide

¹The 7th order of the filter in voltage-sampling mode can be kept by replacing GND with a history capacitor at ϕ_8 . However, we did not do this in the current implementation.

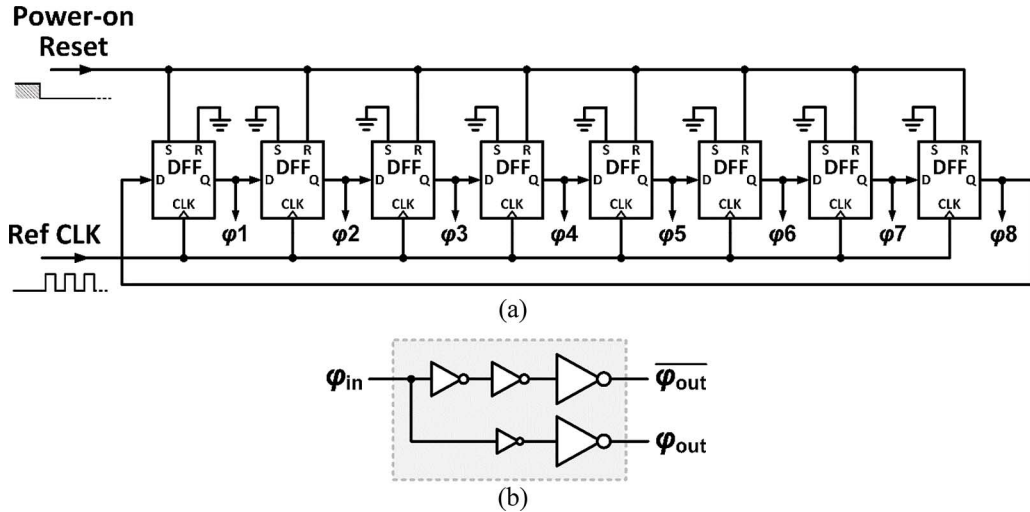


Fig. 14. (a) Waveform generator circuit with (b) its output buffer.

a good linearity. By properly sizing NMOS and PMOS transistors, their nonlinearities could be canceled out perfectly for square-law transistors [23]. However, in nanoscale CMOS, a partial cancellation is carried out. We have used transistors with a large channel length to make their behavior closer to the square-law model. Moreover, a low resistance load by the SC circuit allows a high IIP3.

The differential history capacitors C_{H1-7} range from 0.25 to 64 pF digitally selectable via 8 bits. For both history and sampling capacitors, we used MOM capacitors to have a very good matching. This minimizes variations due to PVT. Differential value of the sampling capacitors C_S range from 0.4 to 2.2 pF digitally selectable by 4 bits. Instead of implementing C_S differentially, we implement each as two single-ended capacitors. Then we can set the common-mode voltage of the filter by terminating C_S to V_{CM} instead of ground. To adjust the filter bandwidth, we keep C_S fixed and change C_H . In this way, both the gain and linearity of the circuit do not change. Also, if the sampling frequency is changed, we change C_S inversely to keep the bandwidth and the gain constant.

As shown in Fig. 12, the filter's switches are implemented with transmission gates. We have chosen equal NMOS and PMOS sizes to reduce charge injection and cancel out clock feedthrough by at least an order of magnitude [24], [25], and at the same time having a lower on-resistance (R_{on}). To have a low R_{on} , low- V_T transistors are chosen. These transistors should be sized carefully to have a low enough R_{on} for fast settling on the sampling capacitors.

The waveform generator shown in Fig. 14(a), is a digital logic block. It consists of eight D-flip-flops (DFFs). At power-on, the DFFs are set/reset to "10000000". Then, at each successive clock cycle, the code is rotated one step. In this way, all the required phases are generated from a reference clock. Outputs of the DFFs are fed to buffer cells before driving the switches (Fig. 14(b)). The buffer is able to drive the switches with sharp rising and falling edges. The sizes of the NMOS and PMOS transistors in the buffer are skewed to ensure non-overlapping between consecutive phases.

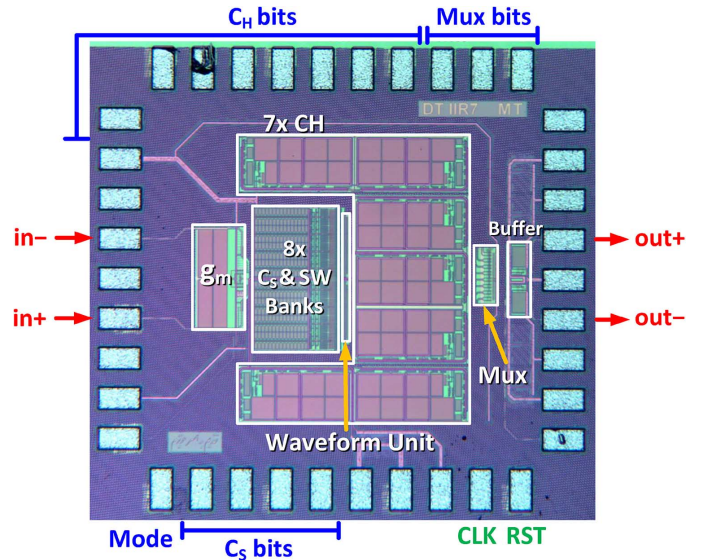


Fig. 15. Chip micrograph of the full-rate CR IIR7 implemented in TSMC 65 nm CMOS. Die size is 1.2×1.27 mm.

B. Implementation

The filter has been implemented in TSMC 1P7M 65 nm CMOS process. It operates at a 1.2 V power supply. The gm-cell drains $250 \mu\text{A}$. The waveform generator unit and its buffers clocked at a reference frequency f_{ref} of 800 MHz consume 1.40 mA. The latter current consumption is proportional to f_{ref} . The filter has been verified to work properly up to 1 GS/s.

As shown in Fig. 12, an analog multiplexer is added to allow monitoring different outputs (orders) of the filter as well as the internal on-chip input of the filter. After the multiplexer, an output buffer isolates the chip internals from the outside. Fig. 15 shows a chip micrograph of the implemented filter.

V. MEASUREMENT RESULTS

To verify the proposed filter, a single-ended input signal is converted to differential with a wideband transformer, terminated with a 50Ω resistor on the PCB and then fed to the chip.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

	This Work				JSSC'11 [15]	JSSC'10 [14]	JSSC'09 [13]	JSCC'06 [12]	JSSC'06 [16]	JSSC'07 [17]
Topology	DT IIR @ 800MS/s				G_m -C, Low Power Hi. Linearity	G_m -C, Noise Reduction	G_m -C, Wide Tuning	Source Follower	Active RC	Active RC
	Charge-Sampling		Voltage-Sampling							
	without Equalizer	with Equalizer	without Equalizer	with Equalizer						
Technology	65nm		65nm		90nm	90nm	0.18 μ m	0.18 μ m	0.12 μ m	0.13 μ m
Order	7th	5th	6th	4th	6th	4th	3rd	4th	3rd, 5th	5th
Type	Real Poles	Butter.	Real Poles	Butter.	Butterworth	Butterworth	Butterworth	Butterworth	Cheb. Elliptic	Chebyshev
Supply Voltage (V)	1.2		1.2		1.0	2.5	1.2	1.8	1.0	1.5
Power (mW)	1.98	-	1.68	-	4.35	1.25	4.1 – 11.1*	4.1	4.6	11.25
3dB BW (MHz)	0.4 – 30	0.82 – 61	0.43 – 32	0.77 – 57	8.1 – 13.5	2.8	0.5 – 20	6 – 14	5, 10	8.9, 19.7
Gain (dB)	9.3	4.4	0	-3.5	-2.7	15	0	-3.5	0	2
Max. Stopband Rejection (dB)	>100		>85		\approx 90	55	60	-	50	-
In-band / Out-of- band IIP3 (dBm)	21.7 [†] / 11.7 [‡]		24 [†] / 25 [‡]		21.7 – 22.1 / 17.5 – 18.9	10 / 35.6	22.3 – 19 / 17.5 – 13*	18 / 12	18.8 – 21.3 / -	18.3 / -
In-band / Out-of- band IIP2 (dBm)	55 [†] / 60 [§]		61 [†] / 68 [§]		- / 51.9 – 53.4	- / -	40 – 30.8* / -	- / -	- / -	- / -
$P_{1dB,out}$ (dBm)	+10		+13		+3.9	-	-	0.5	-4.1 – 2.6	+7
IRN (nV/ \sqrt Hz)	4.57	4.72	4.97	7.27	75	22.6	425 – 12*	7.5	85, 143	30
SFDR (dB)	75 – 68*	74 – 66*	82 – 69*	77 – 66*	54.3	58	51 – 61	65	-	55.2
1% HD3 DR (dB)	93 – 81*	91 – 79*	103 – 83*	96 – 78*	63	67	80	79	-	69
Active Area (mm ²)	0.42		0.35		0.239	0.5	0.23	0.26	0.17	0.2

* In the same order of the filter BW † 3 MHz and 4 MHz tones ‡ 20 MHz and 35 MHz tones § 30 MHz and 35 MHz tones

Differential output of the chip with zero-order-hold is converted back to a single-ended signal with another transformer. Table II summarizes the filter performance in its two operational modes, including the effects of the suggested digital equalizer, and compares with recent state-of-the-art filters.

The transfer function of the filter has been evaluated using an HP8753E network analyzer. To lower the measurement noise floor, a wideband RF amplifier (HP8347A) was used. Fig. 16(a) plots the measured frequency response of the filter in the charge-sampling mode at the 7th-order output for different bandwidth settings. The 3 dB bandwidth is programmable from 400 kHz to 30 MHz. By applying a digital equalizer to map the transfer function to a 5th-order Butterworth, the overall 3 dB bandwidth would be tunable from 0.82 to 61 MHz. As an example, the overall transfer function including the equalizer is plotted with the black dashed line in Fig. 16(a). A maximum 100 dB of stop-band rejection is measured for the narrowest bandwidth setting. Depicted in Fig. 16(b) is the measured transfer function of the filter in the charge-sampling mode, but now for different outputs (orders). In this measurement, the 400 kHz analog bandwidth setting is used. The measured 7th-order output is also

compared with the ideal mathematical transfer function shown by the black dashed line, indicating a very good agreement with theory. The transfer function of the filter in the voltage-sampling mode is similar to that shown in Fig. 16 except that the filtering order is 6th.

To evaluate the linearity of the filter, a two-tone signal is fed to the filter and its output is evaluated by an Agilent E4446A spectrum analyzer. For this test, the analog bandwidth is set to about 9 MHz. Fig. 17 shows the measured 2nd- and 3rd-order intermodulation products versus the input power for both charge-sampling and voltage-sampling modes. Measured IIP2 and IIP3 (with respect to 50 Ω) are +55 dBm and +21 dBm in charge-sampling mode, and +61 dBm and +24 dBm in voltage-sampling mode. In the charge-sampling mode, where the linearity is limited by the gm-cell, IIP3 might be lowered by a few dBs in practice, caused by PVT variations. As listed in Table II, IIP3/IIP2 in the charge-sampling mode is among the best. Thanks to the fully passive operation, the filter in the voltage-sampling mode has an exceptionally high IIP3/IIP2.

To be able to fairly compare the 1 dB compression point of our filter in its two operational modes to other filters with

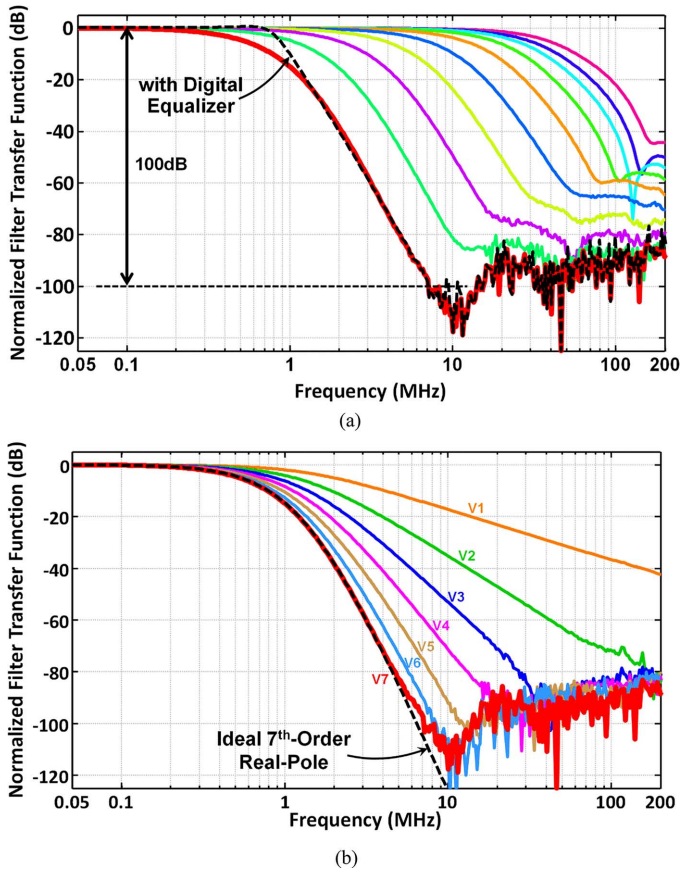


Fig. 16. Measured transfer function of the CR IIR7 for (a) the 7th-order output with different BW settings, and (b) for different orders in 400 kHz BW setting. The filter is in charge-sampling mode clocked at 800 MHz.

various gains, we compare the output compression point as $P_{1\text{dB},\text{out}} = P_{1\text{dB},\text{in}} + \text{Gain} - 1$. The measured output compression point of the filter in the charge-sampling mode is +10 dBm. In the voltage-sampling mode, this value goes to +13 dBm. These are outstanding values compared to the other works listed in Table II.

The noise of the filter is evaluated by the spectrum analyzer. For this measurement, the input of the filter is grounded. A two-step experiment is carried out: 1) measuring the total output noise (including noise of the filter and output buffer), 2) disabling the filter and measuring the noise of only the output buffer. Then, since the noise of the buffer and the filter are uncorrelated, the filter noise is calculated by subtracting the total noise power spectral density (PSD) and the buffer noise PSD.

Fig. 18(a) shows the measured input-referred noise (IRN) spectral density of the filter in the charge-sampling mode for the 9 MHz $\text{BW}_{\text{analog}}$ setting ($C_S = 0.75$ pF, $C_H = 2.35$ pF). The slope below 1 MHz is due to the flicker and bias noise of the gm-cell. Noise between 1 MHz and 20 MHz is mainly the thermal noise of the gm-cell shaped by the filter transfer function, and the rest is dominantly noise of the switched-capacitor circuit. The averaged spot noise over the bandwidth is 4.57 nV/ $\sqrt{\text{Hz}}$. Integrated noise, P_N , from 50 kHz to 9 MHz is 13.6 μV_{RMS} , which increases to 16.4 μV_{RMS} for the entire frequency range. This gives a 71 dB spurious-free dynamic range (SFDR) as defined in [26]. As measured by a single-tone test,

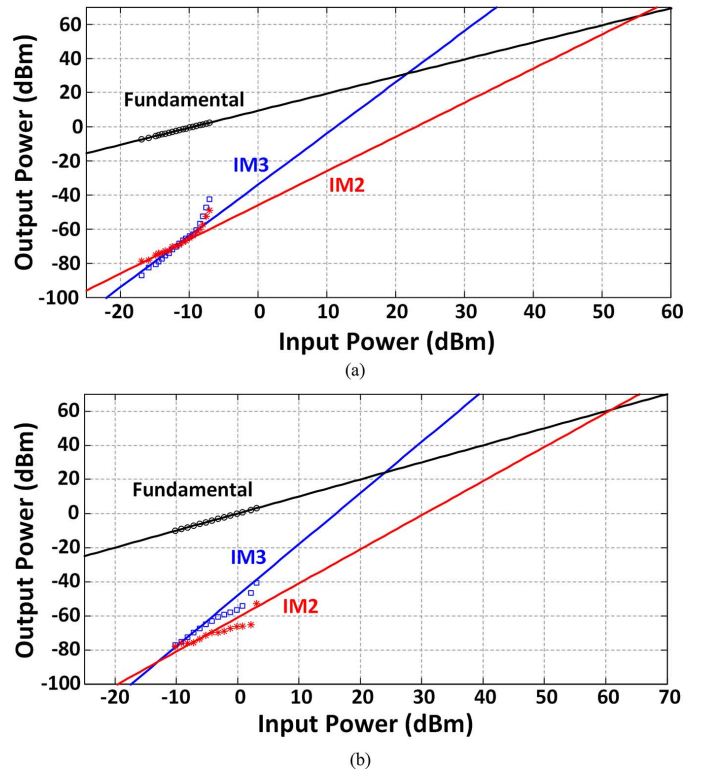


Fig. 17. In-band IIP2 and IIP3 measurement of the CR IIR7 filter in (a) charge-sampling and (b) voltage-sampling modes.

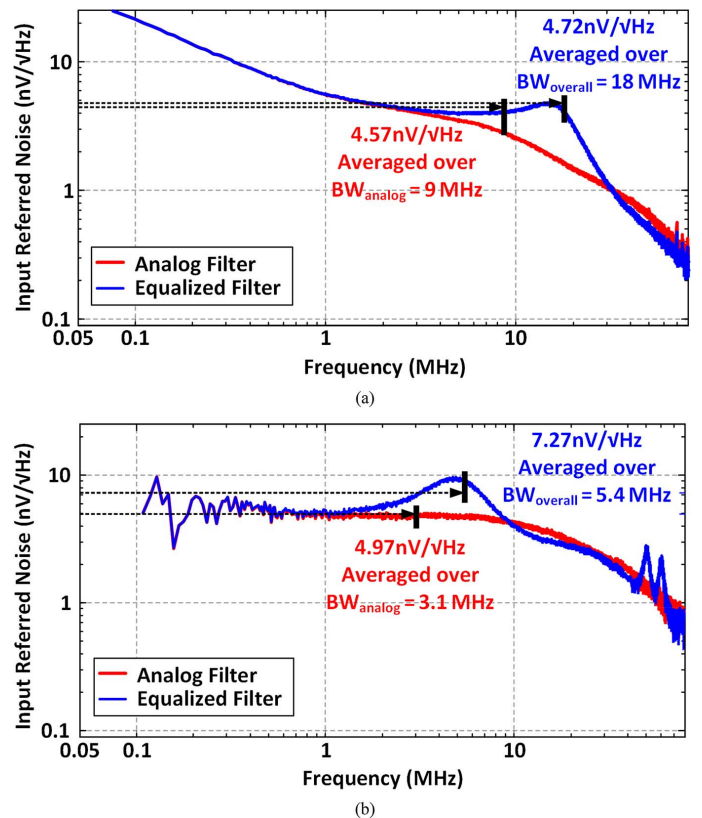


Fig. 18. Measured input-referred noise of the filter in (a) charge-sampling and (b) voltage-sampling mode.

a -3.5 dBm input signal (422 mV peak-to-peak differential) creates -40 dB 3rd-harmonic distortion (HD3) at the output,

giving an 81 dB dynamic range (1% HD3 DR). By applying the digital equalizer to map the analog transfer function to a 5th-order Butterworth, the equivalent IRN of the total filter increases to 4.72 nV/ $\sqrt{\text{Hz}}$, resulting in 68 dB SFDR for 18 MHz BW_{overall} .

Measured input-referred noise of the filter in the voltage-sampling mode for the 3.1 MHz BW_{analog} ($C_S = 0.75$ pF, $C_H = 8.25$ pF) is illustrated in Fig. 18(b). In this mode, the whole noise spectrum is due to the switched-capacitor network. The spot IRN averaged over the bandwidth is 4.97 nV/ $\sqrt{\text{Hz}}$. The integrated IRN over the bandwidth is 8.6 μV_{RMS} and rises to 22.2 μV_{RMS} for the entire frequency range. This results in 75 dB SFDR. As measured, a single tone input signal as large as 8.8 dBm (1.75 V peak-to-peak differential) creates 1% HD3 in this mode. This results in 97 dB dynamic range. By mapping the 6th-order real-pole transfer function of this filter to a 4th-order Butterworth using the equalizer, the overall IRN of the filter rises to 7.27 nV/ $\sqrt{\text{Hz}}$ giving 71 dB SFDR for 5.4 MHz BW_{overall} .

Measured clock feedthrough at the output of this filter is less than -110 dBm at $f_{\text{ref}}/8 = 100$ MHz. This very low value avoids any noise and spur problems caused by the clock signal.

VI. CONCLUSION

In this paper, a high-order discrete-time (DT) charge rotating (CR) IIR filter structure is proposed and experimentally verified. The implemented 7th-order charge-sampling/6th-order voltage-sampling DT filter is elaborated in detail. The order of this filter is easily extendable to even higher orders. Using a pipelining techniques, sample rate of the filter is increased up to 1 GS/s. The CR filter is process-scalable according to Moore's law and friendly to digital nanoscale CMOS technology. Transfer function of this filter is precise and robust to PVT variations. Even though the CR filter features real poles, modern system applications, such as wireless receivers, could expend digital post-processing to equalize the droop at the pass-band edge of the transfer function. Its state-of-the-art performance includes: very low power consumption, the lowest input-referred noise, very wide tuning range and excellent linearity.

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