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Nonlinear Dynamics of Alias-Locked Loop

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Abstract—This paper examines the nonlinear dynamics of an alias-locked loop (ALL) which uses an aliasing divider instead of a traditional frequency divider in the feedback loop of a phase-locked loop. A nonlinear model of the ALL is developed and used to study the global and local nonlinear dynamics of the system. In the global dynamics, we see disconnected regions of stability, which arise as a direct result of the aliasing operation. In the local dynamics, we see how the orbits observed have a particular dependence on the ratio of sample and reference frequencies.

I. INTRODUCTION

Phase-locked loops (PLLs) are closed-loop negative-feedback systems used throughout many areas of electronics, particularly communication applications such as frequency synthesis and clock and data recovery. Recent research has seen significant attempts to provide useful insight into the complicated dynamics of PLLs through the application of nonlinear theory [1-3].

Typically, charge-pump phase-locked loop frequency synthesizers use an N frequency divider in the feedback path of the PLL [4-5]. A new structure, the *alias-locked loop* (ALL), drawing on some ideas from [6], was proposed in [7]. The traditional divider in the feedback path is replaced by a high-speed binary sampling circuit which relies on a stable sample clock to sample the VCO signal. The subsampled VCO signal will be aliased because the sample rate is lower than the VCO signal. Based on the alias-locked loop architecture, it is possible to create high-speed frequency synthesis circuits which can operate at frequencies in excess of 60 GHz.

This paper examines the nonlinear dynamical behaviour exhibited by the alias-locked loop (ALL) from [7]. Section II discusses the ALL architecture and its model. Section III investigates the global dynamics and Section IV the local dynamics of the ALL. In examining the local dynamics, we consider in turn the cases where the ratio of sample and reference frequencies is integer, low-denominator rational and large-denominator rational.

II. ALIAS-LOCKED LOOP CIRCUIT MODEL

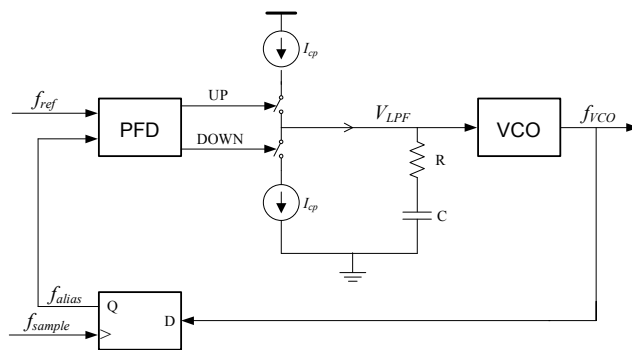


Fig. 1. Block diagram of alias-locked loop.

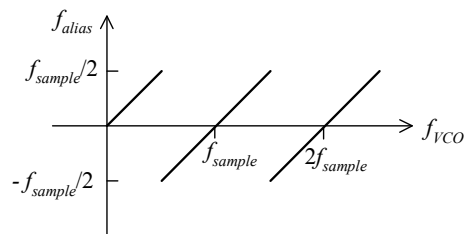


Fig. 2. Frequency produced by aliasing divider

The block diagram of the ALL studied in [7] is shown in Fig. 1. The key element that distinguishes this loop from traditional structures lies in the feedback path. Here, the VCO signal at frequency f_{VCO} is subsampled at a much lower frequency f_{sample} , generating an alias frequency

$$f_{alias} = f_{VCO} - f_{sample} \cdot \text{round}(f_{VCO}/f_{sample}) \quad (1)$$

plotted in Fig. 2. Thus, where a traditional PLL with a frequency divider in the feedback path aims to lock into a frequency divided version of the VCO output signal, the ALL aims to lock to the low-frequency alias of the VCO signal, generated as in (1).

The phase-frequency detector (PFD) detects the phase difference between the alias signal and the reference signal. The charge-pump converts the PFD control signal to a voltage difference on the loop filter, which in turn tunes the VCO until the ALL locks into the low frequency alias of the VCO signal.

III. GLOBAL DYNAMICS OF THE ALL

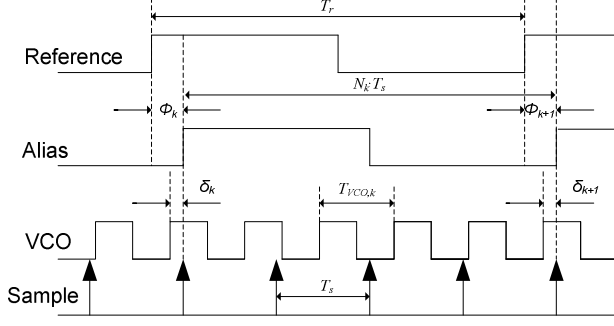


Fig. 3. Time diagrams of the signals in the alias-locked loop (from [7]).

The alias-locked loop to be examined in this paper is described in [7]. In order to understand the behavioral model, let us consider the waveforms shown in Fig. 3. In this model, δ is defined as the offset between the rising edge of the VCO clock and the sampling signal and Φ is the offset between the rising edge of the reference clock and the rising edge of the aliased signal.

We define by N_k the number of samples during one alias period.

$$N_k = \left\lceil \frac{T_{VCO,k} - \delta_k}{\text{remainder}(T_s, T_{VCO,k})} \right\rceil \quad (2)$$

When δ_k has cycled through one period of the VCO clock, one alias period is completed. δ_{k+1} is given by the equation

$$\delta_{k+1} = \delta_k + N_k \cdot \text{remainder}(T_s, T_{VCO,k}) - T_{VCO,k} \quad (3)$$

The phase error is augmented at each step by the difference between the reference clock period and the alias period:

$$\phi_{k+1} = \phi_k + N_k \cdot T_s - T_r \quad (4)$$

The difference equation to calculate $V_{LPF,k+1}$ is given by

$$V_{LPF,k+1} = V_{LPF,k} + I_{cp} \cdot \phi_{k+1} / C \quad (5)$$

where I_{CP} is the charge-pump current and C (along with R) can be seen in the loop filter of Fig. 1.

In calculating the operating frequency of the VCO, we follow the simplification in [7] where the voltage on the LPF is represented by its average value

$$V_{ave,k+1} = I_{cp} \cdot \phi_{k+1} / T_r \cdot [R + |\phi_{k+1}| / 2 \cdot C + (T_r - |\phi_{k+1}|) / C] + V_{LPF,k} \quad (6)$$

and the VCO frequency (the reciprocal of the VCO period) is given by

$$f_{VCO,k+1} = f_0 + K_v \cdot V_{ave,k+1} \quad (7)$$

In this section we examine the global dynamics of the system modelled by equations (2-7) from Section II. The underlying dynamics are three-dimensional, with the additional three equations used to calculate intermediate variable for the equations. Because of their complexity, these equations yield little immediate insight into the behaviour of the ALL system, and so we present here the results of a thorough numerical investigation of their dynamics. To be consistent with (7), we present our results in the two-dimensional plane spanned by ψ and V_{LPF} , where the former is the difference between Φ and δ . In particular, we take the section through the three-dimensional state-space where $\delta=0$.

We know from [7] that for certain parameter values and certain initial conditions trajectories of the system defined by equations (2-7) will converge to a periodic orbit, in the manner shown in Fig. 4(a). This figure, like those in [7], uses parameter values $\zeta = T_r/T_s = 10$, $T_s = 1\text{ns}$, $f_0 = 10\text{GHz}$, $K_v = 1.0\text{GHz/V}$, $R = 89\Omega$, $C = 1.27\text{nF}$ and $I_{cp} = 20\mu\text{A}$. The parameter ζ will be important in our later discussions. The initial conditions for the trajectory of Fig. 4(a) are $\Phi(0) = -0.5\text{ns}$, $\delta(0) = 0$ and $V_{LPF}(0) = 0.25\text{V}$. However, if $V_{LPF}(0)$ changes to 0.2586V , the trajectory diverges, as shown in Fig. 4(b). Changing $V_{LPF}(0)$ to 1.25V we get the behaviour shown in Fig. 5(a), where the trajectory is qualitatively similar to that in Fig. 4(a), but is now converging to a small region around $V_{LPF} = 1.1\text{V}$ rather than $V_{LPF} = 0.1\text{V}$. Changing $V_{LPF}(0)$ to 1.2586V again leads to instability, as shown in Fig. 5(b).

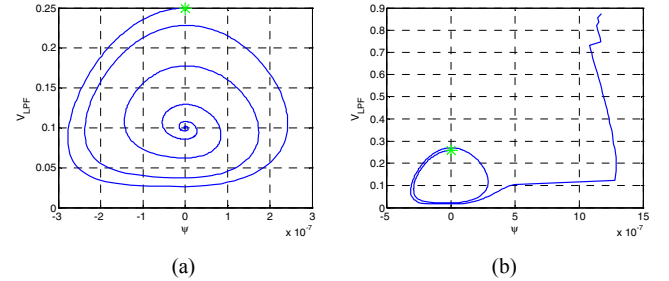


Fig. 4. Trajectories of (2-7) with $\zeta = T_r/T_s = 10$, $T_s = 1\text{ns}$, $f_0 = 10\text{GHz}$, $K_v = 1.0\text{GHz/V}$, $R = 89\Omega$, $C = 1.27\text{nF}$ and $I_{cp} = 20\mu\text{A}$. The initial conditions are $\Phi(0) = -0.5\text{ns}$, $\delta(0) \approx 0$, $V_{LPF}(0) =$ (a) 0.25V and (b) 0.2586V .

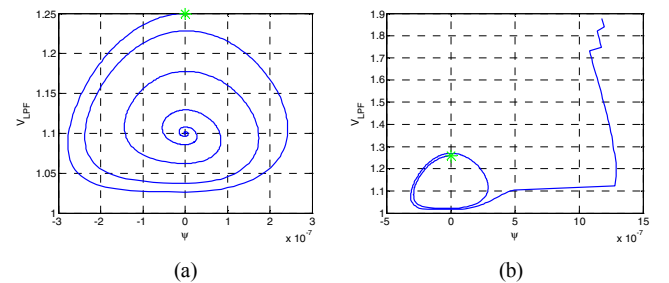


Fig. 5. Trajectories of (2-7) with parameters as in Fig. 4, but $V_{LPF}(0) =$ (a) 1.25V and (b) 1.2586V .

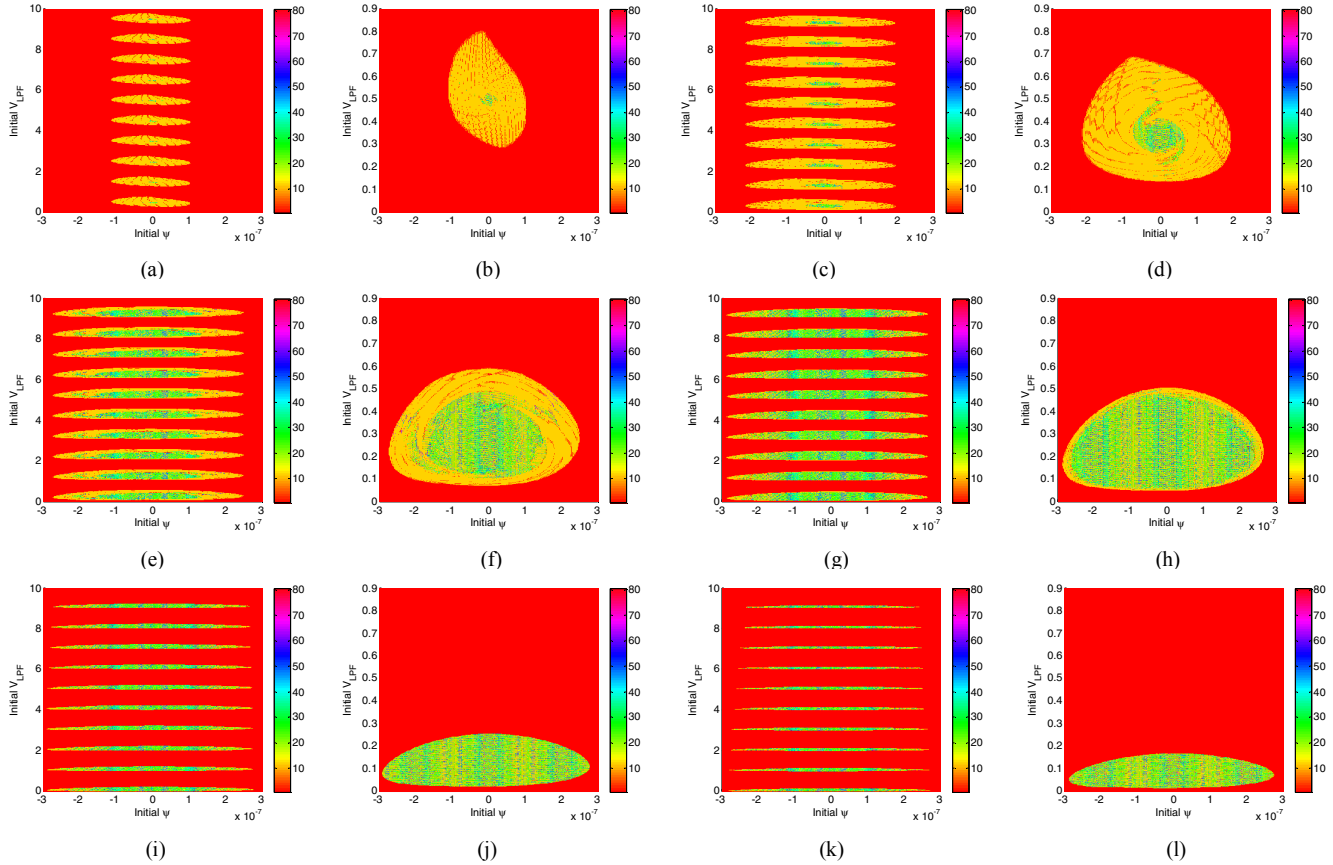


Fig. 6. Basins of attraction of periodic orbits for integer values of ζ and other parameters as in Fig. 4. (a, b) $\zeta=2$, (c, d) $\zeta=3$, (e, f) $\zeta=4$, (g, h) $\zeta=5$, (i, j) $\zeta=10$, (k, l) $\zeta=15$.

It is clear, therefore, that there are regions of stability and instability for the system of Section II. These are plotted in Fig. 6 on the basis of simulations of equations (2-7) for values of ζ ranging from 2 to 15, and $\delta(0) = 0$ – the red indicates the region of instability. Note how the stability region first increases and then decreases in size with ζ , until for values of ζ larger than about 73 there is no stability region.

Note also that the stability region consists of disconnected regions, as suggested by Figs. 4 and 5. This is because, as seen in Fig. 2, the same value of f_{alias} can correspond to different values of f_{VCO} . For example, with the parameters of Figs. 4 and 5, trajectories converge to a region around $V_{LPF} = 0.1$ V or $V_{LPF} = 1.1$ V. These correspond to values of f_{VCO} around 10.1 and 11.1 GHz. These frequencies are separated by one sampling frequency, both giving the same alias frequency around 10^8 Hz, which is the reference frequency to which the loop locks. If we consider the case where ζ is 2, say, rather than 10 as in Figs. 4 and 5, trajectories converge to a region around $V_{LPF} = 0.5$ V, 1.5 V, 2.5 V, etc. These values all give the same alias frequency of 0.5GHz, which is the value of the reference frequency in this case. Thus the disconnected “islands” of the stability region correspond in a natural way to the aliasing action of the frequency divider, with their centres and separation as predicted from an understanding of the aliasing process.

IV. LOCAL DYNAMICS OF THE ALL

Within the stability region of the ALL, different forms of behaviour can be seen. In Fig. 6, which considers a range of integer values of ζ , the basins of attraction for different period orbits can be seen, graded by colour.

Fig. 7 plots typical periodic orbits of the system modelled by equations (2-7) for three different values of ζ – an integer, a nearby low-denominator rational and a nearby large-denominator rational. Changing ζ in a small neighbourhood in this way does not materially change the stability region, but it does, as is clear from the figure, have a significant effect on the periodicity of the orbits observed.

The reason for this is clear from equation (4), which shows how the minimum number of iterations needed for values of Φ to repeat depends on the denominator of the ratio of T_r to T_s , namely ζ . A similar effect was observed and studied in [8] for a different PLL system – once again arising as a result of a discontinuous shift in the phase error variable. Development of a fuller analytical description of this behaviour in the case of the ALL is the focus of our ongoing work.

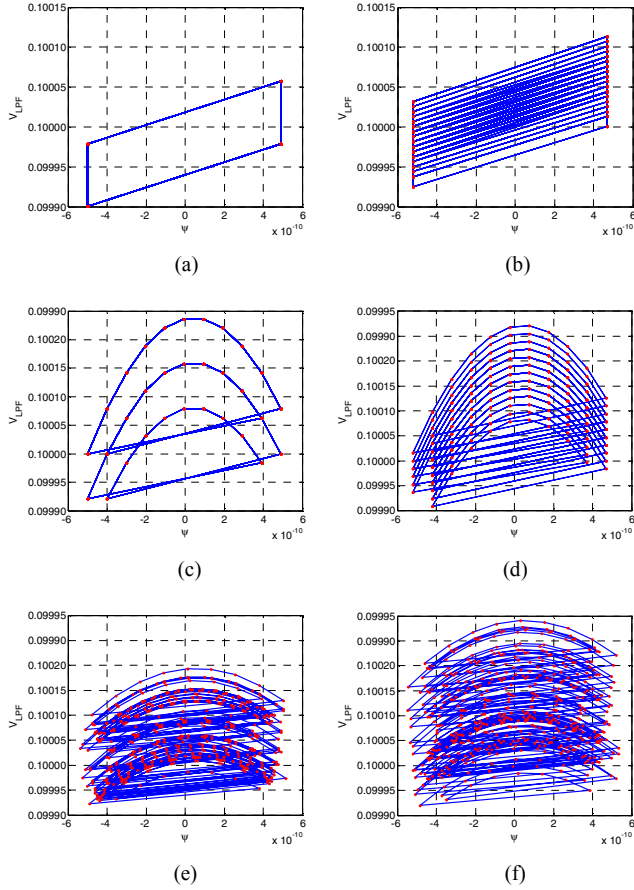


Fig. 7. Period orbits in the system modelled by (2-7) for $\zeta =$ (a, b) 10; (c, d) 10.1, (e, f) 10.12345 and all other parameters as in Fig. 4. Initial conditions are $V_{LPF}(0) = 0.16$ V, $\dot{\alpha}(0) = 0$ and $\phi(0) =$ (a, c, e) $-0.5e-09$, (b, d, f) $-0.52e-09$.

V. CONCLUSION

The investigation described in this paper provides new insight into the global dynamics of the ALL from [7], on the basis of numerical investigations. We have examined the stability region for the ALL for different parameter values. An interesting feature here is the appearance of disconnected “islands” in the stability region, which arise as a result of the aliasing action within the loop. We have also examined the steady-state dynamics of the system, highlighting in particular the effect of the ratio of the reference and sampling frequencies. Our ongoing work in this area focuses on further developing an analytical understanding of the behaviour illustrated in this paper.

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REFERENCES

- [1] R. Flynn, O. Feely, “Nonlinear dynamics of gear-shifting digital phase-locked loops,” in proceedings of the 2004 International Symposium on Circuits and Systems, pp. IV - 657-60, May 2004.
- [2] A. Podgorny, O. Feely, “Global nonlinear dynamics of second-order DPLL,” in proceedings of the 2000 International Symposium on Circuits and Systems, pp. 225 – 228, May 2000.
- [3] A. Teplinsky, E. Condon, O. Feely, “Driven interval shift dynamics in sigma-delta modulators and phase-locked loops,” *IEEE Trans. on Circuits and Systems I*, vol. 52, no. 6, pp 1224 – 1235, 2005.
- [4] F. M. Gardner, “Charge-pump phase-lock loops,” *IEEE Trans. Comm.*, 28(11):1849-1858, 1980.
- [5] P. Acco., “Why do we linearise charge pump pll equations so early?,” NDES, pp. 173-176, 2001.
- [6] A. N. Hafez and M. I. A Elmasry, “Novel low power low phase-noise PLL architecture for wireless transceivers,” in Proc. 9th Great Lakes Symp. VLSI, pp. 306 – 309, March 1999.
- [7] L. van den Berg and D. G. Elliott, “An alias-locked loop frequency synthesis architecture,” in Proc. IEEE Int. Symp. on Circuits and Systems, pp.1536 – 1539, May 2008.
- [8] A. Teplinsky, O. Feely and A. Rogers, “Phase jitter dynamics of digital phase-locked loops,” *IEEE Trans. on Circuits and Systems I*, vol. 46, no. 5, pp 545 – 559, 1999.