



<b>Title</b>	A TDD/FDD SAW-less superheterodyne receiver with blocker-resilient band-pass filter and multi-stage HR in 28nm CMOS
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<b>Publication date</b>	2015-06-19
<b>Publication information</b>	Madadi, Iman, Massoud Tohidian, Koen Cornelissens, Patrick Vandenameele, and Robert Bogdan Staszewski. "A TDD/FDD SAW-Less Superheterodyne Receiver with Blocker-Resilient Band-Pass Filter and Multi-Stage HR in 28nm CMOS." IEEE, June 19, 2015. <a href="https://doi.org/10.1109/VLSIC.2015.7231302">https://doi.org/10.1109/VLSIC.2015.7231302</a> .
<b>Conference details</b>	IEEE 2015 Symposium on VLSI Circuits (VLSI), Kyoto, Japan, 17 -19 June 2015
<b>Publisher</b>	IEEE
<b>Item record/more information</b>	<a href="http://hdl.handle.net/10197/7301">http://hdl.handle.net/10197/7301</a>
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<b>Publisher's version (DOI)</b>	10.1109/VLSIC.2015.7231302

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# A TDD/FDD SAW-Less Superheterodyne Receiver with Blocker-Resilient Band-Pass Filter and Multi-Stage HR in 28nm CMOS

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## Abstract

A SAW-less discrete-time superheterodyne receiver (RX) with multi-stage harmonic rejection in 28nm CMOS, featuring highly linear LNTA, employs a novel blocker-resilient octal charge-sharing band-pass filter to achieve low power consumption. The RX features NF of 2.1 to 2.6 dB, and IIP3 of 8 to 14 dBm, while drawing only 24 to 37 mW in different operating modes.

## Introduction

Conventional multi-band, multi-standard receivers (RXs) require many duplexers, SAW filters and switches, typically one per band. To reduce cost and size, the trend is to eliminate SAW filters and switches by using a highly linear wideband RX [1]-[4]. As a consequence, the isolation of transmitter (TX)-to-RX, and the suppression of TX interferers are worsening, which all further increase RX linearity requirements in FDD modes. The reduced out-of-band (OB) filtering implies very tough IIP2 requirement for zero-IF (ZIF) receivers, thus requiring highly sophisticated calibration algorithms to be frequently run due to PVT and channel variations. There are many other issues associated with ZIF, such as time-variant dc offsets, sensitivity to flicker noise, and large in-band LO leakage. On the other hand, superheterodyne architectures [5], [6] do not experience the aforementioned problems thanks to their high IF. Note that a high-IF RX can have a theoretically infinite IIP2 because a modulated blocker at the input will be down-converted to around dc, thus completely filtered out.

The full-rate high-IF RX in [6] operates in discrete-time (DT) using a quadrature charge-sharing (CS) band-pass filter (BPF) to realize a highly reconfigurable RX solution of small die area and high power efficiency. As in any wideband RX, the linearity and tolerance to out-of-band blockers mainly depends on its first filter's selectivity. Unfortunately, the quadrature CS-BPF has insufficient blocker rejection to support the SAW-less operation. In this work, we propose a novel CS-BPF that utilizes an octal-phase (i.e., eight 45°-separated) signaling and an extra pole to improve filtering and harmonic rejection (HR). Combined with a highly linear wideband LNTA, the first-ever high-IF SAW-less RX is thus demonstrated.

## Receiver Architecture

The proposed RX is shown in Fig. 1. The input voltage is converted to current by LNTA and down-converted to high-IF by octal DT sampling mixer. After the mixer, the sampled down-converted signal is fed to the DT octal CS-BPF to attenuate images and out-of-band blockers. To reduce its power consumption, the decimation by 2 is performed for the 1<sup>st</sup> CS-BPF by integrating two samples, thus giving rise to the anti-aliasing *sinc*-type transfer function. In addition to the intrinsic 3<sup>rd</sup>/5<sup>th</sup> HR of the CS-BPF, further harmonics rejection can be performed by turning on the additional HR block. A 2<sup>nd</sup> CS-BPF is cascaded via inverter-based  $g_m$ -cells providing flicker-noise-free gain. The sufficient front-end filtering (unlike in [6]) allows to directly digitize the IF signal using a low power ADC, and move baseband filtering into digital

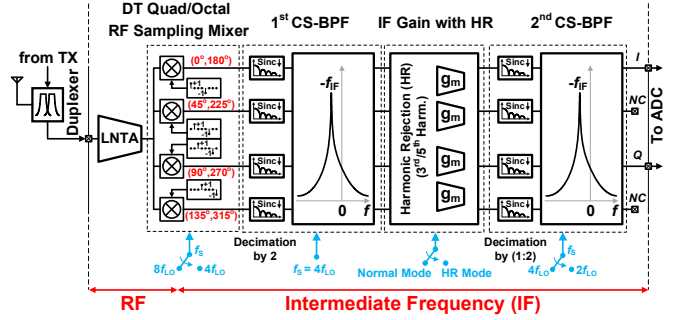
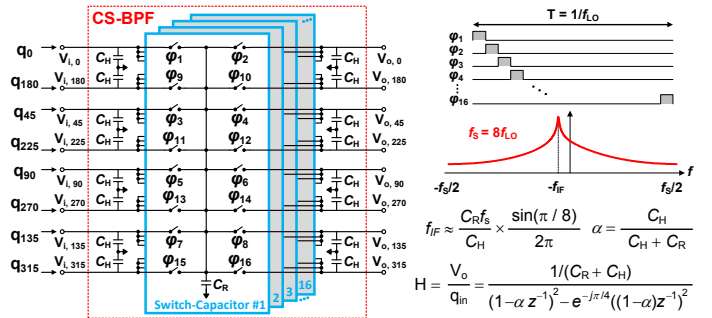


Fig. 1 Proposed SAW-less discrete-time superheterodyne receiver.



domain. As calculated, a 10b 400 MS/s ADC is enough after the two stages of CS-BPF filters, while consuming less than only 2mW with the state-of-the-art SAR ADC structure [7].

## Charge-Sharing Band-Pass Filter (CS-BPF)

The proposed blocker-resilient octal CS-BPF of Fig. 2 features a sharp and highly linear transfer function (TF) in order to filter the images and out-of-band blockers even at 3<sup>rd</sup>/5<sup>th</sup> harmonics of LO. The inputs are charge packages ( $q_0, q_{45} \dots$  and  $q_{315}$ ) with different phases provided by the DT mixer. In each phase,  $\phi_1 - \phi_{16}$ , the rotating capacitor  $C_R$  takes a charge from the *input*  $C_H$  capacitor. In the following phase,  $C_R$  is connected to the *output*  $C_H$ , and so on. As shown in Fig. 2, this technique creates a complex BPF centered at  $-f_{IF}$  due to the charge-sharing between input charges of different 45° phases cascaded by the 1<sup>st</sup>-order LPF positioned at the output without any folding and replicas within  $-f_s/2$  to  $f_s/2$ . The OB blocker filtering is improved significantly compared to [6] by increasing the number of input phases of CS-BPF and adding LPF pole between the complex poles due to the circulation of charge between the complex input charges. The center frequency of the filter is fully controllable by the ratio of  $C_R/C_H$  and sampling frequency, thus making it insensitive to PVT.

## Harmonic Rejection (HR)

The principle of the proposed HR in CS-BPF is shown in Fig. 3 ("stage-1"). Although the 1<sup>st</sup> and 3<sup>rd</sup>/5<sup>th</sup> input harmonics are down-converted to the same IF frequency by the octal mixer, their phases remain preserved. Therefore, instead of storing the harmonic information in the frequency domain, as is the case before the mixer, it is now stored in the 8 mixer output lines and will be preserved as long as the number of lines is maintained. The charge-sharing phases of the signal for the 1<sup>st</sup> (blue) and 3<sup>rd</sup> (red) harmonics are shown in Fig. 3 (top). Fig. 3 (bottom) shows the corresponding phase rotation vectors. The

phase difference between two adjacent lines for the 1<sup>st</sup> and 3<sup>rd</sup>/5<sup>th</sup> harmonics are  $\pi/4$  and  $(-3\pi/4)/(-5\pi/4)$ , respectively. This harmonic phase difference is sensed by CS-BPF. Their different transfer functions (TF) are shown in Fig. 3 (bottom). The HR is 22dB for each CS-BPF, which can be continuously improved by cascading CS-BPFs since the octal format fully preserves the harmonic information. HR is further improved by the proposed “stage-2” HR block. It consists of four  $X_1$  blocks, each having three identical  $g_m$ -cells adding three adjacent vectors, resulting in amplification of 1<sup>st</sup> harmonic vectors and partial rejection of 3<sup>rd</sup>/5<sup>th</sup> harmonics. The two proposed techniques are insensitive to mismatches and do not require any calibration, whereas other well-known approaches, such as HR-mixers or  $g_m$ -weighting, are sensitive to mismatch. Also, HR of those approaches cannot be further improved because the combined output signals are converted to I/Q (quadrature), thus aliasing the harmonic information.

### Low Noise Transconductance Amplifier

Fig. 4(a) shows the fully differential schematic of the proposed LNTA simultaneously featuring low NF and high IIP3 (only single-ended signals are shown). The noise-canceling common-gate transistors ( $M_{n1}/M_{n2}$ ) provide the RX input matching. The noise-canceling operation is as follows: the input signal gets amplified by transistors  $M_{n1}/M_{n3}$  and  $M_{p1}$  in a differential feed-forward manner, whereas the  $M_{n1}$  channel thermal noise experiences subtraction at the output nodes because of the out-of-phase correlated noise voltages at  $V_x$  and  $V_{outn}$ . The 3<sup>rd</sup>-order non-linearity of  $M_{n1}$  and  $M_{n3}$  can be simultaneously cancelled at the differential output because  $M_{n1}$  and  $M_{n3}$  operate in weak and saturation regions, respectively, resulting in out-of-phase  $g_{m3}$  (3<sup>rd</sup>-order transconductance) to each other. Therefore, partial cancellation of IM3 component happens at the differential output. The cancellation happens at the desired frequency because at other frequencies an additional IM3 is generated due to the 2<sup>nd</sup>-order non-linearity of  $M_{n3}$ . Simulated (with extracted parasitics) NF of LNTA is 1.5–1.6dB across 0.85–2.5GHz.

### Experimental Results

Fig. 7 shows the chip photo of the RX in TSMC 28nm CMOS. Measured NF is 2.1–2.6dB across 0.85–2.5GHz, as shown in Fig. 4(b), while providing 29–35dB gain. Peak IIP3 of +14dB is achieved for 2G/3G at max gain. The measured wideband TF in the normal and HR modes for three ICs is shown in Fig. 5(a). The IF image rejection of more than 65dB is achieved in all three ICs. The worst-case HR of 58dB is achieved when the HR-block is enabled: 44dB from the two-stage CS-BPFs and the rest from the HR-block. The measured normalized TF is shown in Fig. 5(b) for different bands. The RX bandwidth is 6.5MHz for 2G/3G and 20MHz for LTE, while IF frequency is -15MHz and -35MHz for 0.85–2.1GHz and 2.5GHz carriers, respectively. The RX consumes 24, 34 and 37mW from 0.9V supply at 0.85, 2.1 and 2.5GHz, respectively.

Table I compares the proposed DT-RX with state-of-the-art RXs. While being best-in-class in meeting the key performance parameters without any calibration, its power consumption and area are generally the lowest, and it does not suffer from any issues related to dc offsets, flicker noise or IM2 products since its IIP2 is infinite.

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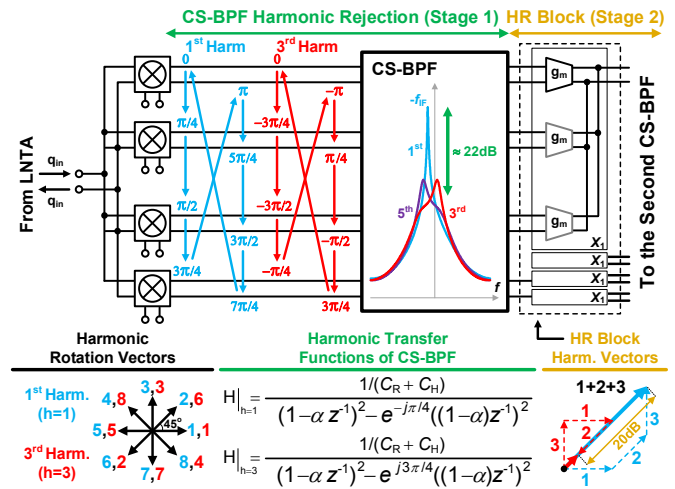


Fig. 3 Harmonic (3<sup>rd</sup>/5<sup>th</sup>) rejection in CS-BPF and HR-Block.

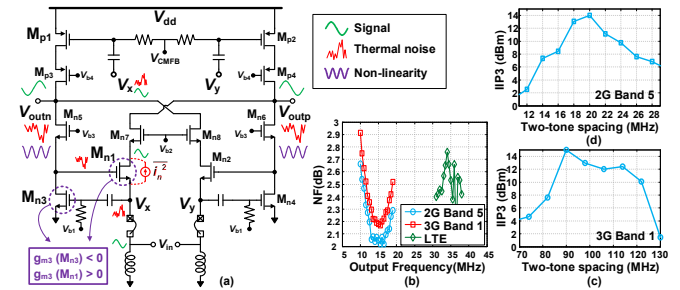


Fig. 4: (a) LNTA schematic, (b), (c) and (d) Measured RX NF, IIP3.

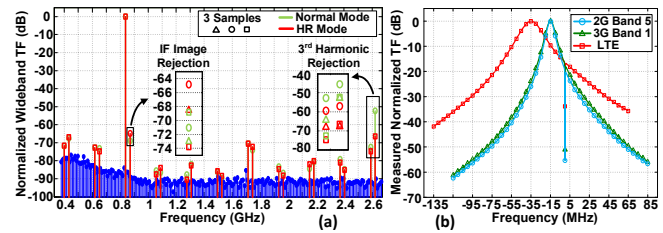


Fig. 5: Transfer function measurements of proposed SAW-less RX.

Table I Performance summary and comparison with state-of-the-art

	This Work	[5] '11 Broadcom	[6]'14 TUD	[3] '14 IMEC	[4] '14 Broadcom	[1] '13 UPavia	[2] '14 MediaTek
Technology	28nm	65nm	65nm	28nm	28nm	40nm	40nm
Architecture	High-IF	High-IF	High-IF	ZIF	ZIF	ZIF	ZIF
NF [dB]	2.1/2.2/2.6	2.8	3.2–4.5	1.8–3	1.7	3.8/1.9	1.7–2.4
Supply [V]	0.9	1.2/2.5	1.2/2	0.9	1.0	1.2/1.8	1.5
HR [dB]	>58*	N/A	N/A	50(70 <sup>s</sup> )	60/60	54/65	N/A
IIP3 [dBm]	14(OB)	-6.3(OB)	-7(1B)	8/5	11.5(OB)	18/16(OB)	0.4(OB)
IIP2 [dBm]	Infinite	N/A	85*(OB)	55(88 <sup>s</sup> )	55(OB)	64(OB)	55(OB)
Power [mW]	24/34/37	≈ 39	55–65	40/35	36–62	32/32	39–46.5
Area [mm <sup>2</sup> ]	0.52	0.76	1.1	0.6	5.2	0.84/0.74	0.57

\* Worst-case without calibration <sup>s</sup> with calibration <sup>v</sup> Due to an IF Mixer

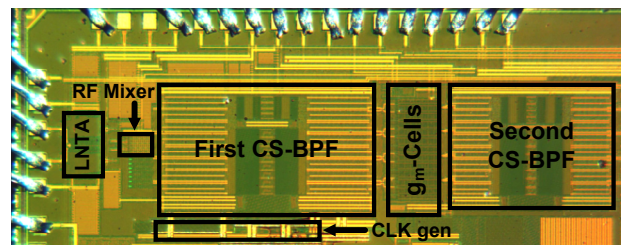


Fig. 7: Chip micrograph of the proposed SAW-less RX.