



<b>Title</b>	A digital to time converter with fully digital calibration scheme for ultra-low power ADPLL in 40 nm CMOS
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implemented based on a pseudo-differential structure. Compared to DTC-only bang-bang phase detector, the combination of DTC and TDC offers fast settling and better phase noise performance.

### III. DIGITAL TO TIME CONVERTER

The dynamic range of a DTC is designed to cover the whole period of  $CKV/2$  over process, voltage and temperature (PVT) variations and the resolution of it is determined by the requirement of ADPLL's in-band phase noise. Hence, a 6-bit DTC is designed. The system diagram of the DTC is depicted in Fig. 2 (a), where the core DTC is composed of 64 delay stages; FREF clock is fed to all stages via clock feeders (CF) and is gated by the decoder output bits  $EK_{0-63}$ , while the signals  $EB_{0-63}$  are applied to enable the delay elements (DE). The delay control bits determine the effective delay of the rising edge of FREF from its input to the DTC output,  $FREF_{DLY}$ . Inside each delay stage (Fig. 2 (a)), two switches (controlled by  $EK_i$  and  $EB_i$ ) decide whether this stage will be a clock feed-in point of FREF or it will be connected to the previous stage. For example, in Fig.2 (b), when the  $i^{th}$  stage is chosen as the feed-in point, the succeeding stages' CFs will be bypassed and only the unit delays (DE) are counted, so the effect delay of DTC equals to the sum of the identical offset ( $\Delta offset$ ) by CF and the total delay of the succeeding stage delay elements and the delay element of the feed-in point.

Fig. 2(a) also shows the schematic of one DTC stage. The tri-state MOS complementary pair of  $P_c$  and  $N_c$  [4] is employed as CF to either pass the signal from the preceding stage

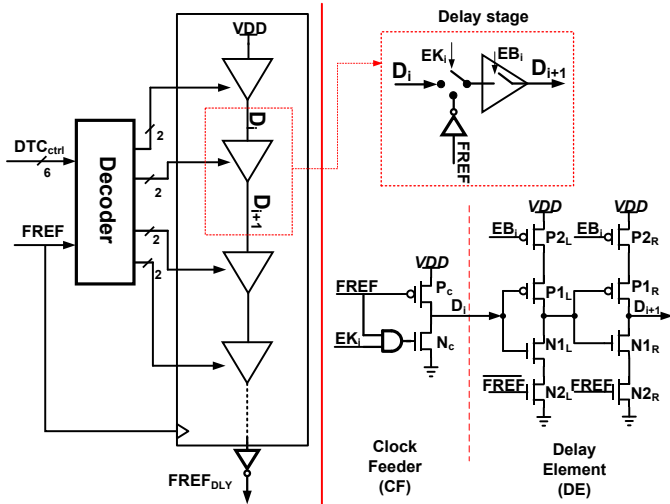


Fig. 2(a). Simplified schematic of the DTC: transistors ( $P_{2L}$ ,  $P_{1L}$ ,  $N_{1L}$ ,  $N_{2L}$ ,  $P_{2R}$ ,  $P_{1R}$ ,  $N_{1R}$ ,  $N_{2R}$ ) compose the delay element (DE), and  $P_c$ ,  $N_c$  are for the clock feeder (CF).

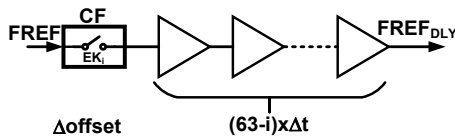


Fig.2 (b). Principle of DTC (when the  $i^{th}$  stage is chosen as the starting point delay chain,  $i=0 \dots 63$ ).

( $EK_i=0$ ), or to feed in the FREF clock ( $EK_i=1$ ).  $P_c$  is on when FREF is low as a preset state, while  $N_c$  serves as a pull-down switch when  $EK_i$  and FREF are both high. For the delay elements, two cascaded inverters are utilized and gated so that they are switched off if they are not active on the propagation path. Doing so reduces unnecessary power loss.

### IV. DIGITAL CALIBRATION ALGORITHM

The DTC control bits ( $DTC_{ctrl}$ ) are calculated based on the conversion gain of DTC ( $K_{DTC}$ ) and the fractional part ( $PHR_F$ ) of the accumulated FCW (see Fig.3-(a)), and their relationship is illustrated in (1), where  $K_{DTC}$  is the ratio of the resolution ( $\Delta t$ ) of the DTC to the time period of  $CKV/2$ . The quantization residue of the DTC is removed from the TDC result and has no impact on phase noise of ADPLL but the resolution of the DTC is sensitive to PVT variations, and the inaccurate  $K_{DTC}$  makes the predicted reference phase ( $FREF_{DLY}$ ) either lag or lead the ideal predicted case, and the deviation of phase error (PHE) is termed as PE. Hence, the least-mean-squared (LMS) calibration based on phase error [3] is applied, as shown in Fig.3 (a). Assumption here is made that the calibration scheme works at the steady state of a type-II PLL, features a statistic zero-mean PHE between the variable oscillator signal ( $CKV$ ) and a reference signal (FREF). Any deviation caused by the  $1/K_{DTC}$  error is observed via PHE or the fractional part (PHF) of PHE.

Equation (3) indicates that finding the minimum mean-square error is to find the correlation between  $e$  and the variable value  $PHR_F$ , and this is implemented in Fig.3 (a) and (b). The background calibration is to adaptively estimate the variation of the reciprocal of the DTC conversion gain,  $1/K_{DTC}$ , and to minimize the error  $e$  (in (2)) related to the fractional phase error detection, in the way that the error  $e$  correlated to PHE by inaccurate  $1/K_{DTC}$  is minimum when the derivative of the mean-squared error  $E(e^2)$  to  $1/K_{DTC}$  is zero. The diagram of  $1/K_{DTC}$  calibration is depicted in Fig. 3 (b), comprising of an estimating error block, an IIR filter and an accumulator. The predicted phase by the DTC conversion gain is a saw-tooth waveform, whose slope is sharper than that of the ideal phase if DTC conversion gain is underestimated and vice versa when overestimated. Furthermore in order to simply the hardware implementation, the sign of  $e$  is utilized instead of  $e$  itself, as well as the sign of fractional vale ( $PHR_F$ ) of PHE. The IIR filter is good for fast convergence and the accumulator is for the correlation function.

This algorithm is fully arithmetic and verified in RTL level together with the whole system of an implemented ADPLL, as depicted in Fig. 3(c). The multiplier ( $1/K_{DTC}$ ) is thus calibrated and it converges to the desired value, and PHF is taken to

$$DTC_{ctrl} = \frac{1 - PHR_F}{K_{DTC}} \quad (1)$$

$$e = \frac{PE}{\Delta t} \times \left( \frac{1}{1 - PHR_F} \right) \quad (2)$$

$$\frac{\partial E(e^2)}{\partial (1/K_{DTC})} = 2E(e \times (1 - PHR_F)) = 0 \quad (3)$$

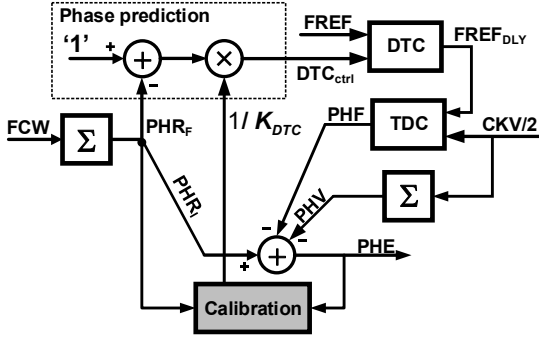


Fig. 3(a). DTC and TDC with phase error detection as part of the DTC conversion gain ( $K_{DTC}$ ) calibration loop.

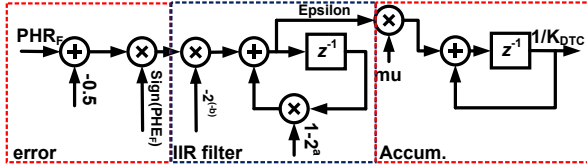


Fig. 3(b). The diagram of  $K_{DTC}$  calibration algorithm.

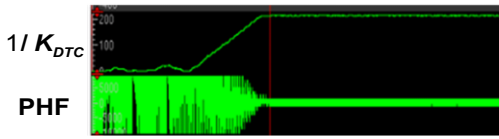


Fig.3(c). RTL code verification of the DTC gain calibration.

monitor the calibration, which is consequently minimized, indicating the locked-loop at the same time.

## V. EXPERIMENTAL VERIFICATION.

The DTC and TDC circuits have been fabricated in a 40 nm CMOS process, together with remaining components for an ultra-low power ADPLL. Thanks to custom layout of the DTC and the TDC, parasitic capacitors are minimized to decrease their impact on the time performance. Also the compact layout helps to reduce the power consumption and mismatch. The die-photo of the chip is shown in Fig. 4, where DTC+TDC occupy a chip area of  $0.0034 \text{ mm}^2$ .

The measured results of the DTC reveal a time resolution of 22.3 ps, the peak DNL is 2.2 LSB and the peak INL is 1.7 LSB, all without calibration (see Fig. 5). Relatively high DTC non-linearity is contributed by the small device geometry for minimizing power consumption. The TDC resolution can be estimated by the in-band closed-loop phase noise floor in a locked state. To avoid any non-ideal effects of the DTC and to

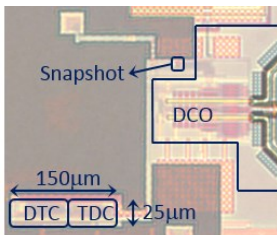


Fig. 4. Chip die photo of DTC, TDC and snapshot circuit.

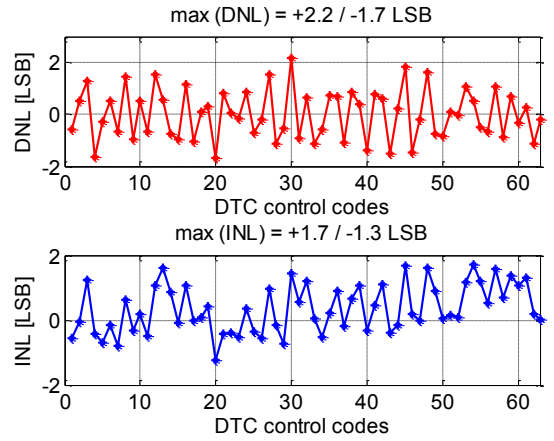


Fig. 5. Measured linearity performance of the DTC without calibration.

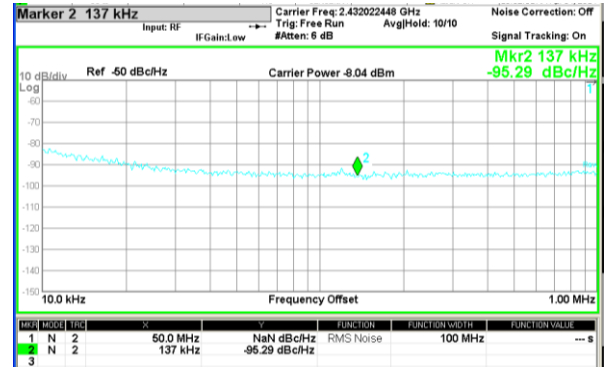


Fig. 6. Zoom-in phase noise of the ADPLL.

suppress the noise contribution from the DCO, the phase noise at an integer channel is measured and the loop bandwidth is maximized to wider than 1 MHz. In Fig. 6, a measured in-band phase noise of  $-95.3 \text{ dBc/Hz}$  corresponds to a worst case TDC resolution of 22 ps.

The post-layout simulation of DTC is shown in Fig. 7. The peak point of both DNL and INL curves are due to the different metal path of the middle two stages in the layout. Compared to the simulation results, the time resolution (27 ps) of DTC is the

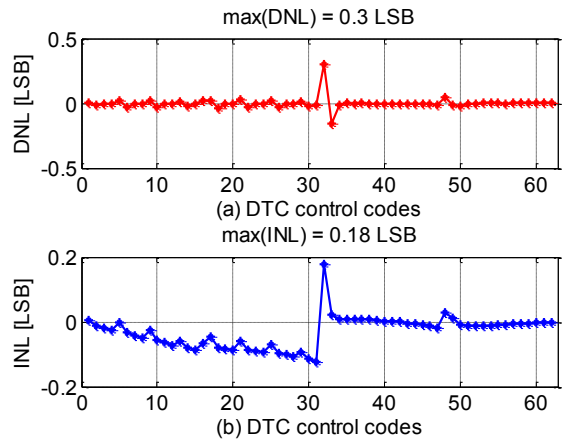


Fig. 7. Simulated linearity performance of the DTC.

TABLE I. PERFORMANCE COMPARISON

	This Work	[5]	[6]	[1]	[7]
Structure	DTC+TDC	DTC+Bang bang PD	Two-step	Cyclic	1st order $\Sigma\Delta$
Tech.	40 nm	65 nm	65 nm	65 nm	32 nm
Supply	1.0 V	1.1 V	1.2 V	1.25 V	1.0 V
Ref. Freq.	32 MHz	48 MHz	200 MHz	NA	10 MS/s
DCO Freq.	1.2 GHz	5.3 GHz	200 MS/s	2.4GHz	10 MS/s
Power	43 $\mu$ W	220 $\mu$ W (DTC only)	3.6 mW	120 $\mu$ W	250 $\mu$ W
Range	1.6 ns	190 ps	960 ps	N/A	N/A
Resolution	22 ps	4.7 ps	3.75 ps	N/A	4.4 ps
FoM	0.49 fJ	1.03 fJ	70.3 fJ	N/A	N/A
$FoM = \frac{\text{power} \cdot \text{resolution}}{\text{InputFreq} \cdot \text{Range}}$					

same but the measured linearity of DTC is degraded.

The measured complete power of DTC+TDC is 43  $\mu$ W. Post-layout simulations help estimate that 1/3 of the power consumption is from the DTC, and 2/3 from the TDC. Table I provides the performance comparison with state-of-the-art TDCs for low energy radios. A TDC FoM is defined in Table I. Thanks to the assistance of the DTC and snapshotting technique [2], this work achieves the lowest dissipated power while maintaining the required TDC dynamic range, leading to a state-of-the-art FOM of 0.49 fJ.

## VI. CONCLUSION

An ultra-low power DTC with fully digital calibration has been proposed and demonstrated in 40 nm CMOS. The use of phase-prediction and DTC assistance is verified to reduce the required dynamic range and power consumption of the TDC. The calibration of DTC conversion gain is discussed and verified. The designed DTC-assisted TDC was also integrated with an ADPLL and overall system results have been demonstrated to validate the system performance of the DTC/TDC pair.

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