Hindawi Publishing Corporation
EURASIP Journal on Wireless Communications and Networking
Volume 2006, Article ID 71249, Pages 1–8
DOI 10.1155/WCN/2006/71249

A Sigma-Delta ADC with Decimation and Gain Control Function for a Bluetooth Receiver in 130 nm Digital CMOS

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Received 25 October 2005; Revised 15 April 2006; Accepted 18 April 2006

We present a discrete-time second-order multibit sigma-delta ADC that filters and decimates by two the input data samples. At the same time it provides gain control function in its input sampling stage. A 4-tap FIR switched capacitor (SC) architecture was chosen for antialiasing filtering. The decimation-by-two function is realized using divided-by-two clock signals in the antialiasing filter. Antialiasing, gain control, and sampling functions are merged in the sampling network using SC techniques. This compact architecture allows operating the preceding blocks at twice the ADC's clock frequency, thus improving the noise performance of the wireless receiver channel and relaxing settling requirements of the analog building blocks. The presented approach has been validated and incorporated in a commercial single-chip Bluetooth radio realized in a 1.5 V 130 nm digital CMOS process. The measured antialiasing filtering shows better than 75 dB suppression at the folding frequency band edge. A 67 dB dynamic range was measured with a sampling frequency of 37.5 MHz.

1. INTRODUCTION

Discrete-time analog signal processing approaches for Bluetooth wireless receivers have been proposed and successfully implemented [1, 2]. These receivers employ a discrete-time architecture in which the RF signal is directly sampled and filtered using analog and digital signal processing techniques. Although sampling close to the front-end may render the receiver architecture more susceptible to noise folding and clock jitter effects, it also provides significant advantages that make this technique very attractive.

From the RF wireless system point of view, integrating analog building blocks and digital baseband circuits on the same chip helps to reduce area and power consumption, thus driving down the total system cost. Advanced digital CMOS technology provides very high-speed switching devices, thus allowing discrete-time circuits to be clocked at very high rates. Additionally, it is well known that these digital CMOS processes show component matching as good as or even better than traditional analog processes, even though absolute component value may present big spread over process corners.

The approach shown in Figure 1 [1, 2] takes advantage of this system and CMOS process characteristics by directly sampling the RF signal after the LNA and subsequent processing that exploits the precise capacitance ratios that set the filtering coefficients. Total noise due to folding can be minimized by sampling at a very high rate compared to the input signal bandwidth. This is achieved in the direct sampling mixer (DSM) which samples the RF signal at RF carrier rate, while down-converting and integrating it in a sampling capacitor. In order to realize the direct sampling, the DSM clocking frequency must be kept high at RF, while, at the same time, the ADC data rate should be kept low in order to reduce power dissipation and to allow for sufficient settling time to the input signal. Thus, an ADC that provides data rate conversion and signal amplification in the input sampling stage becomes very advantageous. Figure 2 represents a basic idea for this approach.

In this paper, we present such an approach, which has been implemented and verified in a 130 nm digital CMOS process. The organization of this paper is as follows. Section 2 presents the receiver architecture. The sigma-delta ADC design and the proposed built-in antialiasing filter merged into sampling network are described in Section 3. Measurements and implementation are presented in Section 4. Performance summary and conclusions are covered in Section 5.

2. RECEIVER ARCHITECTURE

The amount of interferer filtering performed in the front-end establishes the ADC dynamic range (DR) specification

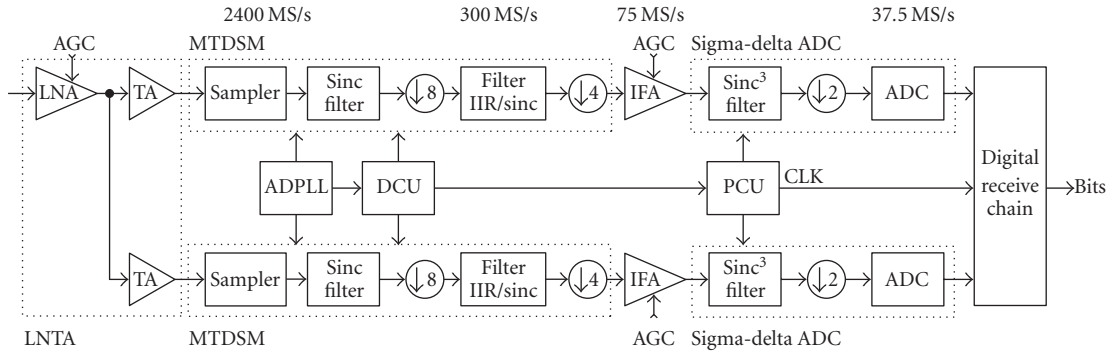


Figure 1: A discrete-time RF wireless receiver [1, 2].

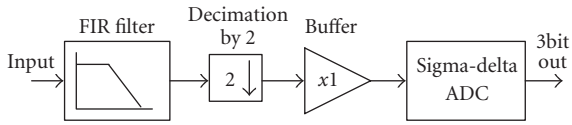


Figure 2: Typical building blocks for what would be required for decimation and gain control.

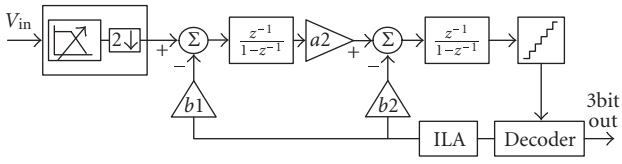


Figure 3: Proposed sigma-delta ADC architecture.

to a minimum of 60 dB. In [3, 4], it was shown that a 5-level second-order sigma-delta ADC can achieve this DR at a $F_s = 37.5$ MHz sampling frequency while maintaining a low power dissipation. The block diagram in Figure 3 shows the 3-bit sigma-delta architecture with the built-in antialiasing filter. This multibit architecture relaxes the first integrator's amplifier requirements, thanks to the reduced signal changes at the amplifier's output when compared to a single-bit sigma-delta ADC. Also, the required full signal swing at this node is reduced, resulting in a relaxed settling time and slew rate specifications. This also results in area and power savings, since a single-stage low-voltage and low-power amplifier can be used for the implementation.

Two issues need to be carefully considered for the ADC system design. First, since decimation causes noise folding, an antialiasing filter is required. This filter is implemented using an FIR switched capacitor structure. Second, from the Bluetooth system requirements, there is a need for an automatic gain control (AGC) function. Providing some gain control at the input of the ADC helps distributing the AGC function between the ADC and the intermediate frequency amplifier (IFA), thus relaxing the IFA specification and optimizing power consumption.

A hypothetical conventional solution, as shown in Figure 2 would require an isolation buffer between the FIR filter and the ADC input sampling stage in order to avoid charge sharing between the two switched capacitor blocks. This buffer would also provide the required AGC functionality. However, this amplifying stage would have very demanding settling time requirements to reduce the error at the sampling instant in the ADC input stage. In addition, it would increase area and power consumption.

The FIR filtering, decimation-by-two, and gain control functions are all implemented in the sampling network at the input of the ADC. As shown in Figure 3, combining these functions in a single sampling structure optimizes area, power, and complexity.

3. SIGMA-DELTA ADC DESIGN

3.1. FIR antialiasing filter and decimation

The diagram in Figure 4 shows a switched capacitor implementation of the sampling network, but, for the sake of clarity at this point, it does not include the gain control function. Since the supply voltage is 1.58 V, that is, above 1.4 V of the nominal supply to ensure good transconductance, all switches are realized as regular NMOS devices with nominal $V_T = 600$ mV. The key role of the FIR filter is to provide enough noise suppression around $F_s/2$. The signal at the input of the ADC is naturally band-limited to 75 MHz by the preceding circuits. The ADC works at half that frequency. A 4-tap charge-domain FIR filter is implemented to attenuate the input signal noise around 37.5 MHz. The FIR order was determined by system level simulations. The FIR filter difference equation is given by

$$C_M \cdot y[n] = C_0 \cdot x[n] + C_1 \cdot x[n-1] + C_2 \cdot x[n-2] + C_3 \cdot x[n-3], \quad (1)$$

where coefficients C_0, C_1, C_2, and C_3 are 1, 3, 3, and 1, respectively, which can be easily implemented as capacitor ratios.

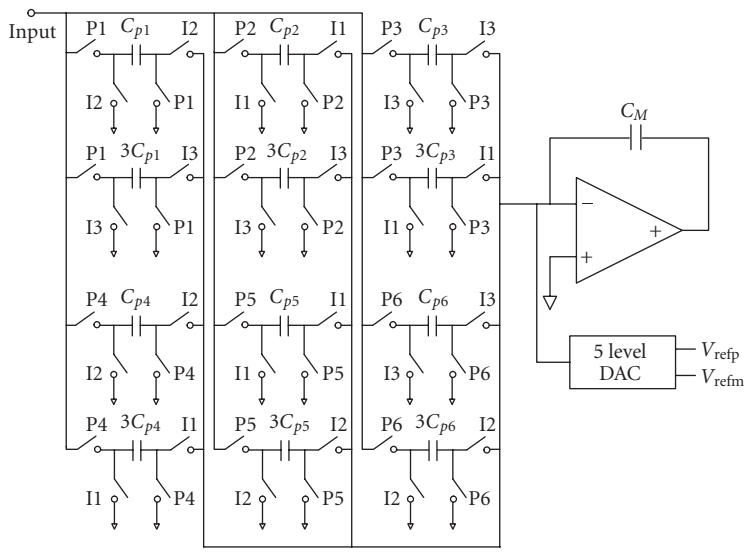


Figure 4: Four-tap FIR filter implementation.

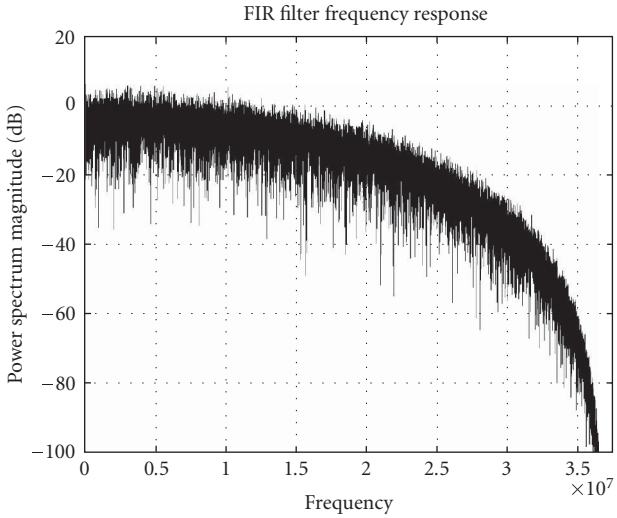


Figure 5: Output power spectrum density for FIR filter with white noise input.

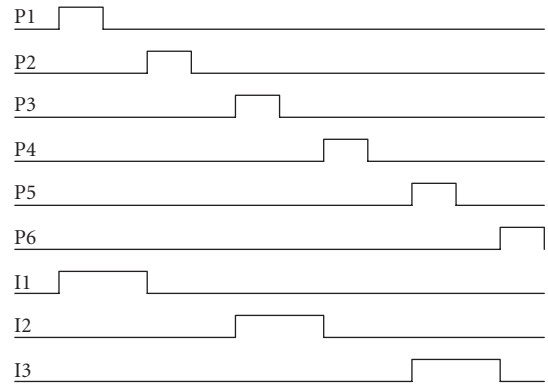


Figure 6: Control signals for the FIR filter.

The plot in Figure 5 shows the FIR output power spectral density with white noise applied as input. Matlab simulations indicate that more than 80 dB attenuations can be achieved at the folding frequency band edge (36.5 MHz, since 1 MHz is the signal bandwidth).

Capacitor mismatches in the FIR filter can possibly cause distortion and unwanted modulation. In order to reduce this effect, dynamic element matching techniques can be employed with additional switched capacitor circuits. However, these extra circuits increase area. Another way to minimize this effect is to use bigger unit capacitance which has generally better matching. Thanks to the good matching property of the CMOS process, 10 bit matching can be easily achieved without dramatically increasing unit capacitance. Based on behavioral-level simulations, the minimum allowable capacitance value was chosen. Six-phase clock signals are utilized to realize both the FIR filter and the decimation functions. On P1 phase, the input signal is sampled in C_{p2} and $3C_{p1}$, on P2 phase, it is sampled in C_{p2}, and $3C_{p2}$, and on Pi phase, the input is sampled into C_{pi} and $3C_{pi}$, with $i = 1, \ldots, 6$. After P6, the process is repeated back from P1 phase. On I1 integrating phase, charge in capacitors C_{p2}, $3C_{p3}$, $3C_{p4}$, and C_{p5} is dumped into the integrating capacitor C_M. As shown in the timing diagram in Figure 6, integration occurs in P1, P3, and P5 phases only (with corresponding signal names I1, I2, and I3). Since there could be no integration for P2, P4, or P6 phases, decimation-by-2 operation is achieved. To increase the time available for integrator settling, integrating control signals' I1, I2, and I3 duty cycle is extended as shown in Figure 6.

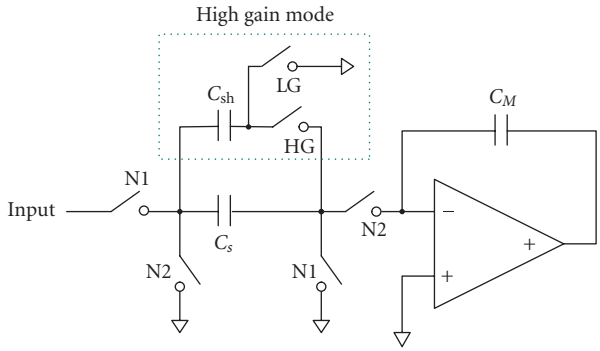
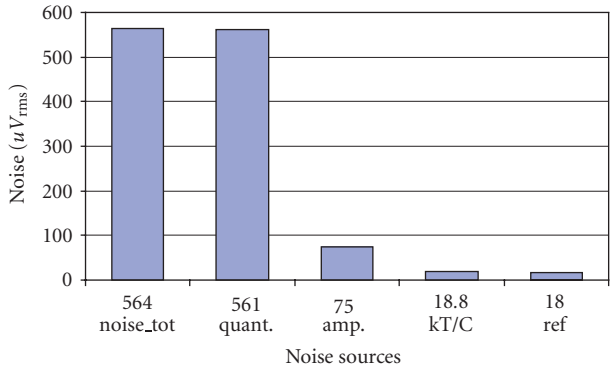


Figure 7: Gain control in the FIR filter.



Conditions:
1. Fs = 37.5 MHz
2. BW = 1 MHz
3. 5 level flash

Figure 8: Noise analysis.

3.2. Gain control

Figure 7 shows how the two-step (0 dB and 14 dB, derived from the Bluetooth RX system specifications) gain control function is implemented using switched capacitor circuits. When the switch HG turns on, the 14 dB gain mode is activated. When the 0 dB mode is activated, switch LG turns on instead of switch HG. The total gain is simply defined by the ratio between the sampling and the integrating capacitors. This function is implemented in the FIR sampling block by adding the high-gain-mode switched capacitor in parallel with each of the capacitors in Figure 4. An alternative of adding the capacitance in the amplifier feedback is not the best choice since it would change the amplifier gain-bandwidth (GBW) product. The load capacitance at the IFA output is an important design parameter, since it affects the GBW product as well as the slew rate of the amplifier. Therefore, both gain modes should provide the same load condition to the IFA output. As shown in Figure 7, the capacitance seen at the input port is kept constant for both gain modes. In order to minimize the sampling error due to charge injection and clock feed-through from the switches, transistor sizes are optimized for speed and area. Figure 8 shows the noise analysis for the proposed ADC. Quantization noise is a dominant noise contributor for this application due to the low oversampling ratio (OSR), making kT/C noise less of an issue. Therefore, the unit capacitance element in the FIR filter is selected based mainly on the effect of mismatch on the ADC performance.

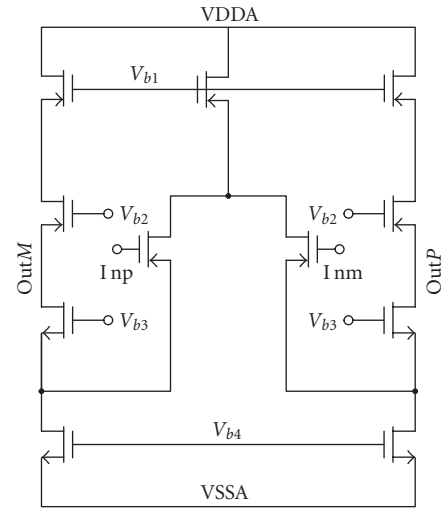


Figure 9: Folded cascode amplifier.

3.3. Amplifier, comparator, and DAC

A folded cascode fully differential amplifier with a switched capacitor common mode feedback is used [5]. Amplifier noise is optimized on the basis of power consumption and area. However, as in the case of kT/C noise, noise from the amplifier is not very critical due to the high in-band quantization noise. Therefore slew rate, GBW, and output dynamic range became the most critical design parameters. Since the sigma-delta ADC has to work in the same substrate as the digital core, digital circuit noise coupling through the substrate and supply rails was carefully considered as an important design and layout parameter. Layout considerations are also very critical, since any component mismatch could result in degradation of common-mode noise rejection and cancellation. Also, great care was taken to provide enough guard ringing and supply decoupling. The final amplifier configuration is shown in Figure 9, which does not include the common mode feedback or the bias circuits.

A five-level quantizer is implemented using four comparators to build a flash ADC. The flash ADC utilizes switched capacitor subtraction in order to generate four different threshold voltages. The simplified comparator circuits for one of the flash's four stages, including subtraction circuits, are depicted in Figure 10.

The 5-level $(+2, +1, 0, -1, -2)$ DAC is implemented using four switched capacitor elements that keep constant the capacitor loading at the input of the amplifier, independently

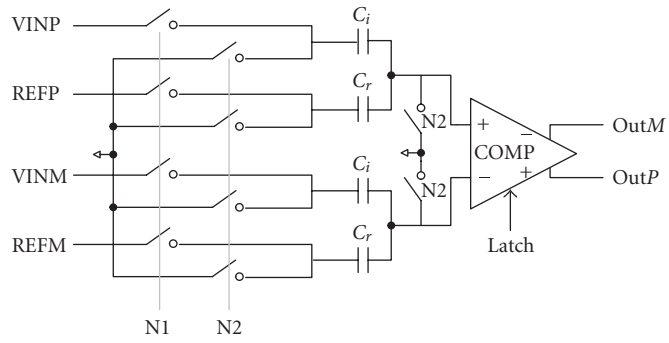


Figure 10: Switched capacitor comparator.

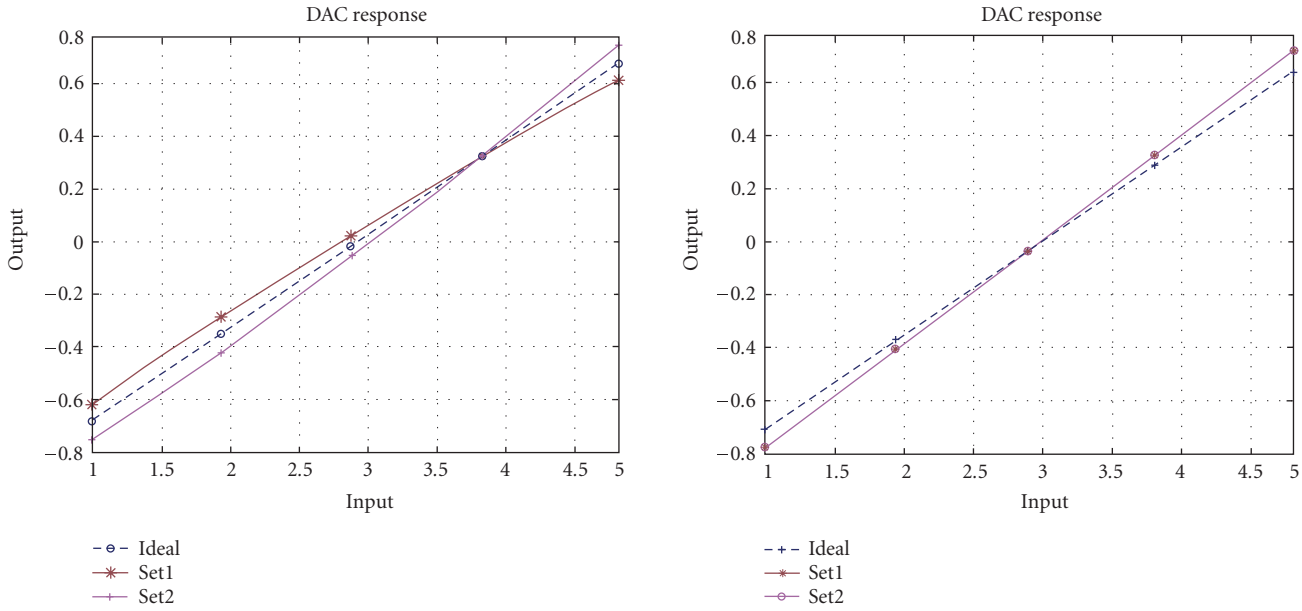


Figure 11: Transfer functions.

of the quantizer output. Two DAC elements could have been used for a 5-level DAC realization, but the load capacitance would be different for the case when quantizer output is +1 or −1 versus the case when it is +2, 0, and −2. In order to suppress nonlinearities generated in the 5-level switched capacitor DAC, the individual level averaging (ILA) algorithm is used [3, 6]. Any possible distortion from the capacitor mismatch in the 5-level DAC is translated into gain error by the ILA algorithm. This phenomenon is depicted in Figure 11. Two worst-case mismatch conditions were chosen and verified in behavioral and SPICE simulations. Figure 11(a) shows the 5-level DAC transfer function by using two worst-case mismatch conditions. Figure 11(b) shows a DAC transfer function when ILA is used to liberalize the DAC transfer function. In order to visualize the effect from capacitor mismatch clearly, unrealistic matching numbers were used to generate the plot in Figure 11.

4. EXPERIMENTAL RESULTS

The 3-bit sigma-delta ADC output was captured using a high-frequency DSP-based data acquisition system. The dynamic performance was obtained by post-processing the captured data through an FFT and computing various performance numbers. Figure 12 is the measured FIR filter response with a −6 dBFS input sinusoidal signal applied to the ADC at frequency steps of 1 MHz from 1 MHz to 30 MHz. The measurement results are well matched to the theoretical curve of the FIR antialiasing filter, as can be seen in the plot. The gain of the filter response is slightly less than the theoretical number due to the gain error induced from nonidealities in the integrator, reference buffer, and SC DAC. The power spectral density plot in Figure 13 shows the system performance when two signals (0 dB at 37 MHz and −6 dB at 275 kHz) are applied together. By sampling theory,

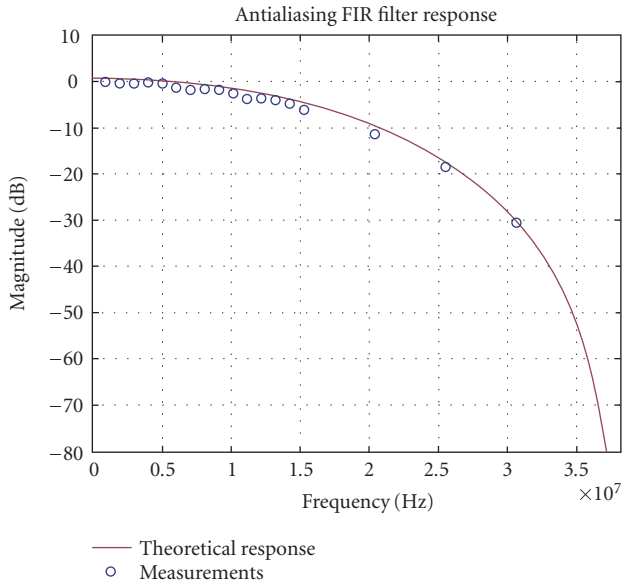


Figure 12: Measured transfer function.

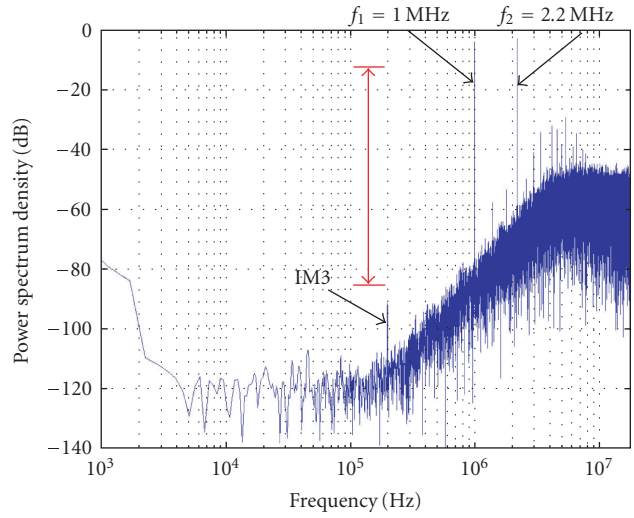


Figure 14: Two-tone test measurement.

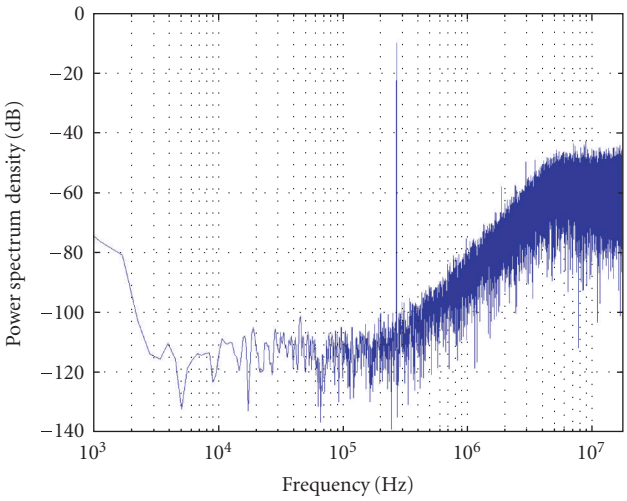


Figure 13: Spectrum of the captured output.

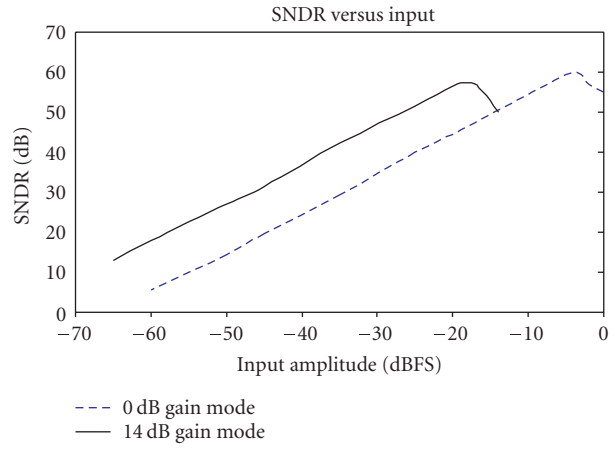


Figure 15: Measured SNDR versus input power.

this should cause a folding signal at 500 kHz (37.5 MHz (F_s) −37 MHz), but as the figure shows, it is filtered and attenuated below the quantization noise floor.

The interferers in communication systems need to be carefully taken into account especially in cases where system nonlinearities may create intermodulation. Due to ADC nonlinearities, an interferer can be folded into the Bluetooth signal bandwidth by means of intermodulation. Figure 14 shows the measured FFT plot for an intermodulation test. Two −8 dBFS sinusoidal signals at 1 MHz (F_1) and 2.2 MHz (F_2) are applied. A −80 dBc IM3 signal appears at 200 kHz. The measured IM3 satisfies and exceeds the system requirements. Figure 15 shows the measured SNDR versus input amplitude for 0 dB and 14 dB gain modes. The measured peak SNDR is 60 dB for an input 4 dB from full scale with a 1 MHz bandwidth, where the full scale is defined as twice the reference voltage. Table 1 shows the performance summary of the implemented ADC. Die photo for the dual channel implementation is shown in Figure 16.

5. CONCLUSION

A discrete-time second-order 5-level sigma-delta ADC has been successfully implemented and characterized in a 1.5 V 130 nm digital CMOS technology. The built-in antialiasing filter and a two-step gain control are merged into the sampling network. The decimation-by-two function relaxes the settling requirements of the amplifier. The two-step gain control increases the overall dynamic range and also relaxes the automatic gain control burden in the Bluetooth system

Table 1: Performance summary.

Technology	130 nm digital CMOS
Sampling frequency	37.5 MHz
Signal bandwidth	1 MHz
Peak SNDR (0 dB gain option)	60 dB
Peak SNDR (14 dB gain option)	57 dB
Dynamic range	67 dB
Overall dynamic range	77 dB
Input range	1.4 V_{pp} (diff)
Supply voltage	1.58 V
Power consumption	1.6 mW
Core area	0.2 mm^2

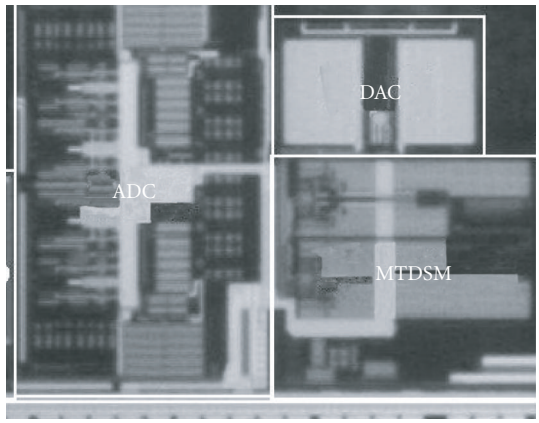


Figure 16: Micrograph of the dual channel ADC.

implementation. Since the quantization noise is the dominant factor due to the low oversampling ratio and the kT/C noise and amplifier noise are not critical, the power consumption in the ADC system was optimized, which resulted in saving area and current consumption. The total area including the switched capacitor sampling network is 0.2 mm^2 per ADC channel. The consumed power is 1.6 mW per channel at a 1.58 V supply. The achieved dynamic performance fully satisfies the system requirements for a Bluetooth receiver. The presented architecture can be easily extended to higher decimation ratios and better gain control resolution, while the FIR filter can be easily adjusted for different modes or system requirements.

ACKNOWLEDGMENTS

The authors would like to thank B. Bakkaloglu for discussion and comments and to W. E. Kim and H. S. Kim for support in device testing and characterization.

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