Oscillator-based ADCs: An Exploration of Time-Mode Analog-to-Digital Conversion

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***Abstract*—This paper presents two novel ideas within the field of time-mode oscillator-based analog-to-digital conversion. In the form of a self-injection-locked ring-oscillator (SILRO), a method is presented to inherently linearise the voltage-to-frequency (V-F) characteristic, while an alternative proposal of an ultra-low-power (ULP), ultra-low-voltage (ULV) VCO-based analog-to-digital converter (ADC) operating in weak-inversion at a supply of 0.2 V is suitable for high power efficiency, direct energy harvesting applications. The ideas are distinctly separate in concept and physical implementation, but through the common platform of Verilog-A behavioural modelling, a unified methodology applicable to both architectures is proposed for system level exploration and performance evaluation.**

Keywords*—*Analog-to-digital converter (ADC), Voltage-controlled-oscillator (VCO), Time-domain ADC, Ultra-low-voltage, Ultra-low-power, Internet-of-Things, Verilog-A behavioural modelling.

I. Introduction

CMOS technology feature scaling typified by Moore′s Law has allowed digital circuits to carry out increasingly complex operations at faster speeds while incurring low power, area and manufacturing costs. The functionality of analog integrated circuits (ICs) on the other hand, face major design obstacles due to voltage headroom reduction, low transistor intrinsic gain and matching. With the dawn of the 'Internet-of-Things' (IoT), the need to integrate analog components such as ADCs into mixed-signal system-on-chips (SoCs) to provide continuous sensing with high power efficiency presents an even more significant challenge. In the relatively new paradigm of time domain signal processing, most of the issues faced by voltage-domain ADCs in nano-scale CMOS processes are overcome. Indeed, resolution and sampling rate of the ADC actually improve with technology scaling given the steeper digital edges and higher transit frequency.

This paper introduces an ultra-low power, ultra-low voltage oscillator-based ADC operating off a supply voltage of 0.2 V. Low power and voltage operation shapes this topology as a potential leading candidate for analog-to-digital conversion in stringent power constraints application space of biomedical and IoT devices.

The highly non-linear V-F characteristic of the voltage-controlled-oscillator however, has prevented this ADC architecture from truly diffusing into the mainstream environment. As a consequence, the central efforts of the research community have been to linearise the VCO at system and circuit level. To that end, this paper offers the possibility of inherently linearising the oscillator at circuit level by leveraging on the RF principle of injection locking [1].

This paper is organised as follows: Section II briefly describes the fundamental operation of an oscillator-based ADC, key issues and synthesis of state-of-the-art implementations. Section III presents the proposed time-mode ADC architectures, while Section IV provides the circuit level investigation and implementation of the critical VCO block. Section V and VI describes behavioural modelling using Verilog-A as a common tool for system exploration and development with top level simulation results and expected performance specifications, followed by the conclusion in Section VII.

II. Prior Art

A. Oscillator-based ADC Basics

Oscillator-based ADCs convert the analog signal into its frequency domain representation using a ring-VCO, which acts as a continuous time voltage-to-phase integrator, with instantaneous phase:

$$\phi_{out}(t) = \int_0^t K_{VCO} V_{in}(\tau) d\tau \tag{1}$$

where K_{VCO} is the VCO gain (Hz/V), and $V_{in}(\tau)$ is the continuous time input voltage (V).

The multi-phase output is then sampled and differentiated in the digital domain using a frequency-to-digital converter (FDC) or a time-to-digital converter (TDC). A simple implementation uses digital counters to count the number of rising and falling edges within a sampling period to obtain the digital representation of the instantaneous frequency. The differentiation operation brings with it the interesting ability of inherent first order noise shaping which makes them, indeed continuous-time $\Delta\Sigma$ modulators. For this reason, the VCO-based ADC is almost exclusively used in oversampled applications.

B. State of Innovation

This section gives a brief chronological description of a variety of techniques that have been proposed in recent years to overcome the VCO-based ADC limitations, highlighting its architectural evolution over time.

The first proposed technique places the VCO-Quantizer within a $\Delta\Sigma$ loop [2]. The high gain of the loop filter acts to suppress the non-linearity and noise, although it does not represent a scaling-friendly approach, results in significant power consumption and necessitates careful design to ensure stability. The authors propose a novel high-speed, power and area efficient FDC to provide dynamic element matching (DEM) for the feedback digital-to-analog converter (DAC),

but constrains the clock frequency to be at least twice the maximum VCO frequency.

In [3], phase is used as the feedback variable in the $\Delta\Sigma$ loop to relax the requirement on the loop filter. Indeed, the VCO acts here as the loop integrator and, as a result, an even smaller range of its tuning characteristics is exercised, thus improving linearity considerably. The intrinsic DEM property however is lost and must be substituted with an external dynamic weighted averaging (DWA) circuit, avoided in [4] by utilising intrinsic clocked averaging (CLA).

The following wave of innovation presents more digitally intensive approaches to linearise the VCO in open loop via digital background calibration [5],[6]. The former employs multipliers and correlators to estimate and cancel out the 2^{nd} and 3^{rd} order harmonic distortion components while the latter approach builds the inverse V-F function using a digital frequency locked loop. Both methods require a matching-sensitive replica-VCO, while the use of digital lookup tables (LUT) for adaptive post-distortion are a major source of dynamic power consumption, in addition to the slow convergence time of the calibration algorithm.

VCO-based ADCs with most competitive figure-of-merit (FOM) use a two-step 0-1 MASH architecture. The coarse and fine quantizers process the entire signal and its residue respectively. The final combined digital output cancels the dominant first stage quantisation error and non-linearity. VCO-based ADC is used in both stages [7] to make use of the intrinsic DEM for the feedback DAC, while [8] employs dithering to remove fine-stage spurious input-dependent tones. It is worth noting that the above-mentioned distortion cancellation is strongly dependent on the matching between the DAC and VCO gains.

The focus is shifted from linearisation to bandwidth extension of the VCO-based ADC up to the Nyquist rate in [9]. The 20 dB/decade noise shaping which overwhelms higher frequencies is removed by differentiating the input in the analog domain and quantised using a TDC. The high pass operation attenuates lower frequency inputs (a more linear region of the VCO tuning curve is exercised), but on the contrary, degrades the system SNR due the oscillator phase noise, dominant indeed at low frequency. For this reason, such topology is more suitable for band-pass applications.

III. Proposed Architectures

A. Injection-locked Oscillator-based ADC

In the majority of published literature, the effect of the nonlinear V-F tuning curve is mitigated by embedding the oscillator-based ADC within some system architecture. An alternative approach would be to linearise the oscillator at circuit level, thus inherently solving its nonlinearity. It has been shown by using the RF principle of injection-locking [1], the oscillator frequency tuning curve can be made reasonably linear thus improving the dynamic range of the ADC. The concept of self-injection locking is shown in Fig. 1, with a proof-of-concept first prototype applied to a SILRO-ADC. [10].

The ring oscillator outputs are multiplied by the input signal using mixers, and the resulting envelope modulated waveform (Vo_mix) is injected backwards at a different RO output node in the form of current (I_inj), obtained

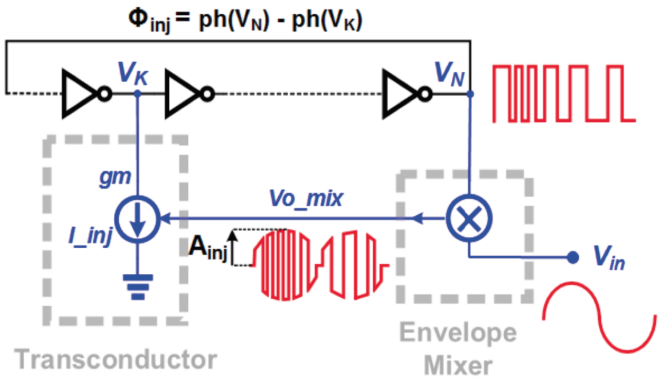

Fig. 1. SILRO-ADC concept block diagram [10].

using a transcondutor (gm). The injected current modulates and linearise the frequency by varying the phase contribution and thus delay of each stage in the ring, while multi-point injection increases the tuning range and provides current at every delay stage to avoid phase imbalance. In order to outline the input voltage versus oscillation frequency characteristic, the ring oscillator has been modelled, considering its delay stages as ideal transcondcutors with fixed parallel RC load, and considering only sinusoidal voltage and current waveforms. Under such approximations, the analysis of the current/voltage phasors of the circuit has given the indication that frequency can, to the first order, be directly proportional to the input voltage. This relationship holds as long as the amplitude $(Ainj)$ and phase (ϕ_{inj}) of the injected signal are properly selected.

Extensive simulations of a first designed prototype (using TSMC 28nm LP CMOS process) have been performed, with the aim of fully characterising its performance and identify circuit non-idealities. Applying a full-scale (FS) input sinewave at 100 kHz and 1.8 V amplitude, the suprious-free dynamic range (SFDR) is 18.6 dB at the third harmonic, at a power consumption of 64.5 mW. Fig. 2 shows the system SNDR in different cases: perfectly linear and nonlinear transfer curves, for both a noisy and noiseless oscillator. As visible from the plots where nonlinearity is enabled, the optimum input voltage range is around 400 mV. Several non-idealites in the physical implementation, however, still severely impair the overall system SFDR. The mixer nonlinearity and the channel length modulation of the transistors used in the transconductor stage are major second-order effects. Consequently, these effects have not been accounted for in the theoretical assumptions of the self-injection-locked loop. This is indeed, the source of the discrepancy between the expected theoretical and actual performance of the SILRO.

B. Ultra-low-voltage Oscillator-based ADC

An alternative proposal is presented to address the ever growing power efficiency requirements and shrinking supply voltages for advanced process nodes. A ULP, ULV VCO-based ADC operating in weak-inversion with a supply voltage of 0.2 V is demonstrated in Fig. 3. The input is AC-coupled to $M_{C,N}$ and $M_{C,P}$, whose gate bias voltage is respectively boosted to 400 mV and -200 mV using switched-capacitor DC-DC converters (voltage doubler and voltage inverter), so as to increase their effective transconductance (which ultimately

results in higher VCO gain). Operating in weak-inversion offers optimum power efficiency, however as shown in Fig. 4, the oscillation frequency of a ring oscillator is severely affected by voltage and temperature variations. This is in contrast with a relatively constant oscillation frequency of an oscillator operating in strong-inversion. Indeed, a 0.2 V VCO-based ADC has already been demonstrated in [11], although the impact of process variations, severe in weak-inversion, has not been considered. Consequently, design in weak-inversion therefore requires the adoption of process, voltage and temperature (PVT) aware circuit design approaches.

IV. Circuit Implementation: A 0.2 V Supply VCO

The design of the voltage-controlled-oscillator, traditionally the most critical block, requires balancing of the following parameters: linearity, power consumption, free running frequency, tuning range and phase noise. While a ring oscillator structure is the obvious choice of implementation due to its multi-phase output as well as its wider tuning range, smaller area and lower complexity compared to LC oscillators, the specific ring-VCO topology to pick is not a straight-forward design decision. Fig. 5 shows the four delay stage topologies considered, where terminals IN and OUT correspond to the output of the previous delay stage, and input of the following delay stage respectively. The terminals INP, INN, $OUTP$ and $OUTN$ as shown in the differential configuration of Topology C denote the differential inputs and outputs of the delay stage. Vin denotes a single-ended input signal voltage as seen in Topologies C and D, while $VinN$ and $VinP$ correspond to a differential input signal voltage as seen in Topologies A and B.

The topologies considered are simulated within a 0.2 V supply, 8-stage pseudo-differential configuration with output back-to-back inverters to realign edges (besides Topology C). An additional 20 fF capacitive load is connected at each VCO phase output node to account for wiring and parasitic capacitance. A resistor-based phase interpolation network [12],[13] is utilised to increase the phase resolution of the multi-phase output by a factor of 4, with negligible variation of oscillator power consumption and oscillation frequency.

Topologies A and B are standard current-starved configurations. The input-controlled transconductors of Topology A (the

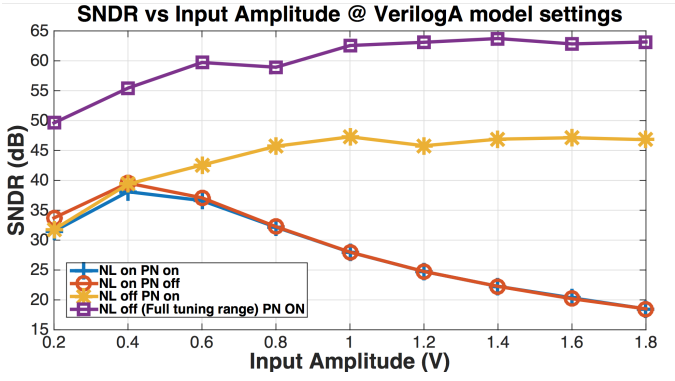

Fig. 2. SILRO-ADC extracted to Verilog-A Model: Input amplitude vs SNDR for nonlinearity (NL) and phase noise (PN) disabled, enabled and if tuning range covered entire frequency count values.

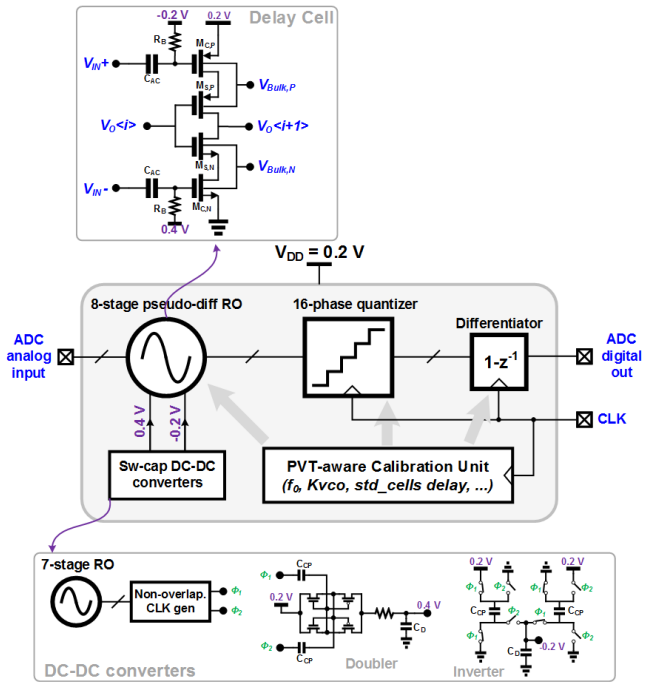

Fig. 3. ULV-VCO ADC block diagram.

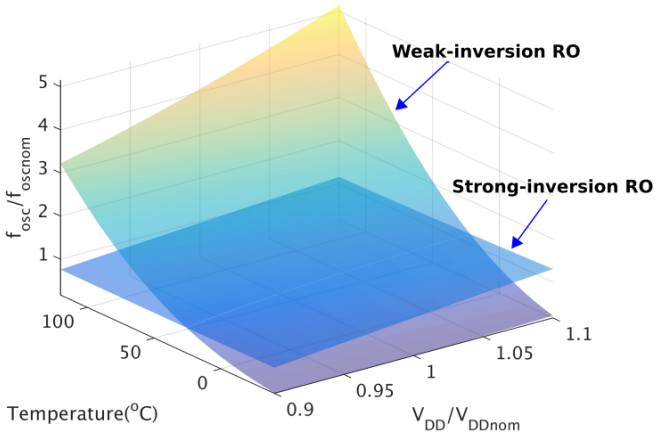

Fig. 4. Ring oscillator normalised frequency under voltage and temperature variations in strong inversion and weak-moderate inversion in TSMC 28nm CMOS.

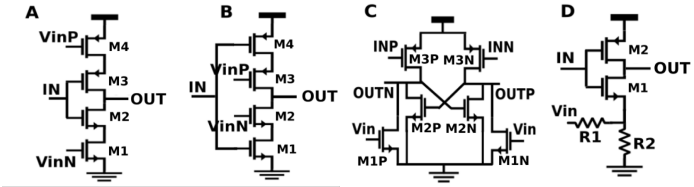

Fig. 5. Investigated ring-VCO delay elements.

PMOS transistor $M4$ and NMOS transistor $M1$ respectively connected to $VinP$ and $VinN$) resemble a common-source current source, while Topology B (the PMOS transistor $M3$ and NMOS transistor $M2$ respectively connected to $VinP$ and $VinN$) resembles a source-degenerated current source. The input-controlled transconductors act to modulate the charg-

TABLE I. VCO TOPOLOGIES PERFORMANCE TABLE.

Topology	A	B	C	D
Frequency (MHz) [-0.1V,0V,0.1V]	[1.7 , 13.5 , 23.3]	[1.31 , 10 , 16.6]	[10 , 16.8 , 43.2]	[28.9 , 18.9 , 11.7]
RMS Power (uW) [-0.1V,0V,0.1V]	[1.2 , 2.6 , 3.5]	[0.9 , 2.5 , 4.4]	[4.1 , 8.8 , 28.7]	[13.9 , 9.8 , 7.1]
Tuning Range (MHz)	21.7	15.3	**33.2**	17.2
HD2 (dB)	**-26.2**	-23.9	-10.0	-22.2
HD3 (dB)	-27.6	-26.3	-26.7	**-66.8**
Phase Noise @ 100kHz (dBc/Hz)	-93.5	**-96.5**	-92.5	-94.5
FOM @ 100kHz (dBc/Hz)	161.9	**162.5**	157.6	160.2

ing/discharging of the load capacitance. The transconductor transistors require large channel length to suppress the effect of channel length modulation, while the W/L aspect ratios have to be large to provide enough current drive in weak-inversion. The inverter transistors (connected to the output of the previous stage, IN in Fig. 5) have low on-resistance to provide more voltage headroom for the transconductors.

Topology C is a pseudo-NMOS inverter ($M2P$, $M2N$) for transition edges realignment, with a PMOS load ($M3P$, $M3N$). The input voltage Vin applied to the gate of the NMOS transistors ($M1P$, $M1N$) changes the transistor's impedance to modulate the frequency. These input-controlled NMOS transistors have to be sized in the appropriate region to offer sufficient tuning range while satisfying Barkhausen Criterion.

The delay stage of Topology D [14] is a standard CMOS inverter, with the NMOS transistor ($M1$) source connected to an input-controlled resistor network. The mixed mode interaction of the control voltage and current acts to provide a more linear V-F tuning. The source impedance of $M1$ and $R2$ have to be small (in the order of a few $k\Omega$) to preserve a wide enough output voltage swing and the proper relationship between Vin and the source voltage of $M1$.

Table 1 compares the performance of VCOs using the delay stage topologies specified in Fig. 5. The oscillator making use of the delay stages from Topology A was chosen based on its overall balancing of power, tuning range and linearity. The oscillator using delay stages from Topology B offers better phase noise performance, but is inferior in all other categories such as VCO V-F nonlinearity (visible from the 2^{nd} and 3^{rd} order harmonic distortion HD2 and HD3[1]), tuning range and power consumption. In this topology, the inverter transistors ($M1$, $M4$) act to decrease the gate-source voltage available to the transconductor transistors ($M2$, $M3$), reducing its effective transconductance, ultimately resulting in a lower tuning range. The oscillators using the delay stages from Topology C and D consume more power as a direct consequence of its higher free-running frequencies. The oscillator using the delay stages from Topology C has a larger tuning range but worse overall performance. The oscillator using the delay stages from Topology D achieves the highest linearity reported so far in simulation using a voltage-controlled ring-oscillator. The HD3 of the VCO-ADC output spectrum when applying a full-scale sinusoidal voltage input, is only -66.8 dB. Such improved linearity is a result of the mixed-mode current-voltage control of the oscillating frequency, in agreement with [14]. The relatively high HD2, however, requires to operate the VCO-based ADC in a pseudo differential fashion (two independent complementary VCO-based ADCs whose digital outputs are eventually subtracted) so as to effectively cancel its contribution [12]. The superior linearity performance eliminates the need to integrate (as an oscillator using delay stages from Topology A would require) within an architecture such as the 0-1 MASH.

[1]The HD2 and HD3 correspond to the 2^{nd} and 3^{rd} order harmonic distortion in the VCO-based ADC output spectrum when applying a full-scale input sinusoidal signal.

V. BEHAVIOURAL MODELLING

With the increasing size and complexity of mixed-signal systems, architectural exploration and design at transistor level becomes time-consuming and inefficient, while modelling approaches which make use of MATLAB and Simulink are highly abstract and far from the physical hardware. Hardware description languages (HDL) for analog design, such as Verilog-A, offer a balanced trade-off between accuracy and efficiency while being integrated within the SPECTRE environment. This section presents the modelling of the two developed oscillator-based ADC embedded within conventional system architectures, following a top-down driven design methodology as the common tool for system development.

A. Voltage-controlled-oscillator

Three major features of ring-VCOs need to be considered: the V-F nonlinearity, the oscillator phase noise (PN), and the multi-phase output (since the system quantisation noise directly depends on the number of different phases).

The V-F characteristic is extracted from a SPECTRE simulation and consequently fitted in MATLAB so as to extract the polynomial coefficients of its Taylor series, which will be used to model the oscillator nonlinear tuning curve.

For what concerns modelling the phase noise of the oscillator, the up-converted flicker and thermal noise ($1/f^3, 1/f^2$ regions of the PN profile) and the white noise region ($1/f^0$) have been modelled in the time-domain following the approach prosed in [15-17], thus in terms of the period timing deviations ΔT_i. The frequency of the oscillator affected by phase noise can be expressed as:

$$f_{fr,i} = \frac{f_{fr}}{1 + \Delta T_i f_{fr}} \tag{2}$$

where $f_{fr,i}$ represents the oscillating frequency of the oscillator during the i^{th} cycle, affected by the period deviation ΔT_i. Such period deviation can be expressed as:

$$\Delta T_i = \Delta\tau_{flicker,i} + \sigma_{wander}\delta_i + \sigma_{jitter}\delta_i - \sigma_{jitter}\delta_{i-1} \tag{3}$$

where δ is a zero-mean, unit-variance Gaussian random variable, $\Delta\tau_{flicker}$ is the period deviation component due to the up-converted flicker noise, σ_{wander} is the standard deviation of accumulating jitter due to time wander (up-converted thermal noise), and σ_{jitter} is the standard deviation of the non-accumulating uniform jitter (white noise).

From [16], the standard deviation of the non-accumulating uniform jitter and accumulating jitter due to wander is derived from the phase noise power spectral density. The flicker noise region is modelled by white noise passing through a series

of single pole IIR low pass filters. The composite response of the filters shapes the input white noise with magnitude response of -10 dB/decade, generating the above mentioned period deviation variable $\Delta\tau_{flicker}$. In order to also account for the multi-phase output of an N-stage ring-oscillator, the authors in [15] divide the oscillation period into 2N jitter update intervals, with each delay stage contributing to the total period timing deviation.

B. System Architectures

The FDC is modeled in Verilog-A as a chain of two flip flops clocked at the sampling frequency to capture the current and previous phase state of each output. An XOR gate compares the two values, and all of the XOR outputs (one per stage) are eventually summed together to obtain the digital count. For the sake of simplicity, second order non-idealities of the digital circuits such as meta-stability, flip-flop setup-hold times have not been modelled.

The open loop model of the SILRO-ADC is embedded within a $\Delta\Sigma$ loop with ideal DAC and loop filter models. The loop filter is modelled by cascading 1^{st} order low pass filters with programmable gain and order. Part of the investigations on this topology aimed to outline how much, thanks to the increased linearity offered by the self-injection-locking, the filter specifications could have been possibly relaxed. Indeed, a low-order, low-gain loop filter would lead to a lower power consumption. It must be noted, however, that this configuration is not applicable to low voltage applications due to the difficulty in designing high gain op-amp integrators.

To explore system integration of the ultra-low voltage VCO employing the oscillator with delay stages from Topology A (Fig. 5), an 0-1 MASH architecture with both coarse and fine stages implemented using VCO-Quantizer [7] has also been modelled. The gain of the DAC is swept to identify its optimum value, which is the one that maximises the SNDR of the ADC output. Timing mismatch between the coarse and fine digital outputs, and between input and DAC feedback output have also been investigated, since these factors can potentially be responsible for performance degradation. Again, it should be noted that the actual implementation of a 0-1 MASH topology at a supply voltage of 0.2 V would be impaired by non-idealities of analog blocks, such as the DAC in this case. Indeed, the design of a current steering DAC (common topology for this class of converters) would be rather challenging due to the severe effect of channel length modulation of its internal current sources.

VI. Simulation Results

This section presents the Verilog-A modelling simulation results for the various system configurations, showing the relative effectiveness, re-usability and speed of this methodology for system level development.

Fig. 6 shows the output spectrum of the SILRO-ADC operated at open-loop (a) and embedded in a $\Delta\Sigma$ loop (b). The former configuration yields a SFDR of 18.5 dB by applying a full-scale input sinusoidal test signal at 1 MHz, while the use of a $\Delta\Sigma$ closed-loop topology, choosing a filter pole frequency and gain of 5 MHz and 5 respectively (a typically relaxed specification on the loop filter) improves the SFDR by almost 16 dB and results in a 40 dB/decade shaping of the quantisation noise. Given its analog intensive nature (loop filter and feedback DAC), it is worth noting again how this architecture may not represent the best choice in terms of power efficiency and amenability to nanoscale CMOS technologies.

Fig. 7 show the SNDR performance of the ULV-VCO-ADC embedded in a 0-1 MASH architecture (same VCO for both coarse and fine quantizers), with the oscillator employing the delay stages of Topology A (Fig. 5) as a function of the normalised DAC gain, at coarse output digital delays of 1, 2 and 3 clock sampling periods (T_s) respectively before addition with the fine-stage output to obtain the combined ADC digital output. The best performance is achieved when the normalised DAC gain is around 1, and when a digital delay of 2 clock sampling periods is applied to the coarse digital output. Indeed, the fine-stage output experiences an additional delay of 2 clock periods relative to the coarse-stage output, introduced by the feedback DAC and fine-quantiser. An identical delay to the coarse digital output compensates for this timing mismatch, leading to a much improved performance. For $1T_s$ and $3T_s$ delays, this required timing resynchronisation is not achieved. Furthermore, a pseudo-differential configuration would not improve performance due to the dominance of the 3^{rd} order harmonic distortion component in this VCO topology, while timing mismatches between the analog input and the DAC output for residue calculation does not degrade system performance.

In the end, promising simulation results have been obtained from a VCO employing Topology D (Fig. 5). Indeed, by operating the VCO-based ADC employing the delay stages of Topology D in an open loop, pseudo-differential configuration, the SNDR with a 1 MHz input full-scale sinewave is around 55 dB, as shown from the output spectrum in Fig. 8.

Fig. 9 shows the SFDR performance of the VCO-based ADC (using the delay stage from Topology D) in the pseudo-differential configuration under global and local statistical process variations, as enabled by a 100-run Monte-Carlo simulation. Evidently, a mean SFDR value of 54.7 dB is achieved, with a standard deviation of 3.7 dB. The degradation in system performance from the nominal SFDR value of 66.8 dB (Fig. 8) is apparent. This, again, highlights the need for process-variation-aware design approaches when operating in weak-inversion mode at a supply of 0.2 V.

VII. Conclusion

Two distinct oscillator-based ADC architectures are proposed in this paper. In spite of their different physical manifestations, a common behavioural modelling procedure can be applied to both in the same manner in order to explore alternative system configurations and evaluate performance with high efficiency, re-configurability and speed. Applying self-injection locking offers an innovative solution to inherently linearise the oscillator at circuit level, while an ultra-low-power, ultra-low-voltage VCO-ADC architecture is proposed for direct energy harvesting applications, suitable for future nanoscale IoT wireless sensor nodes. Additionally, an investigation and performance comparison of four VCO topologies, different as for the delay stages they employ, is presented to provide insights on the best candidate to be chosen, both in terms of linearity and power consumption, for a future CMOS imple-

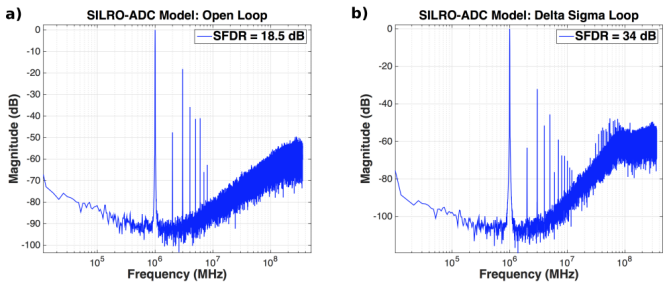

Fig. 6. SILRO-ADC in (a) open loop, (b) in 1^{st} order loop filter $\Delta\Sigma$ loop.

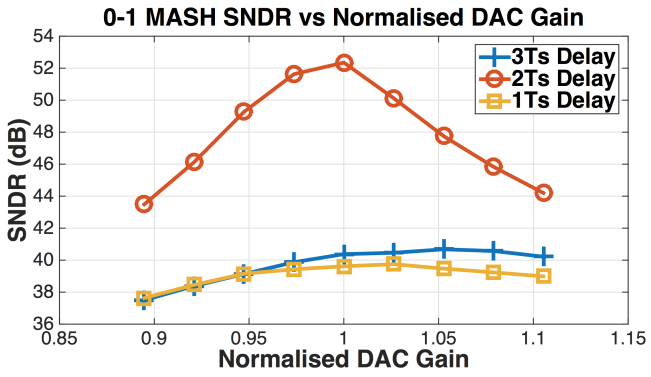

Fig. 7. 0-1 MASH ADC SNDR as a function of the DAC normalized gain with coarse quantizer output delayed by 1, 2 and 3 Ts before final summation.

mentation. Ultimately, a top-down driven design methodology binds these different concepts together with the construction of an accurate and fast Verilog-A model to demonstrate a holistic approach for system development.

VIII. Acknowledgements

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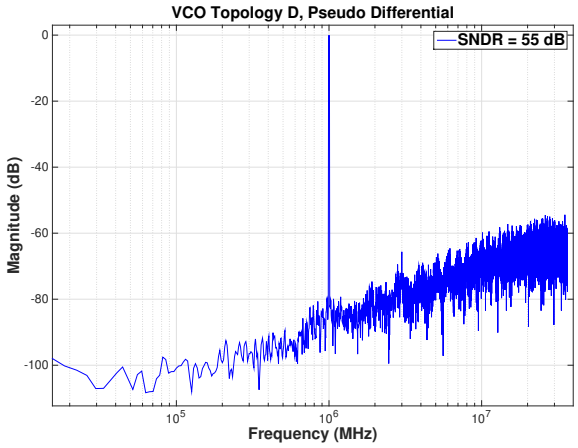

Fig. 8. Output spectrum for a VCO-based ADC with oscillator employing delay stages from Topology D, in pseudo-differential configuration.

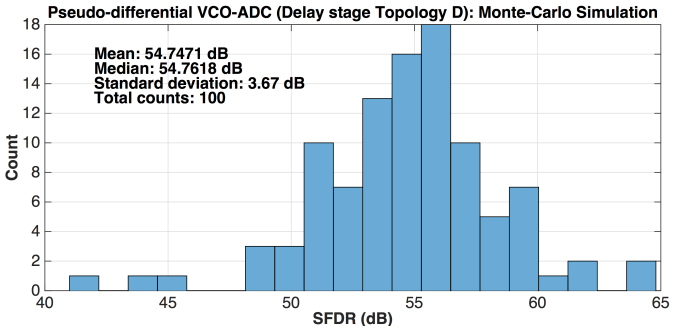

Fig. 9. Statistical distribution of the pseudo-differential VCO-based ADC SFDR using delay stages of topology D, with 100 Monte-Carlo runs.

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