Merging of RF Oscillator and Power Amplifier to Enable Fully Integrated Transmitters for Internet-of-Things

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2019
Merging of RF Oscillator and Power Amplifier to Enable Fully Integrated Transmitters for Internet-of-Things

by

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The thesis is submitted to University College Dublin
in fulfilment of the requirements for the degree of

Doctor of Philosophy

School of Electrical and Electronic Engineering

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September 2019
To my lovely parents and sister
“It is loneliness that makes you different, not gregariousness.”
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Abstract

To facilitate the ever-increasing influx of the Internet-of-Things (IoT) wireless connectivity, the investigation for power efficient and cost effective wireless devices together with the trend towards fully integrated solutions have opened up a new wave of challenges and opportunities for ultra-low-power (ULP) RF integrated circuit design. The full integration of the power-hungry battery-operated CMOS transmitter (TX) is especially challenging and confronted by the down-scaled power supply, lossy on-chip passives and low-resistivity silicon substrate of nanoscale CMOS technology. This sets different requirements for devices working in different RF bands, mainly the 900MHz (sub-GHz) and 2.4GHz bands in terms of range coverage, data rate, maximum allowed RF power, etc.

Specifically, the Bluetooth Low Energy (BLE) as the mainstream standard for IoT applications in that the 2.4GHz band is constrained by the transmitter system efficiency $\eta_{TX}$ due to the fact the power dissipated by the modulator $P_{DC,MOD}$ is generally comparable or even higher compared to the delivered RF power $P_{RF}$ by the power amplifier (PA). Furthermore, $P_{DC,MOD}$ cannot scale down when the PA operates at large power back-off. On the other hand, the 802.11ah, or equivalently WiFi-HaLow, sits in the 900MHz (sub-GHz) band targeted for long-range wireless connectivity which faces the greatest challenge of inexpensively integrating the RF passive components, especially inductors and transformers utilized for frequency generation or impedance matching.

In this thesis, we propose to merge the oscillator (the most power-hungry block in the modulator) and the power amplifier either in the way of “functionally merged” DCO-PA for BLE transmitters in order to boost the system efficiency at large power back-off or in the way of “physically merged” DCO-DPA for WiFi-HaLow transmitters to tremendously
reduce the die area. One chip prototype is fabricated to demonstrate the sub-GHz 802.11ah transmitter (TX) with a physically merged digitally controlled oscillator (DCO) and digital power amplifier (DPA) saving ∼50% of area. The resulting DCO pulling by the DPA is compensated via a feedback path and an inter-winding cancellation capacitor suppresses the 2nd harmonic.

Further, we introduce a super-simple RF front-end with a fully integrated matching network for 2.4 GHz TDD radios featuring a functionally-merged single-MOS DCO-PA and a zero-shifting capacitor that suppresses the 2nd harmonic emission. This not only allows to share the same antenna pin with the RX but also provides passive-gain boosting to an RX low noise amplifier (LNA).
To facilitate the ever-increasing influx of wireless connectivity, the Internet-of-Things (IoT), defined as “the infrastructure of the information society”, has widely expanded from its modest beginning of realizing smart homes or smart grids to reach into the retail and industry markets, such as intelligent transportation and smart cities, with use cases scaling from a single constrained device up to massive cross-platform deployments of embedded technologies and cloud systems connecting in real-time.

Communication (data transfer and processing) between those connected devices in the IoT ecosystem can only be established through encrypted connection. The invisible language behind to enable the “talk” among the physical objects consists of the IoT protocols or standards [1] [2]. To integrate the communications between IoT devices with the Internet, standardization bodies such as the Institute of Electrical and Electronics Engineers (IEEE) and the Internet Engineering Task Force (IETF) have conducted long efforts to design a much necessary wireless communications protocol stack [3]- [5] for the IoT together with the various communication technologies as illustrated in Figure 1.1.

Four layers were introduced to cover the IoT communications stack which attempts to
guarantee the interoperability with existing Internet standards while facing the challenge of exponentially increased traffic. Cost-effective and reliable connection among a large number of heterogeneous elements such as RFID [6] and Machine-to-Machine (M2M) [7] is paramount for IoT networks while developing the standardized protocol stack [8] [9] [10]. The thesis will primarily focus on the design and implementation of ultra-low-power (ULP) wireless devices which are compatible with communication technologies such as IEEE 802.15.4e, IEEE 802.11ah, SigFox, NB-IoT, Zigbee, Bluetooth Low Energy (BLE), etc. with innovative solutions at the Physical (PHY) layer to achieve lower power consumption and longer battery life.

1.1 IoT Data Link Protocols

This thesis mainly concentrates on the innovative solutions for high-efficiency low-power wireless devices in the PHY layer applicable to different standards and application scenarios. ULP wireless transceiver plays a pivotal role in the current development of wireless system on a chip (SoC) due to the fact that it occupies more than 70% of the total power consumption [11].

A brief overview of several popular wireless standards which have paved the way for low power transceiver design is given in Figure 1.2. In general, they can be categorised into two RF bands, namely the 900 MHz (sub-GHz) band and the 2.4 GHz band with different range coverage, data rate, maximum allowed RF power and power consumption. The sub-GHz band can usually provide large transmission coverage range with better propagation and
penetration ability considering only the effect of path loss. For instance, the 802.11ah (Wi-Fi Halow) standard is able to transmit at reasonable rates up to 1 km compared against the 50 m range of conventional 802.11 (Wi-Fi) standards operating in the 2.4 GHz and 5 GHz bands. Additionally, the extensively deployed BLE and Zigbee devices in the 2.4 GHz band can merely offer approximately 100 m coverage range. Another benefit of the sub-GHz band lies in the lower probability to encounter interference or congestion in contrast to the crowded 2.4 GHz.

Nevertheless, the utilization of the sub-GHz band is restricted to a very specific short list of jurisdictions. Contrarily, the deployment of the 2.4 GHz band is worldwide-harmonized. The 802.11ah [12] has defined the channelization according to the radio spectrum availability of different countries which exhibits no common frequency range. It only shows a 3.5 MHz shared frequency range at the sub-GHz band among few countries as described in Figure 1.3 bringing inconvenience to the expansion of products and services globally. Notwithstanding, the 2.4 GHz band is the only common frequency band allocated worldwide that can be accessed freely without license, improving the harmonisation in spectrum utilization. On
the other hand, this band is heavily congested and thus more susceptible to interference. Additionally, the sub-GHz band would suffer from relatively larger RF components especially when downsizing of the devices for wireless sensor network is favoured.

1.2 RF Transmitters

The quest for power-efficient and low-cost wireless connectivity together with the trend towards fully integrated solutions have opened up a new wave of challenges and opportunities for ULP RF integrated circuit design. Along with this integration, board level designs are simplified, requiring fewer external components. Since it has the direct bearing on the battery life and reliability, the full integration of an efficient CMOS transmitter and, in particular, the power amplifier (PA) is still of the greatest challenge [13] in terms of the scaled supply voltage of nanoscale CMOS, the lossy on-chip passives and low-resistivity silicon substrate [14], especially when the size of low energy devices is more constrained in the IoT era.
1.2 RF Transmitters

1.2.1 Transmitter Architectures: Direct-Conversion TX

A wireless transmitter (TX) aims at communicating data over a wireless channel through modulating a higher frequency carrier signal which is converted into the format of electromagnetic wave by an antenna. Conventional direct-conversion TX utilizes orthogonal vectors, namely, in-phase ($I$) and quadrature-phase ($Q$) to describe a Cartesian coordinate system as shown in Figure 1.4. The baseband digital I/Q data applied to the digital-to-analog converter (DAC) are converted to the analog domain. Low-pass filter (LPF) is commonly cascaded to eliminate the undesired noise and spectral replicas. The filtered analog signals are then up-converted to the designated carrier frequency by employing a quadrature mixer that receives carrier frequency from the local oscillator. The power amplifier (PA) is optimized to efficiently boost the combined outputs from the mixers to deliver anticipated RF power. The RF signal resulting from combination of the quadrature modulators ($V_{RF}$) can be expressed as

$$V_{RF} = I \cdot \cos (\omega_c t) + Q \cdot \sin (\omega_c t)$$  \hspace{1cm} (1.1)

where $\omega_c$ represents the RF carrier frequency. The Cartesian transmitter earns its popularity in all kind of wireless systems mainly due to its simplicity in which the circuit merely mirrors the Cartesian expression of $V_{RF}$ in Equation (1.1). The almost linear operation of up-converting the baseband I/Q to RF signals is another benefit belonging to the Cartesian TX. Advances in this area have covered various wireless standards for cellular or Wi-Fi applications, even with multi-standard multi-band solutions [15]– [21]. The RF signal $V_{RF}$ has both amplitude and phase information when complex modulation like 16/64/256 QAM.
is engaged. Since the input driving signal to the PA has a non-constant envelope, linear PAs (class A/AB/B) are preferred but inevitably come at significant compromise on power efficiency in comparison to switching PAs (class D/E/F).

One non-ideality of the direct conversion architecture is the carrier leakage attributable to parasitic coupling leaking through and popping on top of the RF signal at the output. Eventually, it introduces DC offsets and causes distortion to the I/Q data. The I/Q imbalance as another non-ideality which may originate from the amplitude imbalance or phase (LO) imbalance having the visible effect of deforming the constellation diagram, as shown in Figure 1.5(b). Techniques to calibrate the carrier leakage or compensate the I/Q imbalance have been discussed in [22] [23]. Furthermore, the LO pulling [24] [25] is also considerably challenging in direct conversion TXs when the voltage-controlled oscillator (VCO) generates the LO signals operating at the same frequency as the PA. Substantial noise on the power supply and silicon substrate produced by the PA can find its way to the VCO through a coupling path, thus pulling the oscillator. It is therefore favored to separate the VCO frequency from that of the PA in order to mitigate injection pulling [26].

1.2.2 Transmitter Architectures: Polar TX

The polar architecture has materialized as a promising approach to improve the overall system efficiency through linearizing the operation of more efficient switching PAs. In a polar TX, the baseband data is encoded in the format of amplitude (A) and phase (φ) instead of I
and \( Q \) in the Cartesian TX, as the expression in Equation (1.2) and Equation (1.3).

\[
A = \sqrt{I^2 + Q^2} \tag{1.2}
\]

\[
\phi = \tan^{-1}\left(\frac{Q}{I}\right) \tag{1.3}
\]

This conversion is realized through a CORDIC algorithm with non-linear operations. The phase information \( \phi \) is superimposed on a RF carrier to create a phase-modulated RF signal \( \phi_{RF} \) which can be easily differentiated to obtain frequency deviation. Due to the constant-envelope nature of \( \phi_{RF} \), highly-efficient switching-mode PAs can be employed. Early example of the polar modulation is the envelope-elimination and restoration (EER) technique proposed by Kahn [27]. In the EER system, the PA acts as the “combiner” of the efficiently amplified constant-envelope phase information and the detected-restored envelope (amplitude) information. Feasibility of such architectures in CMOS have been demonstrated in [28] [29] [30]. The fact that the complex large bandwidth supply modulator is needed has restricted the popularity of the EER architecture.

To get rid of the supply modulator, the digitally controlled power amplifier (DPA), which functions as a digital-to-RF-amplitude converter (DRAC), is introduced for the power ramp and amplitude modulation [31] [32] [33] [34]. The DPA can adopt non-linear efficient switching PA topology with digitally controlled switch resistance and master the envelope of the phase-modulated carrier by means of turning on and off an appropriate number of unit cells. In the meantime, the phase-modulated digital carrier is generated through the DCO-based digital-to-frequency conversion (DFC). Figure 1.6 illustrates an application of the digitally intensive wireless transmitter performing an arbitrary quadrature amplitude modulation (QAM). The digitally intensive mixed signal polar structure will also benefit from technology scaling. Noting that the approximately linear characteristic of the digital-to-RF-amplitude conversion will become saturated for high RF output powers, more ongoing research focuses on the switch-capacitor PA which achieves accurate amplitude control through exploiting the precise capacitance ratios that CMOS traditionally provides [35] [36] [37] [38] [39].
1.2 RF Transmitters

Figure 1.6: A digitally modulated polar transmitter based on a DCO and DPA circuits (neglecting the PLL).

1.2.3 Challenges and Solutions to WiFi-HaLow and BLE TX

Low-power and low-cost is paramount for IoT transmitters. In addition to the evolution of techniques in the power amplifier (PA) area aspiring to break the efficiency/linearity trade-off for wireless devices using spectrum-efficient complex modulation schemes, much of recent advance has been obtained in the digitally controlled oscillator (DCO) design which is another energy-hungry circuitry in the TX chain. The phase noise (PN) requirements for oscillators towards IoT applications are fairly trivial and can be easily satisfied by LC oscillators as long as Barkhausen start-up criteria are satisfied over process, voltage and temperature (PVT) variations [40]. Subsequently, minimizing the oscillator’s power consumption $P_{DC}$ turns out to be the ultimate target. The power drain of an RF oscillator is derived as

$$P_{DC} = \frac{2V_{DD}^2}{R_{in}} \cdot \frac{\alpha_V}{\alpha_I}$$  \hspace{1cm} (1.4)$$

where $\alpha_I$ is the current efficiency, defined as a ratio of the fundamental current harmonic $I_{\omega_0}$ over the oscillator DC current $I_{DC}$; and $\alpha_V$ is the voltage efficiency, defined as a ratio of the single-ended oscillation amplitude, $V_{osc}/2$, over the supply voltage $V_{DD}$. Phase noise and figure-of-merit (FoM) of any RF oscillator at an offset frequency $\Delta\omega$ from the resonance
frequency can be given respectively,

\[ \mathcal{L}(\Delta \omega) = 10 \log_{10} \left( \frac{K T}{2Q^2_t \alpha_I \alpha_v P_{DC}} \cdot F \cdot \left( \frac{\omega_0}{\Delta \omega} \right)^2 \right) \]  

(1.5)

\[ \text{FoM} = 10 \log_{10} \left( \frac{10^3 K T}{2Q^2_t \alpha_I \alpha_v} \cdot F \right) \]  

(1.6)

Inspired by Equation (1.4), lifting up \( R_{in} = L_p \omega_0 Q_t \) simply via a large multi-turn inductor [41] seems a quite attractive approach to achieve lower \( P_{DC} \). Nonetheless, it comes at a great cost of PN performance owing to the dramatic \( Q \)-factor drop at some point as characterised by Figure 4(a) in [40] where the magnetic and capacitive coupling to the low-resistivity substrate becomes more severe with enlarging the inductance. Thus, the attempt to reduce the power consumption by operating the DCO at a lower supply is straightforward, provided that a relatively large signal swing is maintained for the purpose of PN and FoM performance. In other words, it is desired to employ structures with a lower minimum \( V_{DD} \) and a higher \( \alpha_I \) as \( \alpha_V \cdot \alpha_I \) should be maximized to avoid any penalty on FoM [42]. A transformer-feedback oscillator [43] [44] is a widely adopted promising topology for ULV operation attributed to its passive RF voltage gain. However, the gates and drains of the crosscoupled transistors in [43] share the same DC voltage. This causes the resonance frequency, mainly due to its voltage-dependent gate capacitance, \( C_g \), to strongly track (i.e. be pushed by) the supply voltage, \( V_{DD} \). Furthermore, a 0.2V trifilar-coil oscillator was proposed in [45] to enable the sub-\( V_t \) operation with only 0.6mW power consumption. The introduced tertiary feedback not only enhances the passive voltage gain between gate voltage (VG) and source voltage (VS) swings but also reinforces 3rd-harmonic injection bringing benefits of a higher oscillation amplitude and sharper rising/falling edges. Even though the sub-mW low-power oscillator is accessible, the overall system efficiency \( \eta_{TX} \) of the transmitter targeted at ULP applications will be hugely affected by the oscillator which serves as the most power-hungry block in the phase-locked loop (PLL) utilized for channel selection and frequency modulation (FM). Particularly, \( \eta_{TX} \) in a PLL-based GFSK polar transmitter [46] with a two-point modulation [Figure 1.7] can be expressed as in [47]:

\[ \eta_{TX} = \frac{P_{RF}}{P_{DC,PA} + P_{DC,MOD}} \]  

(1.7)
wherein $P_{RF}$ is the delivered RF power from the PA, $P_{DC,PA}$ is the DC power drawn by the PA and $P_{DC,MOD}$ stands for the power dissipated for data modulation (i.e., the PLL DC power consumption) of which the lower boundary is determined by the oscillator. Rearranging Equation (1.7) as a function of the PA-only efficiency ($\eta_{PA}$):

$$\eta_{TX} = \frac{\eta_{PA}}{1 + \eta_{PA} \cdot \frac{P_{DC,MOD}}{P_{RF}}}$$ (1.8)

Intuitively, the overall system efficiency $\eta_{TX}$ as a function of ratio between modulator power consumption $P_{DC,MOD}$ and RF power delivered $P_{RF}$ under different PA efficiency $\eta_{PA}$ is plotted in Figure 1.8. It demonstrates that when the power consumed by the modulator $P_{DC,MOD}$ is comparable to the delivered RF power $P_{RF}$, the overall efficiency $\eta_{TX}$ would be severely degraded. Even if some fantastic techniques can be explored to improve $\eta_{PA}$ by 10%, it may end up showing less than 5% advantage. This is commonly seen in BLE transmitters with programmable RF output power typically $P_{RF} \leq 0$ dBm where the modulator power $P_{DC,MOD}$ primarily ascribed to either a PLL [48] [49] or an open-loop oscillator [40] [50] can not scale with $P_{RF}$. In cases the ULP BLE device is migrated into medical applications and Wireless Body Area Networks (WBAN) to achieve efficient medical sensor data processing and data fusion with $P_{RF} = -10$ dBm [51], its overall efficiency $\eta_{TX}$ is restricted to be roughly 2% with $\frac{P_{DC,MOD}}{P_{RF}} \approx 10$ exhibited in [48] and [52]. As a result, it is expected that the
functionality of the conventional oscillator and the power amplifier can be merged somewhat so as to provide similar scalability to the oscillator when the RF output power is moderated and to optimize integrally rather than individually, by this means, higher overall transmitter efficiency $\eta_{TX}$ can be attained in the “$P_{\text{DC,MOD}}$-limited” BLE transmitters. By breaking the compromise between $P_{\text{DC,MOD}}$ and $\eta_{TX}$, new challenges may arise in terms of efficiency-phase noise tradeoff, interference immunity and spurious emissions.

The situation with WiFi-HaLow transmitter is totally different. Instead of “$P_{\text{DC,MOD}}$-limited”, the system efficiency $\eta_{TX}$ is more “$\eta_{PA}$-limited”. Since the transmit RF power is set at the level of 10 dBm, it can be deduced that $\eta_{TX} \approx \eta_{PA}$ from Equation (1.7) on the condition that $P_{\text{DC,MOD}} \ll P_{\text{RF}}$, moreover, this can be further confirmed by the efficiency curves sitting between the interval $\frac{P_{\text{DC,MOD}}}{P_{\text{RF}}} \ll 1$ in Figure 1.8. Energy-efficient WiFi-HaLow transmitter is achievable through maximizing its PA efficiency with the cutting-edge sub-mW PLLs [41] [53] [54] [55] [56] [57].
However, the greatest challenge faced by sub-GHz transmitters is that full on-chip integration of inductors and transformers utilized for frequency generation or impedance matching tends to be rather bulky, increasing silicon area and system cost. With the continuous downscaling of CMOS technology, the transistor feature size decreases every generation, making digital circuits ever smaller in area. However, the RF circuits do not substantially benefit from the technology scaling, since the size of passive components at a given frequency is relatively constant over technology nodes. Thus, solutions which employ fewer passives, have smaller form-factor and scalability to emerging technology nodes would be very attractive. Rather than merging the oscillator and PA functionally in the BLE transmitters, it is more encouraging for the WiFi-HaLow transmitters to merge them physically in a compact concentric octagon layout pattern through placing the matching transformer of the PA inside the oscillator transformer with new techniques to mitigate more severe PA-to-Oscillator pulling induced by either harmonics or magnetic coupling.

Brief schematic diagrams of the proposed solutions for “$P_{DC,MOD}$-limited” functionally merged BLE transmitters and physically merged “$\eta_{PA}$-limited” WiFi-HaLow transmitters are depicted in Figure 1.9.
1.3 Thesis Objectives and Outline

In this thesis, the first-ever viable solutions for the merging of RF oscillator and power amplifier to break the aforementioned “η_{PA}-limitation” and “P_{DC,MOD}-limitation” in modern fully integrated transmitters are demonstrated to secure lower cost and higher efficiency without violating the frequency pulling, phase noise and harmonic distortion requirements, which is paramount for the ULP IoT system. Chip prototypes of the physically merged DCO-DPA in the sub-GHz band and the functionally merged DCO-PA in the 2.4 GHz band are fabricated in the 16-nm CMOS and 65-nm CMOS, respectively, showing superior and competitive performance compared to the conventional solutions. Furthermore, the concept of inherent harmonic suppression through engineering the transmission zeros in monolithic transformers targeted for PA impedance matching is proved by mathematical and experimental results.

The rest of the thesis is organized as follows: Chapter 2 presents a sub-GHz transmitter (TX) with a physically merged digitally controlled oscillator (DCO) and digital power amplifier (DPA) saving ~50% of area. The resulting DCO pulling is compensated via a feedback path and an inter-winding cancellation capacitor suppresses the 2nd harmonic. Chapter 3 introduces a super-simple RF front-end with a fully integrated matching network for 2.4 GHz TDD radios featuring a function-reuse single-MOS DCO-PA and a zero-shifting capacitor that suppresses 2nd harmonic emission. This not only allows to share the same antenna pin with the RX but also provides passive-gain boosting to a RX low noise amplifier (LNA). The comparison between the two transformer-based harmonic rejection techniques using a feedback coupling cancellation (FBCC) capacitor or a zero-shifting capacitor is made in Chapter 4. Chapter 5 concludes the thesis and gives future research directions.
This chapter presents a sub-GHz transmitter (TX) with a physically merged digitally controlled oscillator (DCO) and digital power amplifier (DPA). The matching transformer of single-ended DPA is placed inside the DCO transformer to save $\sim 50\%$ of area. The resulting DCO pulling is compensated via a feedback path and an inter-winding cancellation capacitor suppresses the 2nd harmonic. Fabricated in 16-nm FinFET CMOS, the DPA reaches 51% efficiency at 11 dBm output with $<-55\text{dBc}$ HD2. The 1.8 GHz DCO exhibits -116 dBc/Hz phase noise (PN) at 1 MHz offset and draws 195 $\mu$W from 0.3 V supply. The EVM measured with a 2MHz 64-QAM OFDM signal at 5 dBm average power is 3.7%.

2.1 Introduction

IEEE 802.11ah aims to facilitate ultra-low-power (ULP) and low-cost wireless connectivity in the 900 MHz band. It is indispensable for a number of Internet-of-Things (IoT) applications, such as Smart Home and Smart City, where the coverage range of IoT devices is more
important than the data throughput. Furthermore, it is less prone to interference compared to the more popular standards, such as Wi-Fi, Bluetooth and ZigBee, in the crowded 2.4 GHz band. Unfortunately, the relatively low sub-GHz band makes it very difficult to inexpensively integrate RF passive components, especially inductors or transformers utilized for frequency generation or impedance matching, in a way it has been successfully done at 2.4 GHz \cite{58} \cite{40} \cite{59}. For the sake of frequency tuning and frequency selection in the sub-GHz band, a larger inductor is preferred in a parallel inductor-capacitor (LC) resonant tank to maintain a reasonable tank quality factor $Q_T$ which is dominated by the inductor’s $Q_L$. The larger inductor requires a larger radius $r$, inevitably increasing the size, thus ultimately the cost, which is rather against the low-cost philosophy of IoT. In this chapter, we attempt to address this issue by proposing a highly compact fully integrated digital RF front-end, i.e., a digitally controlled oscillator (DCO) and an 8-bit digital power amplifier (DPA), of a 900 MHz-band transmitter.

The following innovations are introduced: Firstly, to increase power efficiency and reduce area, while monolithically integrating all matching-network (MN) components, the DPA adopts a single-ended class-EF topology with a digitally controlled switch resistance. The unavoidable increase in its 2nd harmonic (i.e. HD2) will get self-suppressed by a cross-coupling capacitor $C_C$ across the DPA transformer windings. Secondly, a concentric octagon topology, as shown in Figure 2.1(b), merges the DCO and DPA transformers, and places all active components vertically underneath, thus saving $\sim$50\% of die area compared to conventional

![Figure 2.1: Layout topologies: (a) conventional side-by-side arrangement of oscillator and PA inductors/transformers; and (b) proposed concentric octagon layout topology.](image-url)
2.2 Self-Suppression of HD2 in Power Amplifier

TXs [60]- [62], in which the inductors/transformers dominate the area [see Figure 2.1(a)]. This is far more effective in terms of cost reduction than, for example, with purely vertical integration of associated components underneath their respective transformers [63]. The resultant pulling of DCO by DPA, which can create distortion during non-constant envelope modulation, will be cancelled through a compensating controllable DCO-PA coupling. Thirdly, the DCO uses ULP techniques to bring its power dissipation to below 0.2 mW at 0.3 V supply.

The rest of the chapter is as follows: Section 2.2 introduces a new second-harmonic suppression technique for the single-ended PA topology. The key innovation of DCO pulling mitigation by steering a PA-to-DCO injection and the low power characteristic of DCO are investigated in Section 2.3. Section 2.4 reveals the top-level implementation of the prototype with experimental results. Section 2.5 wraps up the chapter with conclusions.

2.2 Self-Suppression of HD2 in Power Amplifier

A differential PA topology is commonly used to suppress second-harmonic (HD2) emissions that could violate the spurious emission limits of a wireless standard. However, its effectiveness is restricted by the devices’ mismatch and asymmetry. A rise-edge-synchronized harmonic calibration (RESHC) technique in [60] compensates the duty-cycle imbalance and phase offset between the PA’s differential inputs. To suppress HD2 in a single-ended topology, one cannot merely rely on filtering by an inductor in a matching network (MN) or even an LC band-pass filter. This is due to the limited loaded Q-factor of monolithic inductors. Consequently, a conduction-angle (or, equivalently, duty-cycle) calibration technique was proposed by [64], although it was demonstrated with off-chip MN components. A further implementation in [65], which combines the duty-cycle calibration and LC filtering, managed to cancel out HD2. However, the output RF power is restricted by the necessarily lower duty cycle. All the above techniques are at the expense of an additional system complexity and power consumption.

2.2.1 Analogy with Neutralization

An example of a general neutralization technique in high-frequency tuned amplifiers is depicted in Figure 2.2(a). A neutralization capacitor $C_N$ is inserted between the (inverted) output and input ports of an amplifier to cancel the undesired coupling in the feedback
path caused by a parasitic capacitance $C_F$, which could be due to a gate-drain capacitance ($C_{gd}$) in a common-source amplifier. We adapt this technique to achieve our objective of deep HD2 suppression in a single-ended RF PA, as proposed in Figure 2.2(b). A single feedback coupling cancellation (FBCC) capacitor $C_C$ connects across the windings of the PA’s matching-network transformer in the inverting configuration. Unlike in the conventional neutralization technique which copies the inverted output signal into the amplifier’s input, thus being effective only near the operating frequency $f_0$ of the amplifying device [66], the introduced $C_C$ copies the signal from the secondary to the primary winding of the transformer for the purpose of cancelling out the the second-harmonic $2f_0$.

The cancelling capacitor $C_C$ appears to artificially affect the transformer’s inter-winding capacitance $C_{int}$, where the feedback signal at $2f_0$ has an equal amplitude to the HD2 component at the common drains of the DPA but is 180° out of phase. In both cases, a perfect cancellation will require precise anti-phase duplicates of the undesired signals. This is in contrast with [67], where the transmission zero inherent with the non-inverting transformer
is shifted to reject HD2. In Figure 2.2(a), to achieve zero net feedback at the input, the neutralization capacitor $C_N$ has to be

$$C_N = C_F \frac{L_{1b}}{L_{1a}} \quad (2.1)$$

where the unwanted feedback hinges on the amount of lumped parasitic $C_F$. For the case of the proposed feedback coupling cancellation, the optimum $C_C$ to realize the complete HD2 suppression will be dependent on the exact strength of the undesired second-harmonic component at the common drain of the switch array incurred by the hard switching and load network. The feedback current is given by

$$i_f = s (C_c + C_{int}) \cdot (V_{out} - V_{in})$$

$$= s (C_c + C_{int}) \cdot V_{in} \cdot [G(s) - 1] \quad (2.2)$$

wherein $G(s) = V_{out}/V_{in}$ indicates the tank’s voltage gain transfer function. When considering the effect of FBCC capacitor $C_C$ and interwinding capacitance $C_{int}$, $G(s)$ is derived in a long formula in Equation (2.3) with $C_{tot} = C_C + C_{int}$, representing the total (inverting) feedback coupling capacitance. By assigning $C_{tot} = 0$ to both the numerator and denominator of $G(s)$, the transfer function for a case of neglecting the feedback coupling effect can be easily deduced. By simply sweeping $C_C$ in a harmonic balance simulator, we can get the optimum $C_C \approx 247 \text{fF}$ in this implementation to achieve the HD2 emission suppressed to $<-55 \text{dBc}$, that is, the feedback current $i_f$ almost perfectly cancels out the HD2 current $i_{sec}$ at the common drain node. The simulated HD2 suppression under PVT variations is shown in Figure 2.2(e), which proves it is fairly well contained. At room temperature, the worst-case happens at $+10\%$ $V_{DD_{DPA}}$ variation with the HD2 level of -47dBc. Under more severe variations, the programmable load capacitance $C_L$ can also be tuned to compensate for the suppression degradation introduced by the PVT.

$$G(s) = \frac{\left[ (L_p L_s - M^2) s^3 + \left( L_p r_s + L_s r_p \right) s + r_p r_s \right] C_{tot} s + M s}{\left( L_p L_s - M^2 \right) (C_{tot} + C_L) s^3 + \left( L_p r_s + L_s r_p \right) \left( C_{tot} + C_L \right) s^2 + \left( L_p + (C_{tot} + C_L) r_p r_s + \frac{L_p r_s + L_s r_p}{R_L} \right) s + \frac{r_p r_s}{R_L}} \quad (2.3)$$
2.2 Self-Suppression of HD2 in Power Amplifier

2.2.2 Transfer Function of the Tank with $C_c$

After substituting the design parameters of the proposed passive network into $G(s)$, the Bode plot of Figure 2.3 is obtained. At low frequencies, the magnetizing inductor $L_m = k_m^2 L_p$ of the primary will shunt the energy to ground. Therefore, the first pole can be estimated as $\omega_{p1} = r_p/L_p$ only by taking into account $L_p$ and its equivalent series resistance $r_p$ [68]. By applying $r_p = L_p \omega / Q_p$, $r_s = L_s \omega / Q_s$, $C_{tot} \ll C_L$ and assuming $Q_p \cdot Q_s \gg 1$, $G(s)$ in (2.3) can be simplified as a second-order system for frequencies beyond $\omega_{p1}$:

$$G(s) \approx \frac{L_s C_{tot} (1-k_m^2) s^2 + L_s C_{tot} \omega \left( \frac{1}{Q_p} + \frac{1}{Q_s} \right) s + \frac{M}{L_p}}{L_s C_L (1-k_m^2) s^2 + L_s \left[ C_L \omega \left( \frac{1}{Q_p} + \frac{1}{Q_s} \right) + \frac{1+k_m^2}{R_L} \right] s + 1}$$

(2.4)

The complex-conjugate pole pair in (2.4) with corner frequency

$$\omega_n = \frac{1}{\sqrt{L_s C_L (1-k_m^2)}}$$

(2.5)
2.2 Self-Suppression of HD2 in Power Amplifier

introduces a gain peak at frequency $\omega_{pk}$. The damping factor $\zeta$ can be easily derived from the denominator polynomial as

$$\zeta = \frac{1}{2} \left[ \sqrt{\frac{L_s C_L}{1-k_m^2}} \omega \left( \frac{1}{Q_p} + \frac{1}{Q_s} \right) + \frac{1}{R_L} \sqrt{\frac{L_s}{C_L}} \left(1-k_m^2\right) \right]$$

(2.6)

The peak location $\omega_{pk}$ is related to the corner frequency $\omega_n$ as

$$\omega_{pk} = \omega_n \sqrt{1 - 2\zeta^2}$$

(2.7)

With $\zeta \approx 0.4$ in this design, the peak is located roughly at $\omega_{pk} \approx \omega_n$. The Bode plot also indicates that $C_C$ (or $C_{tot}$) has no substantial effect on the frequency response below $\omega_{pk}$, which lies higher than the fundamental resonance frequency $\omega_0 = 2\pi f_0$ designated for frequency selection of the signal. Consequently, the addition of optimal $C_C$ will cancel out the undesired second harmonic (i.e., $2f_0$) with only negligible performance degradation of the desired signal at $f_0$. This observation is supported by circuit simulation results shown in Figure 2.2(c), which reveal only 1% efficiency drop by adding $C_C$.

The numerator of (2.3) also turns out to be a second-order polynomial after taking $C_{tot}$ into account but with a totally different behavior compared to that of the denominator. Zeros of the system are the roots of $N(s) = 0$ with $N(s)$ indicating the numerator polynomial. To simplify the analysis, we rewrite the equation to a more general case $as^2 + bs + c = 0$, where the coefficients $a, b$ and $c$ can be easily mapped to the coefficients of $N(s)$. Accordingly, solutions of $N(s)$ are given by $s = \left( -b \pm \sqrt{b^2 - 4ac} \right) / 2a$. For a transformer in the inverting configuration, the mutual inductance between the primary and secondary windings is negative (i.e., $M < 0$), as a result, $c = M/L_p < 0$. Given that $a = L_s C_{tot} \left(1-k_m^2\right) > 0$ and $b = L_s C_{tot} \omega \left(1/Q_p + 1/Q_s\right) > 0$, it is easy to predicate that there are two real zeros of $G(s)$, thereinto $z_1 < 0$ signifies the zero located in the left half-plane (LHP) of the $s$-domain and the other zero $z_2 > 0$ lies in its right half-plane (RHP). Considering the fact that $C_{tot}$ is on the order of $10^{-15}$ F, this results in $b^2 \ll -4ac \rightarrow |b| \ll \sqrt{-4ac}$. Then, the solutions of $N(s) = 0$ can be estimated as

$$z_{1,2} \approx \pm \sqrt{-\frac{c}{a}} = \pm \sqrt{-\frac{k_m n}{L_s C_{tot} \left(1-k_m^2\right)}}$$

(2.8)

where $n$ represents the turns ratio of the transformer. This highlights that the two real zeros
2.2 Self-Suppression of HD2 in Power Amplifier

Figure 2.4: Bode phase plot for the two adjacent zeros.

$z_1$ and $z_2$, with $|z_1| > |z_2|$, share rather close distance to the imaginary axis in the $s$-plane. The magnitude asymptotes of RHP zeros are identical to those of LHP zeros with a +20 dB/dec slope. However, the phase asymptotes of RHP zeros show similar behavior as LHP real poles, which bring in a $-90^\circ$ phase shift. Because of the complex-conjugate pole pair previously discussed, the voltage gain will drop with a $-40$ dB/dec slope shown as the blue line in Figure 2.3. Nevertheless, this gain drop will be compensated by the two $C_{tot}$-originated adjacent zeros with a +20 dB/dec increase in the slope. (Note that these zeros do not arise if $C_{tot} = 0$). As indicated by the red curve, when it encounters the two zeros at around 3.5 GHz, instead of quickly rolling off, it becomes flattened. The unexpected negative phase jump due to the RHP zero $z_2$ will also be cancelled out by the nearby LHP zero $z_1$, as illustrated in Figure 2.4. Thus, the total phase response of $G(s)$ will be predominately contributed by the poles of the passive network.

Equation (2.8) reveals that $C_c$, being the design-adjustable part of $C_{tot}$, can certainly increase the feedback at $2f_0$ through shifting the zero locations thus to alter the rolling-down slope of the gain response. Beyond that, $C_L$ can also influence the feedback at $2f_0$ through shifting the peak location of $G(s)$ adjusting the rolling-up slope of the gain response before it rolls down, which is manifested by Equations (2.5)–(2.7). As $C_c$ is fixed in this specific implementation, $C_L$ can be tuned to maintain the HD2 rejection when the carrier frequency of the DPA varies. Additionally, $-k_{mn} > 1$ and $C_{tot} \ll C_L$ in (2.8) and (2.5) suggests that the frequency of the gain peak will be lower than that of the zeros, $\omega_{pk} < |z_{1,2}|$. To the authors’ knowledge, this is the first thorough quantitative discussion about the effects of interwinding
2.2 Self-Suppression of HD2 in Power Amplifier

capacitance in a general transformer with operational loading and nonidealities [69] [70].

2.2.3 Quasi-Class-\textit{EF}$_{2,3}$ Switching PA

In comparison with current-source based PAs, the class-E derived switching PA has

distinguished itself in terms of high power efficiency due to the non-overlap between the
switch’s voltage and current waveforms. The disadvantage there, however, lies in the peak
drain voltage $V_D$ during the off-switch times which can be as high as 3.56 times the power
supply ($V_D \approx 3.56 \times V_{DD}$) [71]. In response, a hybrid of class-E with class-F or class-F$^{-1}$ was
reported to reduce the peak voltage to $\sim 2V_{DD}$ and to benefit from waveform shaping through
harmonic tuning [72]. As for the single-ended topology, the hybrid class-E/F PA (see the
definitions in [72]) does not show its superiority over class-EF, which cannot exploit the
differential-mode and common-mode impedances in a single load network to perform distinct
reactions under odd and even harmonic stimuli. A transformer-based power combining
network [$T_1$ in Figure 2.6(a)] can incorporate the RF choke $L_{RFC}$ and fundamental frequency
tuning $L_{tn}$ inductors of the conventional class-E network into the magnetic inductance $L_m$
at its primary coil. Meanwhile, $L_{add}$ can be absorbed into the leakage inductance $L_{leak}$ and $C_{tn}$
equivalently shifted to the secondary as $C_L$ [73]. Furthermore, the capacitor $C_s$ in parallel
with the switch is designed to resonate out at near the third harmonic frequency $3f_0$, taking
advantage of the other resonant tank inherently within $T_1$.

The transformer $T_1$ should also provide the required load impedance transformation of
$R_L$ to the switching devices as $r_L \approx (R_L + r_s) \cdot k_m^2 / n^2$ in order to optimally deliver a certain
desired amount of RF power. For a targeted $P_{out} \approx 12$ dBm under $V_{DD} = 0.85$ V, a step-up
transformer with turns-ratio $n > 1$ should be used to lower $r_L$. (Note that with no impedance
transformation, the maximum delivered power would only be $P_{out, max} = (V_{DD} - V_{knee})^2 / 2R_L \approx$
5.6 dBm with $V_{knee} = 0.1$ V.) By assuming a low-loss case ($r_p, r_s, r_{CL}, r_C \rightarrow 0$), two possible
resonant frequencies in a transformer were described in [68] [74] [75] as

$$\omega_{H/L}^2 \approx \frac{1 + \left( \frac{L_s C_L}{L_p C_s} \right) \pm \sqrt{1 + \left( \frac{L_s C_L}{L_p C_s} \right)^2 + \left( \frac{L_s C_L}{L_p C_s} \right) \left( 4k_m^2 - 2 \right)}}{2L_s C_L (1 - k_m^2)}$$ \quad (2.9)

where $\omega_H$ and $\omega_L$ represent the higher and lower resonance frequencies, respectively. Likewise,
we define $X$-factor as $X = \frac{L_s}{L_p} \cdot \frac{C_L}{C_s}$, thus the ratio of resonant frequencies $\omega_H / \omega_L$ can be
2.2 Self-Suppression of HD2 in Power Amplifier

easily obtained that is purely a function of $X$-factor and the coupling coefficient $k_m$. Given that the turns ratio $n = \sqrt{L_s/L_p}$ is initially decided by the targeted $P_{out}$, $X$-factor will be eventually a subject to the tuning capacitance ratio $C_L/C_s$. The influence of $X$-factor on $\omega_H/\omega_L$ and the matching network efficiency $\eta_M$ ($Q_p$ and $Q_s$ assumed to be 10) for various $k_m$ are both plotted in Figure 2.5. No solutions of $X$ can be found for $\omega_H/\omega_L = 3$ when $k_m > 0.8$ in order to realize a second impedance peak at the third harmonic. On the other hand, the matching network efficiency $\eta_M$ is positively correlated with $k_m$ and will reach its peak value for $1 \leq X \leq 2$ shown with the dashed lines. To preserve a relatively high efficiency, it is desirable to design $X$-factor within the region $1 \leq X \leq 2$ which corresponds to a coupling factor range $0.8 \geq k_m \geq 0.77$ in order to achieve the impedance peak at $3f_0$. In reality, the resonant frequencies of the tank $\omega_{H,L}$ will also be influenced by the series resistance $(r_p, r_s)$ of the two windings and the total interwinding capacitance $C_{tot}$, thus there could be a slight offset from the $X$-factor depicted in Figure 2.5 in order to meet $\omega_H/\omega_L = 3$ under certain $k_m$. The choice of $C_L$ follows a similar way as in [40], mainly to balance the effects of loaded $Q$-factor $(Q_L = R_LC_L\omega_0)$ on the matching network efficiency $\eta_M$ and the frequency selection. In this work, $T_1$ is designed as $L_s/L_p = n^2 \approx 7.5 \text{nH} / 5.5 \text{nH}$ with $k_m \approx 0.8$. The capacitance parameters are $C_L \approx 3.5 \text{pF}$ and $C_s \approx 2.8 \text{pF}$. Now, that the total interwinding capacitance $C_{tot} \approx 0.11C_s$ ($C_{tot} = C_c + C_{int} \approx 320 \text{fF}$) and $n \approx 1.2$ are both fairly small, it is acceptable

Figure 2.5: Ratio of tank resonance frequencies and efficiency versus $X$-factor for various $k_m$. 

![Figure 2.5: Ratio of tank resonance frequencies and efficiency versus X-factor for various k_m.](image)
2.2 Self-Suppression of HD2 in Power Amplifier

Figure 2.6: Transformer-based load transformation network: (a) incorporation of loading network of class-E into transformer [73]; (b) magnitude of the input impedance, $Z_{in}$; (c) drain voltage and switch current waveforms; (d) superimposed harmonics of the drain voltage.

to ignore the multiplicative equivalent capacitance subject to the Miller effect at the primary side of $T_1$. Consequently, we reach $X \approx 1.46$. Figure 2.6(b) illustrates the simulated $Z_{in}$ of the transformer-based load network seen by the common drains of the switching PA for the $X \approx 1.46$ value that satisfies the resonance frequency ratio $\omega_H/\omega_L = 2\pi f_H/2\pi f_L = 3$.

Moreover, the proposed $C_C$ manages to suppress the 2nd-harmonic both at the common drain and output, which effectively shunts the energy of 2nd-harmonic to ground. Following the nomenclature for class-EF in [72], where the load seen by the common drain of the switches is an open circuit at odd harmonics and a short circuit at even harmonics, we name the proposed switching PA as a *quasi*-class-EF$_{2,3}$ PA. As there is no real short circuit at the second harmonic, we term it "quasi". To evaluate the performance of the quasi-class-EF$_{2,3}$ PA, a comparison of waveform factors $F_V \equiv V_{pk}/V_{DC}$, $F_I \equiv I_{rms}/I_{DC}$ and $F_C = P_{out}/V_{DC}^2/Z_C$ [72] is made among various tuning strategies in Table 2.1. Smaller numbers indicate better performance.
Table 2.1: Waveform factors for various hybrids of class-E and class-F Amplifiers

<table>
<thead>
<tr>
<th></th>
<th>$F_V$</th>
<th>$F_I$</th>
<th>$F_C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>3.56</td>
<td>1.54</td>
<td>3.14</td>
</tr>
<tr>
<td>E/F$_2$</td>
<td>3.67</td>
<td>1.48</td>
<td>1.13</td>
</tr>
<tr>
<td>E/F$_3$</td>
<td>3.14</td>
<td>1.52</td>
<td>3.14</td>
</tr>
<tr>
<td>E/F$_{2,3}$</td>
<td>3.13</td>
<td>1.47</td>
<td>2.31</td>
</tr>
<tr>
<td>E/F$_{2,4}$</td>
<td>3.43</td>
<td>1.46</td>
<td>0.97</td>
</tr>
<tr>
<td>E/F$_{2,3,4}$</td>
<td>3.08</td>
<td>1.45</td>
<td>1.18</td>
</tr>
<tr>
<td>Quasi-EF$_{2,3}$</td>
<td>2.38</td>
<td>1.46</td>
<td>1.68</td>
</tr>
</tbody>
</table>

One advantage of the combined tuning of class-EF or class-E/F is to shape the waveforms to have lower peak voltage and rms current, such that it would not affect the transistor’s reliability. When larger number of harmonics are tuned, the waveforms will better resemble those in class-F or class-F$^{-1}$ which primarily determines the waveform factor $F_V \equiv V_{pk}/V_{DC}$. It is well known that for an ideal tuned class-F PA, the switch voltage waveform resembles a square wave with peak-to-peak value of $2V_{DD}$ compared to that of $3.56V_{DD}$ for the ‘pure’ class-E PA. Accordingly, the peak-to-peak voltage of its sinusoidal fundamental component is $\frac{\pi}{4} \cdot 2V_{DD} > 2V_{DD}$ for class-F operation. It can thus be estimated that $F_V$ for the ideally tuned class-EF is around 2 (DC normalized). The voltage and current waveforms are interchanged in class-F$^{-1}$ where the voltage waveform distinctly features a large swing or an overshoot. The expression of switching voltage of ideal class-F$^{-1}$ is deduced in [72] with a peak $\pi \cdot V_{DD}$, therefore the corresponding $F_V$ is roughly 3.14 after the DC normalization. Additionally, the lower HD2 component in the quasi-class-EF$_{2,3}$ PA contributes to decrease the voltage peak revealed in Figure 2.6 in contrast to that in class-E/F$_{2,3}$ whose load at second harmonic is tuned to be open circuit. As for $F_C = \frac{P_{out}}{V_{BB}^2/Z_C}$, $P_{out}$ can be calculated based on the above discussion. For class-F, we have $P_{out} \approx \frac{[(4/\pi) \cdot V_{DD}]^2}{2R}$ leading to an $F_C = (4/\pi)^2 = 1.62$ after normalizing the DC. Waveform factors $F_V = 2$ and $F_C = 1.62$ for a more ideal class-EF tuning are quite close to that of the proposed quasi-class-EF$_{2,3}$ PA which outperforms its class-E/F$_{2,3}$ counterpart. Intuitively, this is simply due to the fact that a square wave has lower peak-to-peak value compared to its fundamental sinusoidal component and the proposed
quasi-class-EF\textsubscript{2.3} PA tunes the second harmonic almost for free.

The simulated drain voltage and switch current waveforms are shown in Figure 2.6(c). The time on x-axis is normalized to the switching period, $T_{sw}$. $V_d$ is the superposition of $V_{DC}$, fundamental frequency voltage $v_{fund}$ and other higher-order harmonic components. When only considering the first three harmonics and ignoring higher orders, which are relatively small, $V_d$ is approximately decomposed into three sinusoidal waves with frequencies at the first three harmonics shown in Figure 2.6(d). It appears that the voltage peak of fundamental $V_{pk,fund}$ is reduced at the presence of third harmonic. Interestingly, the superimposed voltage $v_{sp} = V_{DC} + v_{fund} + v_{sec} + v_{thd}$ has its peak $V_{pk,sp}$ situated around the second harmonic peak $V_{pk,sec}$ which is at $1/4 \cdot T_{sw}$, thus indicating that HD2 will also play an important role in $V_{pk,sp}$.

The rejection of HD2 by means of adding the proposed $C_C$ could benefit the $F_V$ reduction up to 24%.

### 2.3 Pulling Mitigation of DCO by DPA

The ULP operation is paramount for IoT oscillators. The power drain of an RF oscillator is [40]:

$$P_{DC} = 2V_{DD}/R_p \cdot \alpha_v/\alpha_i,$$

so it calls for: low supply voltage $V_{DD}$, high parallel resistance $R_p$ of the tank, low voltage efficiency $\alpha_v$, and high current efficiency $\alpha_i$. However, $\alpha_v \alpha_i$ should be maximized to avoid penalty on FoM in that $\alpha_v$ should not be too low. A 0.3 V $V_{DD}$ is achieved by adopting a transformer feedback topology. Moreover, $R_p = L_p \omega_0 Q_t$ can be magnified through increasing the tank inductance and Q-factor. Multiple turns and large diameter are preferable for large inductors with high Q-factor, thus a transformer with 2:3 turns-ratio and 450 um inner radius is deployed in the 1.8GHz DCO, as shown in Figure 2.7. The tank’s $R_p \approx 1.5$ k$\Omega$ is reached with the primary winding inductance $L_p$ of 10 nH and Q of 12. The trade-off between $P_{DC}$ and die area due to the enlarged inductor is relieved by the proposed concentric octagon layout topology and by placing all other active devices vertically below the region of DCO’s inner diameter.

Compared to the conventional side-by-side (i.e., lateral) arrangement of the oscillator and PA, a stronger magnetic coupling that causes the DCO pulling by the DPA at near $2f_0$ can be expected in this compact topology. To keep the coupling factor $k_{m,A}$ reasonably low ($k_{m,A} \approx 0.16$ as per EMX simulations), a distance of 150 $\mu$m is reserved in between the outermost turn ($PI_1 - PI_2$) of the DPA transformer and the innermost turn ($S_1 - S_2$) of the
Figure 2.7: Schematic of the merged DPA-DCO with the proposed mitigation of injection pulling through magnetic coupling feedback.

DCO transformer depicted in Figure 2.8. To help it further, an extra small coil \((T_1 - T_2)\) is inserted between the two transformers to sense the coupling, and to send an amplified but inverted signal back to the DCO transformer. The compensating strength is controlled by a

Figure 2.8: Inductances and coupling factors of the concentrically laid-out transformers.
2.3 Pulling Mitigation of DCO by DPA

Figure 2.9: LC oscillator under injection pulling: (a) AM-FM conversion mechanism [77]. (b) Concept of pulling mitigation through magnetic coupling compensation.

$V_T$ bias such that the magnetic coupling at the 2nd harmonic between the DPA and DCO transformer windings can be cancelled by the 2nd harmonic injection into the DCO.

Notwithstanding the amount of HD2 already suppressed to a relatively small value through the proposed $C_C$ capacitor both at the common drain node and output nodes of the DPA, i.e., $PI_1$ and $SI_1$ in Figure 2.8, the remaining injection pulling still could be significant since even a weak injection strength can catastrophically impact the transmitter’s performance [76]. Note that the dominant coupling path lies in the magnetic coupling from $(PI_1 - PI_2)$ to $(S_1 - S_2)$ rather than that from $(SI_1 - SI_2)$ attributed to 5 dB higher HD2 power at the drain node as per simulations.

The scenario of a free-running LC oscillator under injection pulling is shown in Figure 2.9(a). The phasor $V_{tot}$ is the composite vector of the oscillator phasor, $V_{osc}$, and AM-modulated aggressor phasor, $V_{inj}$. In the absence of aggressor, $V_{tot}$ aligns with $V_{osc}$, i.e., $\phi$ is zero. Once the oscillator encounters the 2nd harmonic of the PA, either through a parasitic or magnetic coupling, there will be an additional phase shift (a non-zero $\phi$) between $V_{osc}$ and $V_{tot}$ which violates the Barkhausen criterion at $\omega_0$. This will shift the oscillation frequency lower to $\omega_{inj}$. Upon reaching the steady state, the oscillation frequency $\omega_{out} = \omega_{inj}$, indicating that $V_{osc}$, $V_{inj}$ and $V_{tot}$ rotate at the same rate with a constant angular displacement $\theta$ between $V_{osc}$ and $V_{inj}$. However, the phase shift $\phi$ will not be constant under the time-varying AM-FM conversion. A stronger injection $V'_{inj}$ will introduce a different phase shift $\phi'$. In [77], the DCO is exposed to a parasitic frequency modulation (FM) resulting from injection pulling of an amplitude modulated (AM) aggressor, mainly the 2nd harmonic at the DPA output. The solution was to delay the DPA clock to align it with the DCO phase for the lowest
aggressor-victim sensitivity.

To gain insight into the aforementioned mechanism, a general mathematical model of injection-pulled free-running oscillator described in [76]– [78] is retrospected:

\[
\omega_{out} = \omega_0 - \frac{\omega_0}{2 \cdot Q} \cdot \frac{V_{inj}}{V_{osc}} \cdot \sin \theta
\]

(2.10)

\[
\omega_{out} = \omega_0 + \omega_{pulling}
\]

(2.11)

where \(Q\) is the quality factor of the LC tank at undisturbed frequency \(\omega_0\), which may vary under an FM modulation, \(V_{osc}\) and \(V_{inj}\) are the fundamental amplitude of the oscillator signal and the envelope of the injection, respectively, with \(\theta\) as the instantaneous angle between them. Note that \(V_{inj}\) is also time-varying if the TX undergoes AM modulation. The expression \(\omega_{pulling}\) in (2.11) is equivalent to the second term in (2.10) representing the parasitic FM due to the AM-FM conversion. Previous approaches dedicated to reduce the AM-induced FM pulling can be mapped onto equation (2.10). For example, a digitally controlled delay (DCD) stage was inserted between the DCO and DPA in [77] to adjust the phase of \(\omega_{inj}\) such that its phase angle (\(\theta\)) related to \(\omega_{out}\) equals to zero or \(\pi\), which means the second term in (2.10) is close to zero.

The method proposed in this paper is distinct from the previous solutions and indicated in Figure 2.9(b). By virtue of the extra small coil \((T_1 - T_2)\) in Figure 2.7) between the two transformers, an accurate duplicate of the injection aggressor \(V_{inj}\) can be acquired across the terminals of the coil but with a scaling factor \(\xi\). Assuming the aggressor finds its way to the DCO through a coupling path represented by transfer function \(H(s)\), then \(\xi\) can be expressed as

\[
\xi = \frac{1}{H(s)} \cdot \frac{n_{PL,T}}{k_{m,3}}
\]

(2.12)

where \(n_{PL,T}/k_{m,3}\) is exactly the nonideal turns ratio between the \((T_1 - T_2)\) coil and the outermost turn of the DPA transformer \((PI_1 - PI_2)\) with \(n_{PL,T} = L_T/L_{PI} = 0.4 \text{nH/10nH}\) and \(k_{m,3} = 0.4\) at \(2f_0\). Under a scenario dominated by magnetic coupling, \(H(s) \approx n_{PLS}/k_{m,4}\), thus, \(\xi\) can be estimated as

\[
\xi \approx \frac{k_{m,4}}{k_{m,3}} \cdot \frac{n_{PL,T}}{n_{PLS}} \cdot \frac{L_T}{L_S}
\]

(2.13)
Figure 2.10: (a) Top level diagram of proposed DCO-DPA. (b) Simplified pulling mitigation concept between the DPA and DCO.

which is mainly determined by the ratio of two inductances. Even under process variation, $\xi$ is relatively stable. The duplicate signal $\xi \cdot V_{inj}$ is then amplified by $-A_V$ and sent back to the oscillator where it will cancel the aggressor $V_{inj}$. For simplicity, we re-write Equation (2.10) as: $\omega_{out} = \omega_0 + \mu \cdot V_{inj}$. After taking into account the parasitic injection, we have:

$$\omega_{out} = \omega_0 + \mu \cdot V_{inj} + \mu \cdot (-\xi \cdot A_V) \cdot V_{inj}$$  \hspace{1cm} (2.14)

The AM-PM injection pulling can be minimized when $\xi \cdot A_V = 1$. The amplification is realized with a simple common-source stage with a diode-connected load while the gain $-A_V$ is controllable through tuning the $V_T$ bias. Once $V_T$ is optimized for certain $V_{inj}$, it will hold for any complicated AM modulation scheme as $V_{T,opt}$ has no dependency on the injection strength.
2.4 Experimental Results

2.4.1 Proposed DCO-DPA for Sub-GHz IoT TX

A block diagram of the proposed merged DCO-DPA is depicted in Figure 2.10(a). The DCO provides the RF carrier clock and the DPA realizes the digital modulation of the carrier’s envelope. Instead of oscillating at the PA’s carrier frequency \( f_0 \) (i.e., \( \sim 0.9 \text{GHz} \)), the DCO tank’s Q-factor is optimized at \( 2f_0 \) followed a \( \div 2 \) divider for the purpose of smaller area and lower PN under same power budget [58]. A simple 8-bit single-ended quasi-class-\( EF_{2.3} \) DPA is adopted to maximize the efficiency. The concentric octagon layout topology is realized by placing the DPA matching-network transformer within the inner diameter of the DCO transformer. The HD2 emission at \( 2f_0 \) due to the nonlinearity of DPA switches can potentially injection-pull the DCO through magnetic coupling. The 256 amplitude steps of the DPA are achieved by two unit-weighted segments of 64 \( 4 \times \) and three \( 1 \times \) transistors [79]. In this way, the total number of the transistors in the PA array can be reduced from 256 to 64 + 3 = 67, which helps to alleviate the overall routing complexity. All other blocks shown in Figure 2.10(a) are also integrated on-chip.
2.4 Experimental Results

Figure 2.12: DPA output-port measurements: (a) DPA output power and efficiency; (b)(c) HD2 emission performance at $V_T = 0$V and $V_T = 0.3$V (i.e., compensating path turned off/on).

2.4.2 Measurement Results

The chip is fabricated in 16-nm FinFET CMOS, occupying 0.85 mm$^2$ in total, as shown in the die photo in Figure 2.11. The single-ended sub-GHz DPA achieves 51% total power... dBc/Hz
VDD : 0.3V , PDC : 195 uW

Figure 2.13: DCO output-port measurements: (a) DCO phase noise, (b)(c) DPA-induced (by 5 MHz AM) pulling mitigation performance with tunable $V_T$. 
2.4 Experimental Results

The measured phase noise of the 1.8 GHz DCO is plotted in Figure 2.13(a). At a 0.3 V supply, it reaches -116 dBc/Hz at 1 MHz offset from 1.8 GHz carrier while consuming 195 µW. The DCO covers a frequency tuning range from 1.1 to 2.1 GHz. The AM-induced injection pulling spurs are measured at the DCO output port when the DPA toggles all the switches at a $f_m = 5$ MHz rate. The measured $f_c \pm f_m$ spurs are reduced from -35 dBc at $V_T = 0$ V (no compensation) to -57 dBc at $V_T = 0.3$ V, which validates the proposed pulling mitigation method [Figure 2.13(b)]. Different injection strengths are inspected by controlling the power of the AM signal through the ACW controls of the DPA (only tuning the MSB codes here), it indicates that there is one universal optimum $V_T = 0.3$ V for various levels of AM signal power from -10 dBm to 11 dBm in order to suppress the AM-induced spurs. All these spurs
2.4 Experimental Results

![Figure 2.15: EVM versus output power with the compensating path turned off/on.](image)

are below -50 dBc, as shown in Figure 2.13(c). The extra power consumption of the DCO due to engaging of the pulling mitigation path is only 5 µW.

The measured modulation spectrum of a transmitted 2-MHz 64-QAM OFDM signal is shown in Figure 2.14. The IEEE 802.11ah standard defines the operating signal bandwidths from 1 MHz/2 MHz in mandatory modes up to 16 MHz in optional modes. The 20 MHz frequency range marked in Figure 2.12 is intended to show that the proposed HD2 suppression technique is not limited to the single channel frequency at 900 MHz but can work effectively over a relatively large range of channels and still have some margin for the component spread. We employ the same 2 MHz 64-QAM test signal as in the important benchmark reference [58] for fair and intuitive comparison with the prior art. The actual mode (bandwidth) selection is related to the data rates and application scenarios.

By engaging the pulling compensation path, the measured EVM improves to 3.5% at 0 dBm output power, which is a 12.5% improvement compared with the 4% EVM when \( V_T = 0 \) V. That not so strong-enough pulling is mainly due to the 150 µm distance reserved within the dominant coupling path between the outermost turn \( (PI_1 - PI_2) \) of the DPA transformer and the innermost turn \( (S_1 - S_2) \) of the DCO transformer. However, that relatively low coupling factor of 0.16 is still large enough to create significant coupling and modulation...
2.4 Experimental Results

distortion. With the help of pulling mitigation, EVM < 4% is maintained for output power levels of up to 5 dBm, as depicted in Figure 2.15. The abrupt EVM degradation is mainly caused by the non-linearity of the DPA which will produce systematic deviation of the constellation points from the ideal positions. In case of a more visible pulling effect when a 100-kHz 64-QAM signal at 5 dBm is measured, the EVM improves from 3.35% to 1.5% at 5 dBm RF output power through turning on the compensating path, as shown in Figure 2.16.

The DCO-DPA performance is summarized in Table 2.2 and favorably compares to state-of-the-art sub-GHz TXs. The presented concentrically laid-out DCO-DPA solution offers 3× area reduction compared to recent publication [62] with on-chip matching. The deep HD2 (<-55 dBc) rejection is achieved without resorting to complex circuitry or calibration and with insignificant increase in power consumption. Together with the magnetic coupling compensation of injection pulling, our design shows better EVM at 3× higher average RF power with OFDM modulation [58].

Figure 2.16: 100kHz 64-QAM modulation with 5 dBm output RF power at $V_T = 0$ V and $V_T = 0.3$ V (i.e., compensating path turned off/on).
### Table 2.2: Comparison with state-of-the-art sub-GHz TXs.

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a: TX efficiency; b: drain efficiency only; c: external matching needed; d: graphically estimated.

### 2.5 Conclusion

A compact merged DCO-DPA circuitry with a fully integrated matching network for a sub-GHz IoT transmitter is introduced in this chapter. It achieves the highest PA efficiency, thanks to its single-ended configuration, while maintaining sufficiently high HD2 suppression by means of the proposed feedback coupling cancellation (FBCC) capacitor. The lowest DCO power consumption and the smallest system area are achieved via the proposed concentric layout topology. The resulting coupling can be virtually eliminated by the proposed controllable DPA-to-DCO injection.
We propose a super-simple power-efficient sub-1V fully integrated RF front-end (RFE) for 2.4GHz transceivers. It introduces the following innovations: Firstly, function-reuse single-MOS DCO-PA with full supply utilization improves antenna-to-DCO isolation for better resilience to jammers. Secondly, a non-inverting TX matching transformer with a zero-shifting capacitor suppresses the 2nd harmonic emission of the DCO-PA, and allows a single-pin antenna interface for both TX and RX modes eliminating the T/R switches in the signal path. Thirdly, a push-pull LNA reuses the TX matching transformer for passive gain boosting that reduces power consumption. Fabricated in 65-nm CMOS, the RFE occupies merely 0.17mm\(^2\). Through the functional merge of the oscillator and PA, it can transmit 0 dBm at RF, featuring 10.2% power efficiency when delivering the RF power as low as -10 dBm at a 0.3 V supply. Under a 0.5 V supply, the LNA shows 11 dB gain and 6.8 dB noise figure (NF) while consuming 174 \(\mu\)W.
3.1 Introduction

Ultra-low-power (ULP) radios play a crucial role in the expansion of Internet-of-Things (IoT) connectivity where wireless sensors gather and exchange massive amount of data. In battery-operated low-data-rate, short-range sensor applications, such as temperature, humidity and pressure monitoring as well as health tracking, the major bottleneck lies in the battery life. Bluetooth low energy (BLE) is the key standard which has gained popularity not only due to its support for a lower duty-cycle operation but also for various low-power states allowing to reduce current consumption in line with the usage profile and application scenarios. Indeed, the BLE transmitters (TX) typically support programmable RF output power from -20 dBm to +4 dBm, as shown in Figure 3.1 for a few commercial chipsets. The TX comprises an RF power amplifier (PA) and a frequency synthesizer as major components, and dominates the total power consumption of the RF transceiver. Hence, there are intensive ongoing efforts on improving its efficiency, especially at deep power back-off levels.

Open-loop modulation has recently gained popularity in ULP transmitters thanks to its energy saving feature by shutting down the ADPLL loop after quickly acquiring the channel center frequency. Further improvements in substantially lowering of the DCO flicker noise help to bring the carrier frequency drift to well within the IoT specifications. Under the open-loop scenario, the conventional TX architectures can

![Figure 3.1: BLE SoCs with programmable RF power.](image-url)
be simplified as a convenient arrangement of a separate oscillator (e.g. VCO or DCO) and a PA [Figure 3.2(a)], which are the two most power-hungry blocks\(^1\). Generally, the oscillator runs at \(2\times\) PA carrier frequency to mitigate the potential injection pulling attributed to the parasitically coupled (but frequency modulated via the AM component) aggressor from the PA [88]. Consequently, this necessitates divider and buffer stages in cascade to drive the PA wherein the consumed power into the PA driving does not scale with the back-off of the TX output power. At the deep power back-off, where the power spent into the PA driving is comparable to the targeted RF power, the total TX efficiency will be heavily compromised. Even with state-of-the-art highly efficient solutions [40] [89], the total TX efficiency is restricted to 8\% at deep power back-off (-10dBm) even under an open-loop operation. The latest ring-oscillator based 4\(\times\) frequency edge combiner [84] remarkably reduces the power consumed to drive the PA while introducing significant compromise on its phase noise. Separate optimization of the PA, oscillator and other driving stages is not desirable in the low power regime.

A current-reuse PA-VCO stack [90] aims to optimize the VCO and PA as an indivisible entity [Figure 3.2(b)]. However, it is incompatible with the ultra-low voltage (ULV) operation and has a constrained output power due to the reduced voltage headroom. There is an inherent trade-off between the oscillator’s phase noise (PN) and total PA efficiency in terms of the supply division between these two. Instead of the current-reuse TX topology, the function-reuse DCO-PA firstly proposed in [91] seems more promising through assimilating the power consumption of the DCO into the DCO-PA with full \(V_{DD}\) utilization and breaking the aforementioned PN and efficiency trade-off with purely passive (transformer) optimization [Figure 3.2(c)]. Nevertheless, the six-port transformer which merges the oscillator resonance tank and the PA matching network (MN) would inevitably incur unfavorable mutual coupling between these two, as shown by a coupling factor \(k_3\) in Figure 3.3(a). Consequently, this class-F DCO-PA is extremely vulnerable to jammers appearing at the antenna. Additionally, the second impedance peak at the 3rd harmonic for higher efficiency of this class-F DCO-PA could inevitably require off-chip filtering of HD\(_3\).

To avoid the mutual coupling resulting from the forced coexistence of oscillation tank

\(^1\)The power-saving benefits of the open-loop modulation can be extended for quasi-open-loop modulation. An ADPLL for BLE in [87] features a mere 1kHz loop bandwidth so that almost all of its digital circuitry can operate in subthreshold, resulting in the DCO consuming 70\% of its 0.9mW power budget.
Figure 3.2: ULP TXs: (a) traditional, i.e. separate DCO and PA; (b) current-reuse PA-DCO stack; (c) function-reuse DCO-PA.

and impedance matching network in the shared six-port (i.e. three-winding) transformer of Figure 3.3(a), a single-MOS DCO-PA based on source-to-gate (S-to-G) transformer feedback oscillation is proposed in this chapter. It is depicted in Figure 3.3(b). The output matching transformer is simultaneously utilized as a single-pin antenna interface (T/R switch) for both TX and RX modes, while offering passive gain boosting to the push-pull LNA, hence saving extra power.

The rest of the chapter is as follows: Section 3.2 introduces the new single-MOS DCO-PA topology for ULP TX accompanied by the zero-shifting capacitor across the MN transformer windings to suppress the 2nd harmonic. The single-pin antenna interface and the passive gain-boosting push-pull LNA are investigated in Section 3.3. Section 3.4 reveals the top-level implementation of the prototype with experimental results. Section 3.5 wraps up the chapter with conclusions.
3.2 Single-MOS DCO-PA for ULP TX

The concept of implementing the oscillator and power amplifier (PA) using the same transistor and operating at the same frequency was initially introduced in [92], where the tuned power oscillator can be as energy efficient as the class-E PA. However, that scheme requires complicated phase correction to guarantee the \(-196^\circ\) feedback loop phase shift. A DCO-PA-LNA-TX/RX-switch co-designed block proposed in [93] delivers TX power by connecting the antenna to the sources of the cross-coupled transistors pair in the DCO which suffers from limited output power and injection pulling. Analogously, the impediment to the practical application of the class-F DCO-PA in [91] arises from the insufficient isolation between the antenna and the oscillator, which would make the carrier frequency rather sensitive to the interferers, as previously mentioned in Section 3.1. All the above techniques are at the expense of introducing additional trade-offs between system complexity, reliability and efficiency.

3.2.1 S-to-G Transformer-Feedback DCO-PA

The basic idea behind the DCO-PA architecture is to make the PA self-driven for the additional purpose of generating self-oscillation. Consequently, it can eliminate the need for a separate PA driving circuitry necessarily including an oscillator, divider and buffer, whose power consumption cannot easily scale when backing off the optimal PA power levels.

Figure 3.3: Function-reuse DCO-PA: (a) class-F DCO-PA based on six-port transformer in [91]; and (b) proposed DCO-PA.
This can benefit the overall TX efficiency, especially in the low power regime. To meet the Barkhasusen’s criteria for oscillation, a third coil \( L_3 \) is added to produce another 180° loop phase shift through the inverting coupling between \( L_3 \) and \( L_1 \) in [91] enabling the drain-to-gate (D-to-G) transformer feedback oscillation [Figure 3.3(a)]. The inescapable coupling between \( L_3 \) and \( L_2 \) characterized by \( k_3 \) will expose the resonance tank to the antenna leading to vulnerability to jammers or interferers. The D-to-G feedback oscillation is replaced here by an S-to-G feedback to enhance the antenna-to-DCO isolation, breaking the trade-off between system efficiency and jammer resilience performance [67].

The feedback mechanism of the S-to-G feedback oscillator is analogous to that in a Colpitts oscillator [94]. The capacitive divider in the Colpitts oscillator provides the required positive feedback, while the feedback in the proposed oscillator is given by the S-to-G feedback.
3.2 Single-MOS DCO-PA for ULP TX

transformer as shown in Figure 3.4(b). In the Colpitts case, a scaling factor \( n_{\text{Colp}} \) can be expressed as

\[
n_{\text{Colp}} = \frac{v_G}{v_S} = \frac{C_1 + C_2}{C_1} \tag{3.1}
\]

As for the S-to-G transformer feedback case being distinct from the DCO-only implementation in [94], a rather large device is commonly used in the PA in order to lower its power loss. Taking into account the device capacitance \( C_{gs} \), the scaling factor in the proposed DCO-PA is then described as

\[
n_{\text{DCO}PA} = \frac{v_G}{v_S} = k_1 \frac{n_1 - C_{gs} L_s \omega}{n_1 - 1} \tag{3.2}
\]

where \( n_1 = \sqrt{L_s/L_g} \) is the turns ratio of transformer \( T_1 \) and \( k_1 \) is the magnetic coupling factor. Therefore, with \( |Z_s| \) representing the tank impedance seen at source, the loop gain can be estimated

\[
A_{\text{loop}} \approx \frac{g_m |Z_s|}{1 + g_m |Z_s|} n_{\text{DCO}PA} \tag{3.3}
\]

indicating that a smaller turns ratio \( n_1 \) (a larger \( L_g/L_s \)) in the S-to-G transformer-feedback oscillator is preferred to enlarge \( n_{\text{DCO}PA} \), increase the \( A_{\text{loop}} \), boost \( v_g \) swing and to lower the phase noise. This is verified via simulation results shown in Figure 3.5(a), where \( L_g \) and \( L_s \) are the self-inductances of the primary and secondary coils of \( T_1 \), respectively. In the simulations, \( L_g \) is kept constant with an assumed value of 2 nH while \( k_1 = 1 \) is chosen for simplicity.

Neglecting the series resistance inherent with the transformer coils, the input impedance \( z_{\text{in}} \) at the gate of \( M_{1,PA} \) without \( C_1 \) [Figure 3.4(a)] is given by the long formula (3.4), where \( M = k_1 \sqrt{L_g L_s} \) represents the mutual inductance between the two coils. The imaginary part of \( z_{\text{in}} \) will resonate with \( C_1 \) at the targeted frequency and the negative real impedance part happens to be beneficial in compensating for the LC tank losses. Since the 2nd-resonance of

\[
z_{\text{in}} = \frac{(L_g L_s - M^2)(C_{gs} + C_2)s^3 + g_m (L_g L_s - M^2)s^2 + L_g s}{(L_g L_s - M^2)C_{gs} C_2 s^4 + (C_{gs} L_g + (C_{gs} + C_2)L_s - 2MC_{gs})s^2 + g_m (L_s - M)s + 1} \tag{3.4}
\]
$T_1$ is designed at 3× of the oscillating frequency to suppress the 3rd-harmonic current, as will be detailed later, the effect from $C_2$ is relatively small and is further ignored to obtain a simplified expression of $z_{in}$:

$$z_{in} \approx \frac{C_{gs} \left( L_g L_s - M^2 \right) s^3 + g_m \left( L_g L_s - M^2 \right) s^2 + L_g s}{C_{gs} \left( L_g + L_s - 2M \right) s^2 + g_m \left( L_s - M \right) s + 1}$$ (3.5)

It is therefore straightforward to obtain the real part of the impedance $z_{in}$ after some simple manipulations,

$$z_{in,\text{real}} \approx \frac{g_m L_g L_s \omega^2 k_1^2 \left( 1 - \frac{1}{k_1} \frac{1}{n_1} \right) \left[ 1 - C_{gs} L_s \omega^2 \left( \frac{1}{k_1} - k_1 \right) \frac{1}{n_1} \right]}{\left( 1 - C_{gs} L_s \omega^2 \left( \frac{1}{n_1^2} - \frac{2 k_1}{n_1} + 1 \right) \right)^2 + g_m^2 L_s^2 \omega^2 \left( 1 - \frac{k_1}{n_1} \right)^2}$$ (3.6)

Obviously, $0 < k_1 < 1$, so, $\frac{1}{k_1} - k_1 > 0$. Furthermore, $C_{gs}$ is generally on the order of few hundreds of femtofarad with $L_s$ at the level of nanohenry. Hence, we can presume that the square-bracketed factor in the numerator of (3.6) is positive, i.e., $\left[ 1 - C_{gs} L_s \omega^2 \left( \frac{1}{k_1} - k_1 \right) \frac{1}{n_1} \right] > 0$. In order to provide the negative real impedance to compensate for the losses of the LC resonant tank, $\frac{1}{n_1} > 1 \rightarrow L_g > L_s$ is favored, which also coincides with the conditions for lower phase noise. The simulated real part of the input impedance $z_{in}$ across $L_g/L_s$ is plotted in Figure 3.5(b). From equations (3.2) and (3.6), it is apparent that the presence of $C_{gs}$ would have a negative effect of decreasing $n_{DCOPA}$ and $|z_{in,\text{real}}|$. Moreover, when the influence of $C_{gs}$ is further disregarded, $z_{in}$ proves out to be exactly same as the expression given in reference [94]. The phase noise equation for the generated waveform can be straightforwardly obtained from equation (39) in [95].

The PA is realized by transferring the power of drain oscillation waveform to the antenna with an appropriate impedance transformation ratio provided by transformer $T_2$ in Figure 3.4(a). The overall PA efficiency is composed by two parts

$$\eta_{PA} = \eta_{PA,T} \cdot \eta_{MN}$$ (3.7)

wherein $\eta_{PA,T}$ indicates the PA efficiency considering only the loss from the lone power transistor. Correspondingly, the efficiency of the matching network is labeled as $\eta_{MN}$. An intuitive way to lower the transistor’s dissipation, thus improving $\eta_{PA,T}$, is to reduce the fraction of a cycle over which the drain voltage and drain current waveforms of the single-MOS
3.2 Single-MOS DCO-PA for ULP TX

Figure 3.5: Simulation results of the proposed DCO-PA: (a) PN, efficiency and (b) input impedance vs. inductance ratio; (c) voltage swing and (d) PN, efficiency vs. coupling factor.

$M_{1,\text{PA}}$ in Figure 3.4(a) are simultaneously nonzero through properly arranging the gate bias $V_{GB}$. The mathematical expression for $\eta_{\text{PA,T}}$ as a function of the total conduction angle $2\phi$ described in [66] is retrospected with first assuming a cosine drain current

$$i_D = I_{DC} + I_{RF} \cos \omega_0 t, \quad i_D > 0$$

(3.8)

and then $\phi = \omega_0 t$ can be solved by setting the current $i_D$ to zero:

$$\phi = \cos^{-1}\left(-\frac{I_{DC}}{I_{RF}}\right)$$

(3.9)

The average drain current $\overline{I_{DC}}$ from the supply is evaluated by integrating $i_D$ over the
conduction interval $2\phi$ and substituting with the expression for $I_{DC}$ in (3.9) which yields

$$I_{DC} = \frac{I_{RF}}{\pi} (\sin \phi - \phi \cos \phi) \quad (3.10)$$

To gain insight into the power delivered to the load $R_d$ seen at the drain, as well as into the PA efficiency, the fundamental coefficient $I_{h1}$ for the fundamental current $i_{H1}$ in the Fourier
expansion of \( i_D \) is determined by the integral below:

\[
I_{h1} = \frac{2}{2\pi} \int_0^{2\pi} i_D(\phi) \cos \phi \, d\phi = \frac{I_{RF}}{2\pi} (2\phi - \sin 2\phi) \tag{3.11}
\]

In a similar way, we can get the coefficient \( I_{h3} \) for the third harmonic current \( i_{H3} \):

\[
I_{h3} = \frac{I_{RF}}{12\pi} (2 \sin 2\phi - \sin 4\phi) \tag{3.12}
\]

The \( L_s \) inductive degeneration would have a detrimental effect on \( \eta_{PA,T} \) since it consumes the output swing of \( M_{1,PA} \) in the presence of \( v_S(t) \) voltage across its source node [96]. Moreover, \( C_2 \) is added in parallel with \( L_s \) to produce a high impedance at \( 3\omega_0 \), thus obstructing the 3rd harmonic current. To understand this better and to obtain a mathematical expression for \( v_S(t) \), the \( L_sC_2 \) tank at source node is redrawn in Figure 3.6 with corresponding phasor diagrams representing the voltage and current waveforms at different harmonic frequencies. It is noteworthy that the two possible modes of oscillation in our two-port transformer-based resonator happen at two frequencies, same to that in the one-port case [97], which under a high-\( Q \) assumption can be expressed as

\[
\omega_{H,L}^2 = \frac{1 + X \pm \sqrt{(1 - X)^2 + 4k_1^2X}}{2(1 - k_1^2)} \omega_1^2 \tag{3.13}
\]

where \( \omega_1^2 = (L_gC_1)^{-1} \), \( \omega_2^2 = (L_sC_2)^{-1} \), and \( X = (\omega_1/\omega_2)^2 \). To find the \( X \)-factor that can secure the second impedance peak at \( 3\omega_0 \), the frequency ratio between the high and low oscillation modes \( \omega_H/\omega_L \) as a function of \( X \)-factor is plotted in Figure 3.6(b). The \( X \)-factor reaches the desired value of 3 at two points for the coupling factor \( k_1 < 0.8 \). A moderate \( k_1 \) with small \( X = L_sC_2/L_gC_1 \) is expected to mitigate the efficiency impairment caused by \( L_s \). It thus offers a good estimation of the high resonant frequency in (3.13) to be \( \omega_H \approx \omega_2/\sqrt{1 - k_1^2} = 1/\sqrt{(1 - k_1^2)L_sC_2} \) revealing that the effective inductance at the source is \( L_{se} \approx (1 - k_1^2) L_s \). For a certain amount of drain current \( i_D \), there would be a portion of \( i_{C_{gs}} = i_D \cdot j\omega C_{gs}/g_m \) flowing through the parasitic path owing to \( C_{gs} \) [98]. To maintain the same \( v_S(t) \) at the source, this is equivalent to adding another LC tank in parallel to the \( L_sC_2 \).
tank with a scaling $j\omega C_{gs}/g_m$, such that the total admittance seeing into the tank is

$$Y_{t,1} = \left(1 + \frac{j\omega C_{gs}}{g_m}\right) \left(\frac{1}{j\omega L_{se}} + j\omega C_2 + \frac{1}{R_p}\right)$$  \hspace{1cm} (3.14)$$

where $R_p \approx \omega L_s Q_{Ls}$ dominates the tank losses.

At fundamental frequency $\omega_0$, the fundamental current $i_{H1} = I_{h1} \cos(\omega_0 t)$ with an initial phase of zero would split into three parts, $i_{R_1}$, $i_{Ls}$ and $i_{C2}$, flowing through the equivalent RLC components in Figure 3.6(a), respectively. Thereinto, $v_{S,1}$ is marked out to be the reference as it is common to all the three branches. Correspondingly, the current signal $i_{R_1}$ is in-phase to the reference $v_{S,1}$ while the signals $i_{Ls}$ and $i_{C2}$ are $\pi/2$ behind and $\pi/2$ ahead of $v_{S,1}$, which are all sketched as the black arrow lines in Figure 3.6(c). In view that there is a phase difference of $\pi$ between $i_{Ls}$ and $i_{C2}$, the fundamental current $i_{H1}$, which is equivalent to the phasor addition of these three branch currents, can be obtained by applying the parallelogram law and drawing the diagonal line between $i_{Ls} - i_{C2}$ and $i_{R1}$. Due to the fact that the $L_sC_2$ tank resonates at $3\omega_0$, the inductive susceptance would dominate the tank at $\omega_0$ ($1/j\omega_0 L_{se} \gg j\omega_0 C_2$) causing the lagging effect of $i_{H1}$ with respect to $v_{S,1}$. The total tank admittance $Y_{t,1}$ at $\omega_0$ can be simplified as

$$Y_{t,1} \approx \left(\frac{1}{g_m L_{se}/C_{gs}} + \frac{1}{R_p}\right) + \frac{1}{j\omega_0 L_{se}} + \frac{j\omega_0}{g_m R_p/C_{gs}}$$  \hspace{1cm} (3.15)$$

Under the circumstance $g_m/C_{gs} \approx \omega_T \gg \omega_0$ and assuming $\omega_T = \alpha\omega_0$, $Y_{t,1}$ can be further simplified

$$Y_{t,1} \approx \frac{1}{\omega_0 L_s} \left(\frac{1}{\alpha (1 - k_1^2)} + \frac{1}{Q_{Ls}}\right) + \frac{1}{j\omega_0 L_{se}}$$  \hspace{1cm} (3.16)$$

Consequently, the equivalent parallel resistance $R$ of the tank at $\omega_0$ in Figure 3.6(a) can be obtained as $R_1 = \omega_0 L_s \cdot \alpha \left(1 - k_1^2\right) Q_{Ls} / \left(\alpha \left(1 - k_1^2\right) + Q_{Ls}\right)$ which is crucial for determining the swing at the source node. The angle $\theta$ between the resultant signal $i_{H1}$ and the reference $v_{S,1}$ is given by

$$\theta = \tan^{-1} \frac{B_{Ls} - B_{C2}}{G} = \tan^{-1} \frac{1/\omega_0 L_{se} - \omega_0 C_2}{1/R_1}$$  \hspace{1cm} (3.17)$$

where $G$ is the relevant conductance of $R_1$. $B_{Ls}$ and $B_{C2}$ stand for the corresponding susceptances.
3.2 Single-MOS DCO-PA for ULP TX

Figure 3.7: S-to-G feedback transformer: (a) Layout pattern; and (b) $L_g$ and $L_s$ Q-factors.

At third-harmonic frequency $3\omega_0$ where the resonance happens, the inductance and capacitance would cancel out each other leaving the tank purely resistive with $R_3 \approx 3\omega_0 L_s Q_{Ls}$ which is annotated in Figure 3.6(a) as the purple current $i_{H3}$ circulating through the $R$ path only. The corresponding voltage signal $v_{S,3}$ is identically in-phase with $i_{H3}$, with zero initial phase shown in Figure 3.6(c). In addition to the high-$Q$ tank at the output filtering the third harmonic, the fairly high impedance peak $R_3 \approx 3\omega_0 L_s Q_{Ls}$ at the source would lift up the knee voltage, thus limiting the swing of third-harmonic component at the output.

It is then straightforward to indicate that the signal $v_{S,1} = V_{s,1} \cos (\omega_0 t + \theta)$ has an amplitude $V_{s,1} = I_{h1} \cos \theta \cdot R_1$ with $0 < \theta < \pi/2$ due to $B_{Ls} > B_{C2}$. Likewise, the third harmonic signal can be expressed as $v_{S,3}(t) = V_{s,3} \cos (3\omega_0 t)$ with amplitude $V_{s,3} = I_{h3} \cdot R_3$. So far, we have not involved a discussion on second harmonic nonlinearity, but it will be pointed out in the next section that the HD$_2$ component at the output matching network is suppressed through the introduced zero-shifting capacitor $C_z$. Without considering even higher-order harmonics, the source voltage is the superposition of its fundamental and third harmonics, $v_S(t) = V_{s,1} \cos (\omega_0 t + \theta) + V_{s,3} \cos (3\omega_0 t)$. When the drain current $i_{H1}(t)$ attains its peak, the source voltage in the direction of $i_{H1}(t)$ is of interest which can be written as $V_{s,in} = V_{s,1} \cos \theta + V_{s,3}$.

Assuming $M_{1,PA}$ behaves all the time as a current source, the output voltage will reach its maximum swing $V_d = |−I_{h1} \cdot R_d|$. The negative sign means the current flowing into the load
3.2 Single-MOS DCO-PA for ULP TX

is inverse to the drain current. Taking into account the effect of \( V_{s,in} \), the maximum swing

\[
V_d = I_{h1} \cdot R_d \approx V_{DD} - V_{s,in}
\] (3.19)

From equations (3.10) and (3.11), it is easy to solve for the average DC current \( I_{DC} \) in terms of \( I_{h1} \),

\[
I_{DC} = 2 \cdot \frac{\sin \phi - \phi \cos \phi}{2\phi - \sin 2\phi} \cdot I_{h1}
\] (3.20)

Substituting the expression for \( V_{DD} \) from (3.19), the DC power consumption can be derived as

\[
P_{DC} = 2 \cdot \frac{\sin \phi - \phi \cos \phi}{2\phi - \sin 2\phi} \cdot I_{h1}^2 \cdot \left( \cos^2 \theta R_1 + \beta R_3 + R_d \right)
\] (3.21)

where \( \beta \) is defined as the ratio between \( I_{h3} \) and \( I_{h1} \) in (3.12) and (3.11). Together with the RF power delivered to the load,

\[
P_{RF} = \frac{1}{2} \cdot I_{h1}^2 \cdot R_d
\] (3.22)

the transistor efficiency \( \eta_{PA,T} \) can be readily calculated from the long formula (3.18), wherein the third factor stands for the efficiency drop in the presence of the LC tank at the source and the MOS non-linearity. When \( L_s \to 0 \), the third factor would vanish to one, leaving \( \eta_{PA,T} \) to be exactly same as that of the class-C power amplifier.

Intuitively, the denominator of the third fraction in (3.18) defines the equivalent resistive loss owing to \( L_s \) in the “direction” of the drain load \( R_d \), although the “direction” comes from the phase difference between the aforementioned two signals \( i_R, i_{H3} \) to \( i_{H1} \). Under numerical boundaries, when \( \theta \to 0 \), the “anti-phase” resistive loss reaches its maximum, raising up the knee voltage and bringing down the efficiency. At the other extreme of \( \theta \to \pi/2 \), the \( L_s \) induced loss reaches its minimum. The anticipated load resistance \( R_p \) is realized through the impedance transformation provided by transformer \( T_2 \) upon the amount of RF output power

\[
\eta_{PA,T} = \frac{1}{4} \cdot \frac{2\phi - \sin 2\phi}{\sin \phi - \phi \cos \phi} \cdot \frac{1}{1 + \left( \frac{1 - \frac{Q_{Ls}}{a(1-k_l^2)}}{\frac{1}{1+\frac{Q_{Ls}}{a(1-k_l^2)}} \cdot \cos^2 \theta + \frac{1+2\sin 2\phi - \sin 4\phi}{2\phi-\sin 2\phi} \cdot \frac{\omega_0 L_s Q_{Ls}}{R_d} } \right)}
\] (3.18)
targeted. Assuming a quality factor $Q_L = 10$ applies for all the windings in $T_1$ and $T_2$ in the DCO-PA circuit using a simple, but parameterized, transformer model, the maximum swing we can reach under the 0.7 V supply is $V_d \approx 0.6$ V, thus $R_d \approx \frac{1}{2} \frac{V_d^2}{P_{RF}} = 180$ Ω indicating that the step-down transformer $T_2$ should have a turns ratio $n_2 \approx \sqrt{R_L/R_d} \approx 1/2$ with $R_L = 50$ Ω representing the antenna.

![Figure 3.8: $\eta_{PA,T}$ given in (3.18) by substituting the design parameters.](image)

Furthermore, to assure the feasibility of $T_1$ physical implementation, $L_s \approx 0.2$ nH is chosen in this design to minimize its negative impact. The exact amount of inductance seen at $M_{1,PA}$ source would also be affected by the coupling factor $k_1$ between the $L_g$ and $L_s$ coils. Under a relatively large $L_g/L_s = 10$, the effects of different $k_1$ on the output swing $v_D$, fundamental voltage peak at source $V_s$, phase noise $L\left(\Delta\omega\right)$ and DCO-PA efficiency $\eta_{PA}$ are exhibited in Figs. 3.5(c)–(d). Conspicuously, there is a comparatively great compromise between the total efficiency of the proposed single-MOS DCO-PA and its phase noise at a moderate coupling factor $k_1 \approx 0.5$. The corresponding time-domain node voltages and current waveforms are shown in Figs. 3.6(d). As previously discussed, $C_2 \approx 2.4$ pF is adopted to induce the expected impedance peak at $3\omega_0$. The physical layout pattern of $T_1$ with a coupling factor $k_1 = 0.52$ is
revealed in Figure 3.7(a). It consists of a series-wound 3 turns on top-metal (M9) as $L_g$ and a parallel stack of 2 innermost turns of AP and M9 as $L_s$. By virtue of simply overlaying the AP layer, this contributes to diminishing the $L_s$ inductance by 20 pH while increasing its quality factor $Q_{Ls}$ by 1. The resultant inductances, $L_g \approx 2 \text{nH}$ and $L_s \approx 220 \text{pH}$, are confirmed by EM simulations with their quality factors plotted in Figure 3.7(b). In addition, $T_1$ exhibits a self-resonant frequency (SRF) of roughly 12 GHz. By substituting the design parameters into (3.18), $\eta_{PA,T}$ is compared in Figure 3.8 to the efficiency of an ideal class-C suggesting the influence of source degeneration with near 30% efficiency drop at low conduction angles. It also reveals a near 10% efficiency difference between the two numerical boundaries of $\theta$. Additionally, the total conduction angle $2\phi$ strongly depends on the gate bias $V_{GB}$ and there is generally a trade-off between the width of RF current pulse and efficiency. At $2\phi \approx 150^\circ$, $\eta_{PA,T}$ in (3.18) reaches its peak, as shown in Figure 3.8.

Remarkably, in contrast with the conventional PAs which might exhibit stability issues, there is no such concern here as the gate and source nodes of the single-MOS $M_{1,PA}$ in this DCO-PA are actually resonating as intended.

### 3.2.2 HD$_2$ Suppression through Zero-Shifting Capacitor $C_z$

Transfer function behavior of a general transformer-based matching network (MN) for a PA has been discussed comprehensively in [99], including the effects of inter-winding capacitance $C_{tot}$. Similarly, by means of neglecting the frequency response below the first pole $\omega_p = r_d/L_d$ in $T_2$, established mainly by $L_d$ and its equivalent series resistance $r_d$ [68], the voltage gain transfer function $G(s)$ can be simplified as a second-order system:

$$G(s) \approx \frac{L_o C_{tot}(1-k_d^2)s^2 + L_o C_{tot} \omega \left( \frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}} \right) s + \frac{M_{T2}}{L_d}}{L_o C_{o}(1-k_d^2)s^2 + L_o \left[ C_{o} \omega \left( \frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}} \right) + \frac{1-k_d^2}{R_L} \right] s + 1}$$

(3.23)

where $C_{tot} = C_{int} + C_z$ implying the total effective inter-winding capacitance $C_{tot}$ is composed of the intrinsic inter-winding capacitance $C_{int}$ and the artificially added zero-shifting capacitor $C_z$ across the primary and secondary coils of $T_2$. Although the MN together with $C_z$ looks superficially similar as that in [99], the working principle and system response are essentially different, primarily owing to the fact that the $T_2$ transformer in this implementation is in the non-inverting configuration (i.e., $M_{T2} > 0$). After the numerator’s second-order polynomial
is rearranged into a more standard form $N(s) = s^2 + 2\xi_n\omega_n s + \omega_n^2$, it is straightforward to derive the corner-frequency damping factor $\xi_n$ and the corner-frequency $\omega_n$ of $N(s)$:

$$\xi_n = \frac{1}{2} \omega \left( \frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}} \right) \sqrt{\frac{L_o C_{tot}}{n_2 k_2 (1 - k_2^2)}} \quad (3.24)$$

$$\omega_n = \sqrt{\frac{k_2 n_2}{L_o C_{tot} (1 - k_2^2)}} = \sqrt{\frac{k_2}{\sqrt{L_o L_d C_{tot} (1 - k_2^2)}}} \quad (3.25)$$
In this form, the quadratic formula gives the zero locations as

\[ s = -\xi_n\omega_n \pm \omega_n\sqrt{\xi_n^2 - 1} \]  

(3.26)

With \( \xi_n \approx 0.05 \) in this design falling into the interval \( 0 < \xi_n < 1 \), we can expect that the numerator polynomial \( N(s) \) will exhibit one complex-conjugate zero pair. Furthermore, when damping factor \( \xi_n \) satisfies \( 0 < \xi < 1/\sqrt{2} \), the amplitude-frequency response of \( N(s) \) unveils a valley (i.e., minimum value) at frequency \( \omega_v = \omega_n\sqrt{1 - 2\xi^2} \) whose depth is bound up with its damping factor \( \xi \). The amplitude of this valley is given by

\[ |H(j\omega_v)| = \frac{1}{2\xi\sqrt{1 - \xi^2}} \rightarrow -20\log \left( 2\xi\sqrt{1 - \xi^2} \right) [dB] \]  

(3.27)

Under the case \( \xi_n \approx 0.05 \ll 1 \), the valley is located roughly at \( \omega_v \approx \omega_n \) with approximate 20 dB roll-off. Recalling that \( C_z \) is the design-adjustable part of \( C_{tot} \), (3.25) can certainly be optimised to shift the valley location to \( \omega_v = 2\pi f_0 \), thus suppressing the second-harmonic component. Following a similar fashion, the damping factor \( \xi_d \) for the denominator’s second-order polynomial can be derived as

\[ \xi_d = \frac{1}{2} \left( \sqrt{\frac{L_oC_o}{1-k_2^2}} \omega \left( \frac{1}{Q_{L_d}} + \frac{1}{Q_{L_o}} \right) + \frac{1}{R_L} \sqrt{\frac{L_o}{C_o}(1-k_2^2)} \right) \]  

(3.28)

By substituting into the same design parameters, we can thus achieve \( \xi_d \approx 0.3 \), indicating that \( G(s) \) involves one complex-conjugate pole pair with a corner frequency

\[ \omega_{n,d} = \sqrt{\frac{1}{L_oC_o(1-k_2^2)}} \]  

(3.29)

All of the main conclusions on the complex-conjugate zero pair would pertain to the complex-conjugate pole pair apart from its amplitude-frequency response being merely a mirror image to that of the complex zeros. The initiated peaking effect resides at \( \omega_{pk} \approx \omega_{n,d} \approx 4.1 \) GHz with a peak amplitude of around 5 dB calculated by substituting \( \xi_d \approx 0.3 \) into (3.27). The formulas (3.23)–(3.29) form a good guideline to the frequency response of the \( T_2 \) matching network with respect to the locations and amplitudes of the peak and valley originated by the zeros and poles in the system. Circuit-level simulation results in Figure 3.9(a) verify a total of 26 dB rejection at \( 2f_0 = 4.8 \) GHz at a cost of sub-1 dB in passband loss. The proposed
HD\textsubscript{2} suppression technique is fairly well contained under the expected capacitance variations, as depicted with a zoom-in plot embedded in Figure 3.9(a). Instead of making $C_z$ tunable, for the sake of maintaining the high-$Q$ factor, it is viable to retain the HD\textsubscript{2} suppression under PVT variations [Figure 3.9(b)] through tuning the $C_o$, which indirectly alters the valley location and depth of the system response by adapting the peaking effect at $\omega_{n,d}$ (3.29), and regulating the $V_{GB}$ which partly compensates for the $M_{1,PA}$ threshold voltage variation. The peaking effect in Figure 3.9(a) originates from the conjugate poles of the transformer-based passive matching network, where there is no feedback path with enough phase shift to incur any instability issue.

Note that the complex-conjugate zero pair does not arise in the absence of inter-winding capacitance ($C_{tot} = 0$). Practically, it will be located at a fairly high frequency limited only by the intrinsic inter-winding capacitance $C_{int}$ from the $T_2$ transformer. More intuitively, we name $C_z$ as the zero-shifting capacitor, as it actually shifts the valley frequency $\omega_v$, which is extremely close to the corner frequency $\omega_n$ of the complex zero pair when the damping factor $\xi_n$ is small. Detailed discussion about the visible zero-notch in a general non-inverting transformer with operational loading was first presented in [69] [100] [101].

The proposed harmonic suppression technique is merely for the sake of HD\textsubscript{2} component rejection to satisfy the FCC requirement on spurious emission ($<-41.5$ dBm), not for the purpose of boosting the PA efficiency through different harmonic termination in class- F/F\textsuperscript{-1} PA. Moreover, the harmonically tuned PAs generally feature high peak voltages or currents, that could seriously stress the MOS devices, threatening the MOS reliability. Especially, tuning the second harmonic tends to increase the peak voltage [72]. Unlike the harmonically tuned PAs, the class-C PA can achieve high efficiency by means of lowering the conduction angle during one signal period.

### 3.3 Single-Pin Antenna Interface

#### 3.3.1 Re-using the TX Matching Transformer for the T/R Switching

Single-pin direct antenna connection with fully integrated T/R switches is highly desired in ULP radios in order to maximally reduce the system cost [63]. Conventional integrated T/R switches utilize series-shunt physical switch pair (carrying RF signals) in both the TX
and RX modes to connect to the antenna. This incurs high insertion loss and insufficient isolation, which has been discussed thoroughly in [70]. There have been continuous efforts to merge the RX mode switches into the input matching network of the LNA for high TX power tolerance and strong RX isolation through proper high-\(Q\) resonant tank design [103] [104] [105]. In a similar manner, the explicit series-shunt switches can be further eliminated [63]. All those solutions are at a cost of introducing additional LC tanks on top of the TX MN and involving complex programmable capacitor banks to assist with the mode switching. It would be preferable for the T/R switching to be accomplished by re-using the TX MN without resorting to the extra on-chip inductors/transformers, thus switching only the minimum
As formerly discussed in Section 3.2, in the transmitter (TX) mode, a step-down transformer is chosen to augment the equivalent impedance seen at the drain of DCO-PA in order to ensure a lower RF power transfer to the antenna. On the other hand, provided that the same antenna can be reused in the receiver (RX) mode, the RF signal from the antenna will then come across a step-up transformer with a passive gain boosting. This is precisely the scenario of time-division duplex (TDD) systems where TX and RX paths share an antenna while operating in the same frequency band [70]. By virtue of the proposed single-MOS DCO-PA topology with the fully integrated solutions handling the spurious emissions, the single-pin antenna interface not only eliminates any physical transmit/receive (T/R) switch in the signal path (by using purely DC power switches) [102] but can also manage to share
the same natural LC resonance of the transformer for the RF frequency selection in both TX and RX modes such that only one tunable capacitor ($C_o$) is required to fulfill the mode switching.

To take full advantage of the passive gain-boosting while preserving good linearity [105] at low power consumption, a push-pull topology is exploited for the LNA in the RX mode, as shown in Figure 3.10. When the DC supply switch $M_{TX}$ of Figure 3.12 is toggled to ground in Figure 3.11(a), the single-MOS $M_{1,PA}$ in the TX mode is completely cut off, turning itself into a mere capacitive load to the RX LNA symbolized by $C_{p,TX}$ in the circuit model in Figure 3.10(b). This can be compensated by altering $C_o$ (3-bit switched capacitor bank) to a lower code thus retaining good frequency selectivity of $T_2$-based MN at 2.4 GHz, which facilitates a more independent optimization of the TX-mode DCO-PA and RX-mode LNA. Likewise, in the TX mode, the parasitic capacitance of the RX input, which is rather small.
### Table 3.1: Comparison with state-of-the-art Integrated T/R Switches.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>SW Topology</th>
<th>IL (TX / RX) (dB)</th>
<th>Isolation (TX / RX) (dB)</th>
<th>Number of Ind. / Switchable Cap.</th>
<th>Fully-integrated RFIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>[103] 90nm</td>
<td>2.4</td>
<td>series-shunt switches with resonance</td>
<td>0.4 / 0.2</td>
<td>30 / 16</td>
<td>5 / 1</td>
<td>No</td>
</tr>
<tr>
<td>[105] 32nm</td>
<td>2.4</td>
<td>series-shunt switches with resonance</td>
<td>1.3 / 1.1</td>
<td>32 / -</td>
<td>&gt;3 / 1</td>
<td>No</td>
</tr>
<tr>
<td>[104] 65nm</td>
<td>2.4</td>
<td>series-shunt switches with resonance</td>
<td>- / -</td>
<td>- / -</td>
<td>4 / 5</td>
<td>Yes</td>
</tr>
<tr>
<td>[63] 28nm</td>
<td>2.4</td>
<td>soft switches * with resonance</td>
<td>- / -</td>
<td>- / -</td>
<td>3 / 3</td>
<td>Yes</td>
</tr>
<tr>
<td>This work</td>
<td>65nm</td>
<td>soft switches * with resonance</td>
<td>- / 2.2</td>
<td>30 / -</td>
<td>1 / 1</td>
<td>Yes</td>
</tr>
</tbody>
</table>

* soft means without any explicit switches carrying RF signals

compared to $C_{p,TX}$ is absorbed into the implementation of $C_o$. High resistance due to the off-state of $M_2$ and $M_3$ has a negligible penalty on the DCO-PA. Nevertheless, the single-MOS $M_{1,PA}$ cannot get overly large for the sake of DCO-PA efficiency, otherwise its off-state parasitic $C_{p,TX}$ may inadvertently break the tunability range of the switchable $C_o$, ruining the RX-mode input matching. Comparison with state-of-the-art integrated T/R switches is presented in Table 3.1.

#### 3.3.2 Passive Gain-Boosting Push-Pull LNA

The RX-mode input matching is realized through the inductive source degeneration provided by the supply/ground bond-wire inductances $L_{bd}$ to create a real part of the input impedance, thus, avoiding any additional bulky on-chip inductors. Assuming a good symmetry between the PMOS and NMOS transistors, with $I_{g,in}$ flowing entirely through $C_{gs}$, the input impedance looking into the LNA from $V_g$ node in Figure 3.10(b) can be derived as

$$z_{in,g} \approx \frac{s(1-k_2^2)L_d}{1+\frac{s^2}{\sqrt{L_d C_{gs} (1-k_2^2)}}} + 2sL_{bd} + \frac{2}{sC_{gs}} + \frac{2}{sC_c} + 2 \frac{g_{m2} L_{bd}}{C_{gs}}$$

$$\approx s \left( (1-k_2^2)L_d + 2L_{bd} \right) + \frac{2}{sC_{gs}} + \frac{2}{sC_c} + 2 \frac{g_{m2} L_{bd}}{C_{gs}}$$

Note that the effect of $C_z$ can be neglected at around $\omega_0$ due to the induced zero in the RX mode, which is also located at $2\omega_0$ and confirmed by $\omega_n$ in (3.25). Deploying a practical bond-wire inductance $L_{bd} \approx 0.5$ nH, real part of the impedance $z_{g,real} \approx 160$ Ω with $g_{m2} \approx 8.5$ mS
and \( C_{gs} \approx 53 \text{fF} \) under the supply \( V_{DD,LNA} = 0.5 \text{V} \). Further, \( z_{g,real} \) is then scaled down by a factor of \( n_2^2/k_2^2 \) when reflected to the antenna port due to the impedance transformation of \( T_2 \). The real-part of impedance looked into from the antenna port is thus roughly 74 \( \Omega \), which is quite close to the simulation result shown in Figure 3.11(b), validating the feasibility of the introduced T/R switch. Further, the simulated \( S_{11} \) and Smith chart in both T/R modes are exhibited in Figure 3.11(c) and Figure 3.11(d). They cover the intended frequency band of interest of 2.4 to 2.48 GHz with margin, and validate the feasibility of the introduced T/R switch. Under various bondwire inductance \( L_{bd} \) values (0.5 nH to 1 nH), simulation results show that the input impedance matching with \( S_{11}<-15 \text{dB} \) is well maintained.

![Figure 3.13: Chip micrograph of the single-pin antenna interface RF front-end.](image)

The passive gain boost due to the step-up transformer is \( A_{v,tran} \approx k_2/n_2 \approx k_2\sqrt{L_d/L_o} \approx 1.5 \) (3.5 dB), which is favorable for the voltage amplification and to alleviate noise contribution from the succeeding push-pull stage, thus ultimately saving consumed power [106]. The noise figure (NF) of the cascaded lossy passive network and LNA is described as \( NF_{tot} = L \cdot NF_{LNA} \) in [96] while \( L = P_{in}/P_{out} \) stands for the power loss defined by the ratio of available powers between the input and output. Consequently, the expression for \( NF_{tot} \) is given as

\[
NF_{tot} \approx \frac{R_s M_2^2 \omega^2}{(R_s+r_{L_o}) \omega^2 + r_{L_d} (R_s+r_{L_o})^2} \left( 1 + \frac{8\gamma}{g_{m2} R_{in}} \right) \tag{3.31}
\]

where \( R_s \) is the source impedance, \( r_{L_o} \) and \( r_{L_d} \) represent the series losses of the transformer coils, and the excess noise coefficient \( \gamma \) is assumed to be 2/3 for long-channel transistors.
Moreover, the input resistance of the push-pull stage $R_{in} = z_{g,real}$, as previously discussed. The first term at the right-hand side of equation (3.31) is exactly the available power gain of the transformer. Theoretically, it gives a total noise figure $NF_{tot} \approx 5.5$ dB\textsuperscript{1} by substituting into all the design parameters at 0.5 V supply without engaging any noise cancellation technique [107]. Device mismatches introduce a maximum 0.15 dB standard deviation on the key LNA performances confirmed by the Monte Carlo simulation. At the slow-slow (SS) corner, the key performance of the LNA, namely $S_{11}$, $S_{21}$ and NF, degrades mainly attributing to the current drop, which can be easily compensated by raising the power supply a bit.

A full schematic diagram of the proposed single-pin antenna interface RFE is depicted in Figure 3.12. A self-biased replica circuitry is intended to bias the LNA in the RX mode. A test buffer with a low voltage gain is designed to facilitate the measurements, especially from the system linearity standpoint. Switching between the TX/RX modes is realized through toggling the relevant supply switches between $V_{DD}$ and ground.

3.4 Experimental Results

The RF front-end (RFE) chip is fabricated in 65-nm standard CMOS, occupying a compact active area of 0.17 mm\textsuperscript{2}, as shown in the die photo in Figure 3.13. Measurement results of

\textsuperscript{1}NF\textsubscript{tot} will slightly increase by 0.38 dB if the gate-induced noise is taken into account.
3.4 Experimental Results

Figure 3.15: TX mode measurement: DCO-PA phase noise under $P_{out} = 0 \text{dBm}$.

the introduced RFE in TX mode are summarized in Figure 3.14. The single-MOS DCO-PA achieves 20.8% total power efficiency at 0 dBm RF output and 0.7 V supply. The measured HD$_2$ emission, shown in Figure 3.14(a) when delivering a single-tone at 0 dBm, is $<-44 \text{dBm}$, which verifies the effectiveness of the zero-shifting capacitor $C_z$. A relatively high efficiency of 10.2% is retained at 10 dB large power back-off by scaling the supply in TX mode to 0.3 V, which is confirmed by Figure 3.14(b). The measured phase noise of the DCO-PA is plotted in Figure 3.15. At 0.7 V supply, it reaches $-126.4 \text{dBc/Hz}$ at 2.5 MHz offset from the 2.4 GHz carrier. The DCO-PA covers a frequency tuning range from 2.2 to 2.5 GHz, leaving enough margin to cover the targeted frequency band of interest in case of process variations. The DCO-PA stability over antenna impedance variations is measured under VSWR = 1.5:1, and captured in Figure 3.16. It shows a maximum 1.1 dB $P_{out}$ variation when delivering 0 dBm RF power.

Resilience to jammers is validated in the same manner as in [91] by means of connecting the signal generator, DCO-PA output and spectrum analyzer to a three-port circulator, which allows the signal to travel in the direction of signal generator $\rightarrow$ DCO-PA output pin $\rightarrow$
3.4 Experimental Results

![Graphs showing experimental results](image)

Figure 3.16: TX mode measurements: (a) $P_{\text{out}}$ and DCO-PA efficiency under VSWR = 1.5:1; (b) Harmonic emissions under VSWR = 1.5:1.

spectrum analyzer. The scenario of applying a -30 dBm interferer at $\Delta f = 5$ MHz offset frequency from the 2.4 GHz carrier is sketched in Figure 3.17(a) showing a jammer image spur at -41 dBm, which is 28 dB better (lower) than that in [91] which barely provides any isolation between the antenna and oscillator. The single-MOS DCO-PA is so robust that can hardly get injection locked by the interferers even as strong as 0 dBm, shown as the blue curve in Figure 3.17(b). Jammers at large offsets of $\Delta f = 10, 100$ MHz from the carrier are also captured in the same plot.

When switching from the DCO-PA output pin to the LNA input, the measured key LNA performance metrics are demonstrated in Figure 3.18. At a 0.5 V supply, the LNA exhibits $S_{21} = 11$ dB with $S_{11} < -20$ dB, consuming only 174 $\mu$W power. The corresponding NF is 6.8 dB within which the test buffer contributes roughly 0.2 dB by simulation. The worsened NF versus the calculation in (3.31) may stem from the degraded $Q$-factor of the transformer in which the passive devices and wires are put right underneath and which could not be modeled in the EM simulation. The LNA performance under lower (0.45 V) or higher (0.6 V) supplies are also captured in Figures. 3.18(a)–(b) with 90 $\mu$W and 540 $\mu$W power consumption respectively. Two-tone test is applied to measure IIP$_3$, as explained in Figure 3.18(c)–(d). The power for fundamental tone and output inter-modulation (IM) products are captured from the spectrum analyzer, and then extrapolated over increasing the fundamental tone
3.4 Experimental Results

Figure 3.17: Jammer resilience performance: (a) output spectrum when in front of a -30 dBm jammer at 5 MHz offset; (b) image spur power versus the interferer power at various offset from the carrier.

amplitude, yielding an excellent $IIP_3 = -2.23 \text{ dBm}$. Further, the 1 dB compression point of the LNA is measured at -13.6 dBm. Table 3.2 compares it with stat-of-the-art LNAs.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>Supply (V)</th>
<th>$P_{DC}$ (µW)</th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
<th>$IIP_3$ (dBm)</th>
<th>FOM * (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[107]</td>
<td>65nm</td>
<td>2.4</td>
<td>0.7</td>
<td>475</td>
<td>2.8</td>
<td>-10.7</td>
<td>28.8</td>
</tr>
<tr>
<td>[108]**</td>
<td>40nm</td>
<td>2.4</td>
<td>0.8</td>
<td>30</td>
<td>3.3</td>
<td>-11.6</td>
<td>38.2</td>
</tr>
<tr>
<td>[108]**</td>
<td>40nm</td>
<td>2.4</td>
<td>0.18</td>
<td>30</td>
<td>5.2</td>
<td>-8.6</td>
<td>37.7</td>
</tr>
<tr>
<td>[109]</td>
<td>65nm</td>
<td>2.4</td>
<td>0.3</td>
<td>930</td>
<td>4.7</td>
<td>-20</td>
<td>20.7</td>
</tr>
<tr>
<td>This work</td>
<td>65nm</td>
<td>2.4</td>
<td>0.5</td>
<td>174</td>
<td>6.8</td>
<td>-2.2</td>
<td>30.2</td>
</tr>
</tbody>
</table>

* FOM=$10 \log \left( \frac{\text{Gain} \cdot 20 \cdot 10^{(IIP3-10)/20} \cdot 10^{-NF} \cdot 10^{-P_{DC}/10^{-3}}}{10} \right)$ \[107\] ** \[108\] includes two LNA designs with simulation results only

The DCO-PA performance is summarized in Table 3.3 and favorably compares to state-of-the-art 2.4 GHz TXs. To the best of authors’ knowledge, the presented single-MOS DCO-PA architecture is the first fully integrated single-ended solution with competitive carrier phase noise and power efficiency, especially at low power modes, while simultaneously handling the harmonic emission and easy switching to the RX LNA. Even the most recent contender, [84],
which uses a ring-oscillator-based edge-combining frequency generation TX, no longer shows
the power efficiency advantage at lower (-20dBm) RF power, especially given that only drain
efficiency is reported there with off-chip matching and filtering. In addition, the proposed
single-MOS DCO-PA outperforms it at least 18dB in terms of phase noise performance. The
deep HD\textsuperscript{2} rejection is achieved (<-44dBm) without resorting to complex circuitry, external
filtering or calibration and with insignificant degradation in power efficiency.

3.5 Conclusion

A simple RF front-end with a fully integrated matching network for 2.4GHz TDD radios
is introduced in this chapter. It features a function-reuse single-MOS DCO-PA with full \( V_{DD} \)
utilization while improving antenna-to-DCO isolation for better resilience to interferers. The 2nd harmonic emission is deeply suppressed by a zero-shifting capacitor that crosses over the non-inverting matching transformer. This not only allows to share the same antenna pin with the RX but also provides passive-gain boosting to the push-pull LNA.
### Table 3.3: Comparison with state-of-the-art 2.4GHz RF Front-End

<table>
<thead>
<tr>
<th>CMOS Technology</th>
<th>Supply Voltage (V)</th>
<th>RF band (GHz)</th>
<th>TX Architecture (in open loop operation)</th>
<th>RF Power (dBm)</th>
<th>Power Consumption (mW)</th>
<th>Efficiency (%)</th>
<th>Active Area (mm²)</th>
<th>HD2/HD3 (dBm) @ Pout</th>
<th>VCO Phase Noise (dBc/Hz) @ 2.5 MHz / RF power</th>
<th>VCO Frequency Range (GHz)</th>
<th>TX_FOM (dBm) @ Pout</th>
<th>5MHz jammer Image Spur (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40nm</td>
<td>0.4</td>
<td>2.4</td>
<td>LC-VCO + Edge Combiner + SC + DPA</td>
<td>-10</td>
<td>-10</td>
<td>8</td>
<td>3.3</td>
<td>N/A</td>
<td><strong>123</strong></td>
<td>2.37 - 2.5</td>
<td>-73.5</td>
<td>-37</td>
</tr>
<tr>
<td>130nm</td>
<td>0.6 to 0.9</td>
<td>2.4</td>
<td>Class-D PA + LC + VCO + Divider + Buffer</td>
<td>22</td>
<td>22.25</td>
<td>18</td>
<td>16.5</td>
<td>0.98</td>
<td><strong>123</strong></td>
<td>2.4 to 2.5</td>
<td>-72.5</td>
<td>-28</td>
</tr>
<tr>
<td>65nm</td>
<td>1.2</td>
<td>2.4</td>
<td>Single MOS DCO</td>
<td>0.35</td>
<td>0.35</td>
<td>18</td>
<td>0.35</td>
<td>0</td>
<td><strong>123</strong></td>
<td>2.16</td>
<td>-72.5</td>
<td>-28</td>
</tr>
<tr>
<td>40nm</td>
<td>0.3 to 0.7</td>
<td>2.4</td>
<td>Single MOS DCO</td>
<td>0.35</td>
<td>0.35</td>
<td>18</td>
<td>0.35</td>
<td>0</td>
<td><strong>123</strong></td>
<td>2.16</td>
<td>-72.5</td>
<td>-28</td>
</tr>
<tr>
<td>40nm</td>
<td>0.3 to 0.7</td>
<td>2.4</td>
<td>Single MOS DCO</td>
<td>0.35</td>
<td>0.35</td>
<td>18</td>
<td>0.35</td>
<td>0</td>
<td><strong>123</strong></td>
<td>2.16</td>
<td>-72.5</td>
<td>-28</td>
</tr>
</tbody>
</table>

**Notes:**
- TX_FOM = HD2 + 10log(PDC)
- No. of external components
- VCO frequency range (GHz)
- VCO Phase Noise (dBc/Hz)
- VCO Frequency Range (GHz)
- Power Consumption (mW)
- Efficiency (%)
- Active Area (mm²)
- HD2/HD3 (dBm) @ Pout
- VCO Phase Noise (dBc/Hz) @ 2.5 MHz / RF power
- VCO Frequency Range (GHz)
- TX_FOM (dBm) @ Pout
- 5MHz jammer Image Spur (dBm)

**References:**
- CICC' 18 [89]
- JSSC' 19 [84]
- JSSC' 14 [93]
- JSSC' 16 [90]
- JSSC' 17 [91]
- This work
As stated in the previous chapters, the unavoidable 2nd harmonic emission in single-ended power amplifiers can be easily rejected via artificially adjusting the inherent interwinding capacitance $C_{int}$ of the monolithic transformer either in the format of a feedback coupling-cancellation (FBCC) capacitor $C_c$ in Chapter 2 or a zero-shifting capacitor $C_z$ in Chapter 3, which requires the transformer to be in the inverting or non-inverting configuration, respectively. Interestingly, the two proposed harmonic suppression techniques share the same schematic as shown in Figure 4.1, except that the direction of the coupling factors $k_m$ are opposite. Different from the zero-shifting capacitor $C_z$, which regulates the position of the visible zero-notch in the frequency response of a general non-inverting transformer matching network, the FBCC capacitor controls the feedback at $2\omega_0$ frequency through altering the rolling-down slope of the inverting transformer gain response to ensure the perfect phase cancellation.

More features of the transformer-based inherent harmonic rejection techniques will be
Figure 4.1: Inherent harmonic suppression in monolithic transformers by artificially adjusting the inter-winding capacitance.

Figure 4.2: The rolling-down slopes of the gain responses by changing $C_{tot}$ with $C_c$ as the design-adjustable part.

discussed in this chapter mainly with regard to the frequency coverage and capacitor variance resilience.

4.1 Frequency Coverage

Up to now, the discussion regarding the HD2 suppression performance due to the FBCC capacitor is limited to the 900 MHz frequency channel of the DPA. As discussed in Chapter 2, the proposed HD2 cancellation purely relies on the feedback current $i_f$ having equal amplitude
and anti-phase property to the HD2 component at the common drain node of the DPA. From Equation (2.2), the feedback current will be decided by $C_c$ being the adjustable part of total inter-winding capacitance $C_{tot}$ and the voltage gain $G(s)$ of the tank. In addition to that, $C_c$ can increase the feedback at $2\omega_0$ through shifting the zero locations, thus to alter the rolling-down slope of the gain response whose effect is shown in Figure 4.2.

Furthermore, $C_L$ as the operational loading capacitance can also influence the feedback at $2\omega_0$ through shifting the peak position of $G(s)$, adjusting the rolling-up slope of the gain response before it rolls down. Besides, $L_s$ and $C_L$ are closely related to the resonance for fundamental frequency selection as indicated in Equation (2.9). As $C_c$ is not adjustable in this specific implementation, it is thus expected that $C_L$ can be tuned to maintain the HD2 rejection when the DPA operates at various frequency channels. Figure 4.2 demonstrates the HD2 rejection performance over different PA operating frequencies by tuning $C_L$ by 0.5 pF steps. It indicates that <-49 dBc HD2 emission is achieved covering a wide operation frequency range from 700 MHz to 950 MHz defined by 802.11ah. As to the 2.4 GHz band BLE transmitters. There is no reason to be concerned about the frequency coverage of the HD2 rejection technique using the zero-shifting capacitor due to the fact the BLE technology operates in the 2.400–2.4835 GHz spectrum range with 40 2-MHz channels. The HD2 suppression is proved to be fairly well contained throughout all the channels (at least 25 dB rejection) shown as the grey area in Figure 3.9.

### 4.2 Resilience to Capacitor Variation

To facilitate the comparison between the FBCC capacitor and zero-shifting capacitor into HD2 suppression, the latter technique is applied into the 802.11ah transmitter described in Chapter 2 by simply rearranging the transformer in the non-inverting configuration and tuning the capacitance value. Consequently, a zero-shifting capacitor $C_z \approx 2.6 \text{ pF}$ is needed to conserve the similar performance as the FBCC capacitor with > 20 dB HD2 rejection shown in Figure 4.4.

The bright side of the zero-shifting capacitor lies in the visible zero-notch in the frequency response which is easy to understand and explain while at a great sacrifice of implementation cost with approximately $10 \times$ higher capacitance in comparison with the FBCC capacitor $C_c \approx 247 \text{ fF}$. Besides, the transformer in the inverting configuration generally has a higher
4.2 Resilience to Capacitor Variation

Figure 4.3: FBCC HD2 suppression versus frequency through $C_L$ tuning.

...cut-off than for the non-inverting connection as a result of the absence of the transmission zero.

The HD2 self-suppression technique using the FBCC capacitor is principally based on the 180-degree phase difference between the primary and secondary coils of the inverting transformer, which may deviate significantly at higher frequencies. It needs to be checked carefully whether the “inverting” property of the transformer still holds at $2\times$ operation frequency, but transformer geometries need to be considered differently at higher frequencies. In this scenario, the zero-shifting capacitor may be a better choice as seen from the retrospective Equation (4.1), a much lower $C_{tot} = C_{int} + C_z$ is required to shift the zero-notch to relatively high frequency.

$$\omega_n = \sqrt{\frac{k_2n_2}{L_o C_{tot} (1 - k_2^2)}} \quad (4.1)$$

where $\omega_n$ is the corner frequency of the numerator’s second-order polynomial and primarily decides the zero-notch location. As long as the $2\omega_0$ frequency sits below the self-resonance frequency of the transformer, the zero-notch can be tuned to $\omega_n \approx 2\omega_0$, thus effectively rejecting the HD2 component.

Another important aspect is the HD2 suppression performance under process variations.
4.2 Resilience to Capacitor Variation

Figure 4.4: Applying the zero-shifting $C_z$ capacitance into suppressing the HD2 of sub-GHz band transmitter.

The implemented capacitor may significantly deviate in value from the design-optimized capacitance for the deepest harmonic suppression. The optimum capacitor $C_{\text{opt}}$ is amended by adding a $\pm 20\%$ variation to simulate the HD2 emission power in both the sub-GHz DCO-DPA with FBCC capacitor and the 2.4 GHz DCO-PA with zero-shifting capacitance, as shown in Figure 4.5. It can be seen that the FBCC capacitor with a fairly small optimum value $C_{\text{opt,c}} \approx 247 \, \text{fF}$ shows better immunity to process variation with less than 5 dB performance degradation. Nevertheless, the zero-shifting capacitor with a rather large optimum value $C_{\text{opt,z}} \approx 2.3 \, \text{pF}$ is more sensitive to process variation with more than 15 dB deterioration. To some extent, the huge deterioration originates from its large absolute value. In spite of this, the zero-shifting technique works well in narrow band wireless system [110].

Though the proposed transformer-based harmonic suppression through the zero-shifting capacitor looks superficially similar as the FBCC technique, the implementation, working principle and system response differ in essence. The zero-shifting method requires the
4.2 Resilience to Capacitor Variation

Capacitor Variation (%)

-20 -15 -10 -5 0 5 10 15 20

HD2 Power (dBc)

-65
-60
-55
-50
-45
-40

FBCC Capacitor
Zero-shifting Capacitor

2.4GHz DCO-PA

Figure 4.5: HD2 power over capacitor variation.

The transformer in the non-inverting configuration, mutual inductance $M > 0$, such that there is the visible valley in the frequency response of the transformer-based matching network due to the complex-conjugate zeros pair in the numerator of its transfer function, and then the harmonic suppression relies on steering the location and strength of this valley. Whereas with the FBCC method, the harmonic suppression is based on the transformer in the inverting configuration, mutual inductance $M < 0$, resulting in a totally different frequency response with two real zeros (one RHP, the other LHP) in the numerator in its transfer function. Although difficult to see directly, the harmonic suppression depends on the anti-phase feedback coupling cancellation.

The proposed transformer-based harmonic suppression through the zero-shifting capacitor is more viable and reliable due to the strength and position of the visible zero-notch. It purely depends on engineering the passive matching network regardless of the input signal (drain node of the power transistor), whereas the effectiveness of the FBCC harmonic cancellation heavily relies on both the input and feedback harmonic components having the same strengths.
4.3 Conclusion

Comparison between the two inherent harmonic suppression techniques in monolithic transformers are discussed in this chapter mainly in terms of frequency coverage and resilience to capacitor variations.
5.1 Summary

To merge the two most power-hungry and area-constrained blocks in the ULP transmitter, namely, the RF oscillator and the RF power amplifier, is one promising and viable way to enable the power-efficient and cost-effective fully integrated RF CMOS transmitters for the Internet-of-Things (IoT) applications.

Two chip prototypes have been fabricated and measured to demonstrate the proposed solutions. Concretely, the physically merged DCO-DPA and the functionally merged DCO-PA for 802.11ah and BLE transmitters, respectively.

The compact physically merged DCO-DPA circuitry with a fully integrated matching network for the sub-gigahertz IoT TX achieves the highest PA efficiency, thanks to its single-ended configuration while maintaining sufficiently high HD2 suppression by means of the introduced FBCC capacitor. The lowest DCO power consumption and the smallest system area are achieved via the proposed concentric layout topology with the resulting coupling being virtually eliminated by the proposed controllable DPA-to-DCO injection.
Furthermore, the super-simple RF front-end with a fully integrated matching network for 2.4 GHz TDD radios is introduced. It features the functionally merged single-MOS DCO-PA with full \( V_{DD} \) utilization while improving antenna-to-DCO isolation for better resilience to interferers. The 2nd harmonic emission is deeply suppressed by a zero-shifting capacitor that crosses over the non-inverting matching transformer. Not only this allows to share the same antenna pin with simple switching to the RX but also it provides passive-gain boosting to the push-pull LNA in the RX chain.

Taking advantage of artificially adjusting the inter-winding capacitance in monolithic transformers to suppress the harmonics would influence the self-resonant frequency of the transformers, thus limiting its application at high frequencies.

### 5.2 Some Suggestions for Future Developments

The future research can be advanced on several fronts:

1. **For the physically-merged sub-GHz transmitter:**

   A relatively large 150 um distance is reserved within the dominant coupling path between the outermost turn of the DPA transformer and the innermost turn of the DCO transformer in order to minimize the coupling factor. However, it seems the PA pulling effect is not so strong to create significant coupling and modulation distortion from the measured EVM results with the compensation path turning off/on, which signifies that concentric octagon layout topology can be further optimized to reduce the chip area as the controllable DCO-PA coupling can compensate more severe DCO pulling.

2. **For the functionally-merged 2.4 GHz RF front-end:**

   The source-to-gate feedback transformer utilized to enable the self-oscillation of the single-MOS DCO-PA would inevitably consume the output swing in the presence of a signal swing across the source node deteriorating the transmitter efficiency. Additionally, the antenna-to-DCO isolation is merely provided by the drain-to-source separation of the transistor. It is favored to further improve the isolation for better resilience to interference. Twisted inductors/transformers [111] [112] can be a promising technique to offer better isolation through the magnetic field cancellation beyond the perimeter of the passives. Equivalent inductances at the source node and drain node can be diminished
or increased through connecting the two (or even more) twisted windings in parallel or in series, respectively which is beneficial to boost the transmitter efficiency.


[80] M. Ding et al., “A 0.8V 0.8mm^2 bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in


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Acknowledgment

It finally arrives at the last stop of my PhD journey with joys and sorrows. Those stunning moments just flash through my mind, unmanageably.

I still remember clearly the first day when I dropped by your office and the photo I shared on the WeChat Moments with the nameplate reading PROF. R STASZEWSKI. You ranked last in the list I’ve made during my PhD application in order of chances to be admitted from high to low. Most dramatically, you are the only one who offers me full scholarship. I gradually realized the way a great man show his greatness is to be willing to give opportunity and confidence to your students. Sometimes I just have the feeling that the level of your giants’ shoulders are so high that I can never stand on it. I am always proud to be one of your PhD student.

You have taught me a lot unquestionably from every aspect far more than academically. I remember when we visited the National Museum of China together in Beijing you pointed at the Buddhist Sculptures telling me stories about the Buddha, the Bodhisattva and the Arhat; I remember when we saw the Confucius Statue in Cambridge you shared gladly with us that you know “Kongzi” and “Laozi” in mandarin; I remember when we were floating freely in the Dead Sea near Jerusalem smearing each others’ body with mud. Unreservedly, I have learned how to analyse problems, how to write and correct papers, and how to communicate with different people all from you. Most sincere gratitude to you.

I would like also to express great appreciation to all members of my thesis examination committee: Prof. Antonio Liscidini (University of Toronto), Prof. Teerachot Siriburanon (University College Dublin), and Prof. Elena Blokhina (University College Dublin) for the precious and valuable time to review the thesis with remarkable comments and suggestions.
Many thanks to Prof. Jun Yin and Prof. Pui-In Mak from the State-Key Laboratory of Analog and Mixed Signal VLSI, University of Macau who have supervised me with greatest wisdom and patience during my one year visiting there. It is such a great opportunity to work with the rapidly rising group in the world.

Many thanks to Dr Yao-Hong Liu from imec, the Netherlands who offers me the unique internship opportunity to work on the cutting-edge research in miniaturized ULP systems for medical applications at the most prestigious microelectronic research institution in Europe. Your passion and expertise into the power optimization across the analog and digital world has really inspired me.

I would also like to express my thanks to my college and friend Dr Y. Hu with whom I have been talked to even before I joined the UC Dublin team. It is the continuous talk that witnesses the ups and downs of the tough PhD life.

The same appreciation shall be given to those PKUers all over the world: S. Liu, X.R. Zhang, Z.K. Ruan, K. Lin, Y. Peng, T.N. Hu, S.C. Li, J.H. Zhang, J.L. Hou, C.X. Wang, C. Chen, F. Gao, H.B. Shao, F. Huang, M.Q. Liu, and J.L. Zhao. You always show me your concerns unsparingly in an era of indifference. It is that I know you are everywhere that I dare to be anywhere.


I would like to thank our team manager Sunisa for caring every detail of our life on and off campus. Many thanks for all the other team members.

Kai Xu
September 2019
Dublin, Ireland
A 3.5mmx3.8mm crystal-Less MICS transceiver featuring coverages of ±160ppm carrier frequency offset and 4.6-VSWR antenna impedance for insertable smart pills [ISSCC 2020] (with imec-Netherlands)

A 0.85 mm² 51%-Efficient 11-dBM Compact DCO-DPA in 16-nm FinFET for Sub-Gigahertz IoT TX Using HD, Self-Suppression and Pulling Mitigation [ISSCC SRP-2018, JSSC-2019] (with Feng-Wei Kuo)

A 2.4-GHz single-pin antenna interface RF front-end with a function-reuse single-MOS VCO-PA and a push-pull LNA in 65nm CMOS [ASSCC-2018, JSSC-2019 (minor revision)]

An Inductorless 100MHz-1GHz Wideband Noise Cancellation Low-Noise-Transconductance-Amplifier for IoT applications in 28nm CMOS

Chip Micrograph Gallery
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