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A Broadband Continuous Class-F GaN MMIC PA Using Multi-Resonance Matching Network

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Abstract—In this paper, we present a design technique for broadband harmonic-tuned monolithic microwave integrated circuit (MMIC) power amplifiers (PAs). A multi-resonance harmonic matching network is proposed for the continuous class-F mode operation, featuring low loss and compact chip area for integrated PA realization. A design procedure is developed for this network, considering low quality factor and electromigration current density limitation of on-chip inductors. A proof-of-concept GaN MMIC PA, implemented in a 0.25- μm GaN-on-SiC technology, provides 33.9–36.1 dBm output power and 38–48% power-added efficiency (PAE) in the frequency band 4–6 GHz. For a 64-QAM signal with 100 MHz modulation bandwidth and 8 dB peak-to-average power ratio (PAPR), at 5 GHz, the average output power of 30.2 dBm and average PAE of 32% are achieved, while the error vector magnitude (EVM) is –32 dB.

Index Terms—5G, broadband amplifier, GaN, monolithic microwave integrated circuit (MMIC), power amplifier (PA).

I. INTRODUCTION

Broadband high-efficiency power amplifiers (PAs) are important components in wireless transmitters, especially in the next generation wireless networks, 5G, due to the increasing demands of high data rates. Gallium Nitride (GaN) technology with impressive output power capability has become popular in recent years [1]. In 5G, it is expected that GaN monolithic microwave integrated circuit (MMIC) PAs will be extensively deployed in cellular base stations to reduce size and enhance system integration [2]. Specific features of the GaN process, mainly high supply voltage and large optimum load resistance, call for special considerations in the PA circuit design [3].

The continuous-mode enables broadband operation of harmonic-tuned PAs by extending the design space for the fundamental and harmonic load impedances [4]. Most of PAs designed based on the continuous-mode have been realized as hybrid circuits. However, for MMIC implementations, it is essential to develop low-loss and compact circuits [5]. In this paper, we present a design approach for realization of the continuous class-F mode in a broadband MMIC PA. We propose a suitable multi-resonance harmonic matching network, and develop a design procedure for this circuit, considering loss and current density limitation of on-chip inductors. This technique is verified using a proof-of-concept MMIC PA implemented in a 0.25- μm GaN-on-SiC process.

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II. BROADBAND HARMONIC MATCHING NETWORK

A. Design Approach

The continuous class-F mode is described by the following optimum load impedance at fundamental, second-, and third-harmonic frequencies

$$Z_L(f) = \left(\frac{2}{\sqrt{3}} + j\gamma \right) R_{opt} \quad (1)$$

$$Z_L(2f) = -j \frac{7\sqrt{3}\pi}{24} \gamma R_{opt} \quad (2)$$

$$Z_L(3f) = \infty \quad (3)$$

where $R_{opt} = 2V_{dc}/I_{max}$ is the optimum load resistance, V_{dc} and I_{max} denote the drain dc voltage and the maximum current, and $-1 \leq \gamma \leq 1$ [6].

In practice, it is difficult to meet all these conditions, especially in an MMIC PA where loss of passive components prohibits the use of high-order matching circuits. For example, (1) and (2) indicate that a constant ratio should be maintained between reactive parts of the second-harmonic and fundamental impedances, i.e., $X_L(2f)/X_L(f) \approx -1.59$, while (3) indicates that an open-circuit impedance is required at the third harmonic. These conditions, however, cannot be easily satisfied over a broad bandwidth. Furthermore, nonlinearity of the transistor's parasitic capacitances and output resistance limit accuracy of this model [6]. In order to develop practical design criteria, we use the optimum load impedance at fundamental frequency as per (1), while harmonic load-pull simulations are used to determine the optimum load impedances at harmonic frequencies.

In the following harmonic load-pull simulations, a 0.25- μm GaN-on-SiC process from WIN Semiconductors is used. The transistor is driven 2–3 dB into gain compression, to deliver about 37 dBm output power with 24 dBm input power at 5 GHz. The input source impedance is optimized at the fundamental frequency and short-circuited at higher order harmonics. The transistor parameters R_{opt} and C_{out} are roughly extracted as 70 Ω and 0.5 pF, respectively. The second- and third-harmonic load-pull simulation results are, respectively, shown in Figs. 1 and 2. The impedances are given at the extrinsic drain of the transistor. The results are given for $\gamma = 0$, while further simulations indicate that the harmonic load-pull contours do not significantly change with γ .

Fig. 1. Second-harmonic load-pull simulation results for the extended continuous class-F mode operation, with highlighted area for PAE > 60%.

Fig. 2. Third-harmonic load-pull simulation results for the extended continuous class-F mode operation, with highlighted area for PAE > 60%.

Fig. 3. Proposed multi-resonance harmonic matching network.

B. Proposed Multi-Resonance Harmonic Matching Network

To enable the continuous class-F mode operation, an harmonic matching network shall provide optimal load impedance in the fundamental and harmonic frequency bands. Unfortunately, a traditional single-frequency multi-harmonic matching network cannot support these conditions over a broad bandwidth [5]. For MMIC implementation, this network should have a simple architecture to reduce loss and save chip area. Moreover, the network should absorb the drain-source parasitic capacitance of the transistor and include a parallel inductor to provide the drain bias path. As an example, simple network for an integrated GaN PA was proposed in [7], but it is applicable only to class-J mode.

In this work, we propose a network, shown in Fig. 3, that is capable of meeting the continuous class-F mode conditions over a wide bandwidth for MMIC PAs. Broadband frequency response of the load impedance at fundamental and harmonics can be controlled via resonant frequencies of the three resonators ($\omega_{1,2,3}$). We present an intuitive analysis to provide insights into the circuit operation. Then, the circuit can be optimized in a circuit simulator to achieve the desired broadband response in the presence of loss and parasitics of the passive elements.

The input impedance of the circuit in Fig. 3 is derived as

$$Z_{in}(j\omega) = jX_p(\omega) || [jX_s(\omega) + R_L], \quad (4)$$

where $X_p(\omega)$ and $X_s(\omega)$ are respectively given by

$$X_p(\omega) = \frac{\omega L_1}{1 - \omega^2 L_1 C_1} \quad (5)$$

$$X_s(\omega) = \omega L_2 - \frac{1}{\omega C_2} + \frac{\omega L_3}{1 - \omega^2 L_3 C_3}. \quad (6)$$

By equating the respective real and imaginary parts of (1) and (4) at center of the band $\omega_0 = 2\pi f_0$, it can be shown that

$$X_p(\omega_0) = \left(-B_L(f_0) \pm G_L(f_0) \sqrt{\frac{1}{R_L G_L(f_0)} - 1} \right)^{-1} \quad (7)$$

$$X_s(\omega_0) = \mp R_L \sqrt{\frac{1}{R_L G_L(f_0)} - 1}, \quad (8)$$

where $G_L(f_0)$ and $B_L(f_0)$ are real and imaginary parts of the optimum fundamental load admittance $1/Z_L(f_0)$. We assume that the resonant frequency of the first resonator ω_1 is placed at $\omega_0 < \omega_1 < 2\omega_0$. Therefore, the resonator operates as an inductive reactance at the fundamental and a capacitive reactance at harmonics frequencies. It can be shown that this choice leads to the desired frequency response behavior at harmonic bands. Moreover, we choose $C_1 = C_{out}$, and hence using (5), the inductor L_1 is derived as

$$L_1 = \frac{1}{\omega_0} \frac{X_p(\omega_0)}{1 + \omega_0 C_{out} X_p(\omega_0)}. \quad (9)$$

The input impedance of the network should be reactive at harmonics to achieve high efficiency. Using (4), it is shown that the condition $R_{in}(n\omega_0) \ll X_{in}(n\omega_0)$ is simplified as

$$X_p(n\omega_0) \ll R_L + \frac{1}{R_L} X_s(n\omega_0) [X_s(n\omega_0) + X_p(n\omega_0)]. \quad (10)$$

This condition is automatically satisfied at sufficiently high frequencies, e.g., the third harmonic, as $X_p(n\omega_0) \approx 1/n\omega_0 C_1$ becomes much smaller than R_L . At the second harmonic, we can choose $\omega_3 \approx 2\omega_0$, to obtain a large $X_s(2\omega_0)$. At the third harmonic, an inductive impedance is required (see Fig. 2), which can be obtained by adjusting the resonant frequency ω_2 and circuit elements to make $X_s(3\omega_0)$ inductive (e.g., assuming $\omega_2 \approx 2\omega_0$ and using (6), $\omega_0^2 L_3 C_2 > 25/144$).

III. MMIC PA DESIGN

The layout structure of the harmonic matching network has significant effects on performance of the broadband integrated PA. In addition to the optimum load impedance conditions, other issues, including the losses and parasitics of passive elements, electromigration current density limit of transmission lines, and chip area should also be considered in the layout design. Properties of the double-metal transmission lines on the 100- μm SiC substrate are summarized in Table I. The line width should be chosen based on these tradeoffs.

To proceed, we present the design of a PA operating in 4–6 GHz using the developed technique. In the proposed circuit

TABLE I
PROPERTIES OF TRANSMISSION LINES IN THE GAN PROCESS.

Width (μm)	Z_0 (Ω)	Q	I_{max} (mA)
10	104	18	296
20	88	30	592
30	78	40	888
40	71	50	1184
50	66	57	1480

Fig. 4. Fundamental and harmonic load impedances of the designed harmonic matching network. The fundamental load impedance is given at the intrinsic drain while the harmonic load impedances are given at the extrinsic drain.

of Fig. 3, inductor L_1 should tolerate a dc current of 300 mA at the maximum output power. Moreover, simulations indicate that the layout of this inductor is critical in the PA's broadband performance. The other inductors are not burdened by such current density constraint and so their widths are optimized based on insertion loss and chip area. The inductors $L_{1,2,3}$ are implemented as meandered microstrip transmission lines with the width of 30, 15, and 30 μm , respectively. The circuit elements are roughly estimated as $L_{1,2,3} = [1.4 \ 0.6 \ 1.1]$ nH and $C_{1,2,3} = [0.5 \ 0.5 \ 0.3]$ pF. The resonant frequencies of the resonators are derived as $f_{1,2,3} = [6.0 \ 9.1 \ 8.7]$ GHz, indicating that the conditions set on these resonant frequencies are maintained as $f_0 < f_1 < 2f_0$, $f_2 \approx 2f_0$, and $f_3 \approx 2f_0$. The insertion loss of the matching network is 0.6–1.1 dB over the bandwidth.

The input impedance of the harmonic matching network in the fundamental (intrinsic drain) and harmonics (extrinsic drain) frequency bands is shown in Fig. 4. It is noted that load impedance in the fundamental band is almost placed on the constant resistance arc of the Smith chart, as theoretically expected from (1), while traces of the load impedance in the second- and third-harmonic bands are close to the high-efficiency areas shown in Figs. 1 and 2. The PA circuit schematic and chip micrograph are shown in Fig. 5.

IV. MEASUREMENT RESULTS

A. CW Measurements

The chip is fabricated in a 0.25- μm GaN-on-SiC process from WIN Semiconductors. The PA is biased at $V_{GS} = -2.4$ V and $V_{DS} = 28$ V, consuming 17 mA of bias current. The gate-source bias voltage is chosen such that soft gain compression of the PA be minimized. Measured drain efficiency (DE),

TABLE II
COMPARISON OF BROADBAND GAN MMIC PAs

	This Work	[7]	[8]	[9]	[10]
BW (GHz)	4–6	2.2–3.1	6.4–8.3	5.2–6.8	4.9–5.9
P_o (dBm)	33.9–36.1	24–27	36–36.6	45.7–46.4	37–37.7
PAE (%)	38–48	40–52	40–50	52–57	48–55
Gain (dB)	10–12.2	7–10	10–12	22	28.5–31.7
Modulation	64-QAM	—	256-QAM	—	256-QAM
BW_m (MHz)	100	—	7	—	80
PAPR (dB)	8.0	—	7.4	—	11.25
f_c (GHz)	5	—	7	—	5.7
EVM (dB)	–32	—	—	—	–32
$P_{o,av}$ (dBm)	30.2	—	28.7	—	30.6
PAE_{av} (%)	32	—	26	—	27
Area (mm^2)	2.3	4.0	7.8	12.5	4.7
Process	0.25 μm	0.8 μm	0.25 μm	0.25 μm	0.25 μm

power-added efficiency (PAE), and gain versus output power are shown in Fig. 6. The PA achieves maximum output power of 36.1 dBm and maximum DE/PAE of 51/48%, with associated power gain of 12.2 dB. In Fig. 7, output power and DE/PAE are shown versus frequency, at the fixed input power of 24 dBm. The PA achieves 33.9–36.1 dBm output power, 42–51% DE, 38–48% PAE, and 10–12.2 dB power gain in 4.0–6.0 GHz. The output power 1-dB bandwidth is 3.6–5.6 GHz.

B. Modulated Signal Measurements

The modulated signal measurements are performed by using R&S SMW200A vector signal generator and R&S FSW43 vector signal analyzer. In Fig. 8, measured output signal constellation and spectrum are shown for a 64-QAM signal with 100 MHz modulation bandwidth and 8 dB PAPR, at 5.0 GHz. An error vector magnitude (EVM) of –32.4 dB (2.4%) is achieved at average output power of 30.2 dBm. Also, adjacent channel leakage ratio (ACLR) of the output spectrum is –37.8 dBc for the lower channel and –38.5 dBc for the upper channel. In Fig. 9, EVM and average PAE are given versus average output power for different modulation bandwidths. The EVM degrades with an increased modulation bandwidth. For EVM < –28 dB, average output power of 32.1/32.0/30.2 dBm and average PAE of 39/38/32% are achieved for 50/100/200 MHz modulation bandwidth. The effect of higher modulation bandwidth is more pronounced when a more stringent EVM condition should be satisfied.

In Table II, performance of the designed PA is compared with broadband GaN MMIC PAs. The PA achieves a high efficiency over 4–6 GHz (40.8% fractional bandwidth), while it features a small chip area using the proposed harmonic matching network. Moreover, a low EVM of –32 dB is obtained for a 64-QAM signal with 100 MHz modulation bandwidth (BW_m), which is essential for 5G applications.

V. CONCLUSION

A design technique for broadband harmonic-tuned integrated power amplifiers (PAs) is presented in this paper. A multi-resonance circuit is proposed to realize the continuous

Fig. 5. Circuit schematic and chip micrograph.

Fig. 6. Measured PAE, DE, and gain versus output power, at 5.0 GHz.

Fig. 9. Measured EVM and average PAE versus average output power for a 64-QAM signal with 8 dB PAPR at 5.0 GHz.

Fig. 7. Measurement and simulation results for output power, DE, and PAE versus frequency, at input power of 24 dBm.

Fig. 8. Measured output constellation and spectrum for a 64-QAM signal with 100 MHz bandwidth and 8 dB PAPR at 5.0 GHz.

class-F mode in integrated PAs. A prototype PA, designed using the developed circuit and implemented in a GaN-on-SiC process, achieves high efficiency over a broad bandwidth and features a compact chip area.

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