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Broadband Fully Integrated GaN Power Amplifier With Minimum-Inductance BPF Matching and Two-Transistor AM-PM Compensation

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Abstract—In this paper, we present a design technique for broadband fully integrated GaN power amplifiers (PAs), with merged bandpass filter (BPF) and AM-PM compensation. The minimum-inductance BPF structure is used as the output matching network of the PA. A new theory of the minimum-inductance BPF is developed and it is shown that, compared to the standard BPF, it can be implemented using lower total inductance and provide higher out-of-band attenuation. Furthermore, using a two-transistor architecture, an AM-PM compensation technique is proposed where compressive and expansive nonlinearity profiles of the transistors' transconductance and gate-source capacitance are combined to achieve a linear total transconductance and input capacitance, over a wide power range. A fully integrated PA prototype, implemented in a 0.25- μm GaN-on-SiC process with 28-V supply, provides 35.1–38.9 dBm output power, 45–61% drain efficiency (DE), 40–55% power-added efficiency (PAE), and 11.3–13.4 dB power gain, across 2.0–4.0 GHz. For a 256-QAM signal with 7.2-dB PAPR and 100-MHz bandwidth at 2.4 GHz, it achieves 2.5% (–32.0 dB) rms error vector magnitude (EVM_{rms}) and –37.5/–37.6 dBc adjacent channel leakage ratio (ACLR), while average output power and DE/PAE are respectively 30.1 dBm and 20.6/19.5%, without predistortion. EVM_{rms} and ACLR can be improved to 0.5% (–46 dB) and –46.4/–46.8 dBc by using digital predistortion (DPD).

Index Terms—5G, AM-PM, bandpass filter (BPF), broadband amplifier, GaN, linearization, power amplifier (PA).

I. INTRODUCTION

The Fifth Generation (5G) wireless networks bring new challenges in hardware system and circuit design, calling for innovative solutions in various design aspects. Power amplifiers (PAs) are among the most important circuits which should meet stringent requirements in terms of efficiency, linearity, bandwidth, and output power. Several technologies are considered to implement integrated PAs for 5G applications [1]. CMOS is preferred in handsets where low power levels (e.g., 10 dBm) are required for each element of a phased array transmitter. Furthermore, GaN with impressive high output power density is well suited for small-cell base stations and beyond [2]. Nevertheless, the PA design in each process requires specific circuit techniques to meet stringent 5G system requirements.

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GaN provides several advantages over other semiconductor processes, such as CMOS. The higher supply voltage of GaN, e.g., 28 V, leads to a significantly higher power density. This enables high output power levels without the need for complicated and lossy power combining techniques which degrade efficiency and limit bandwidth of the PA. Moreover, high supply voltage leads to a larger optimum load resistance of GaN transistors which can be made close to 50 Ω , resulting in a lower impedance transformation ratio, wider bandwidth, and higher efficiency of the PA. GaN processes are mainly implemented on SiC substrate which feature losses comparable with GaAs and much lower than the Si substrate of CMOS and LDMOS. As a result, inductors and transmission lines with high quality factor are available to boost efficiency of the PAs. These considerations make GaN a promising process for high-power applications, e.g., base stations and radars, in RF and mm-Wave frequencies [3]–[5].

In a broadband transmitter, the PA is usually followed by a bandpass filter (BPF) for channel selection and suppressing the out-of-band distortions. Conventionally, surface/bulk acoustic wave (SAW/BAW) filters are used in mobile and base-station applications, because of high selectivity and low cost. However, their insertion loss is high (e.g., 2–3 dB) and are usually used in < 3 GHz bands. Furthermore, lumped-element filters can be used to attenuate out-of-band distortions, with lower insertion loss (e.g., 0.5–1 dB), where very high quality factors are not required. There are several advantages of *merging* the filtering function with the output matching network of the PA to improve efficiency and reduce physical size [6]. This is especially important in multi-input multi-output (MIMO) transmitters where the improved efficiency helps to reduce the overall power consumption and cooling power, while smaller circuit size is useful in making a compact system with lower cost. In integrated circuit PAs, this network should provide low insertion loss, compact chip area, and high out-of-band attenuation in the second-harmonic band.

Linearity performance of the PA is of paramount importance to accommodate spectrally efficient complex-modulated signals with non-constant envelope and high peak-to-average power ratio (PAPR). Conventional linearization approaches which perform linearization at a specific power level, e.g., sweet spot inter-modulation cancellation and derivative superposition technique, cannot be effective in such conditions. Therefore, a linearization technique is required which can operate over a *wide power range*. There are several specific

challenges in linearization of GaN PAs: (1) The *soft compression* feature of GaN HEMTs exacerbates nonlinearity of the PA, especially for high-PAPR complex-modulated signals [7]. (2) The charge trapping effects in GaN devices result in different nonlinearity behaviors in the static and dynamic conditions [8], [9]. These effects degrade linearity of the PA for wide modulation bandwidths, which is important in 5G applications. (3) GaN processes offer only N-channel transistors and, as a result, linearization techniques using complementary nonlinearity behaviors of NMOS and PMOS devices are not feasible.

In this paper, we expand the concepts introduced in [10], and present a design approach for broadband PAs with minimum-inductance BPF matching and AM-PM compensation. The new contributions can be summarized as follows.

- 1) A comprehensive theory of the minimum-inductance matching networks is developed based on bandwidth, in-band insertion loss, and out-of-band attenuation features. The effects of limited quality-factor of inductors, an important limitation of fully integrated PAs, are investigated in the presented theory.
- 2) A theoretical comparison between the minimum-inductance and standard BPF structures is presented and, for the first time, it is shown that the total inductance can be much lower, e.g., by 40%, in the minimum-inductance network. The total inductance ratio of the two networks is dependent on the impedance transformation ratio, quality factor of the optimum load impedance, and parameters of the minimum-inductance network.
- 3) The theory is extended to the case of high-order minimum-inductance networks, which can provide wider bandwidth for large impedance-transformation ratios.
- 4) The modulated-signal measurements are performed using higher-order 256-QAM signals with up to 200 MHz modulation bandwidth, which is important for high-data-rate 5G wireless communications. The effects of modulation order and bandwidth on the error vector magnitude (EVM) and average efficiency of the PA are illustrated. Furthermore, the modulated-signal measurements are presented across the 2.0–4.0 GHz band to check effectiveness of the proposed AM-PM compensation in a wide bandwidth.

The paper is structured as follows. In Section II, a new theory of minimum-inductance matching networks is developed, where bandwidth, in-band insertion loss, and out-of-band attenuation performances are investigated. In Section III, a two-transistor circuit combining compressive and expansive nonlinearity profiles of the transistors' transconductance and gate-source capacitance is proposed to compensate the AM-PM distortion of the PA. We present the circuit design details of a fully integrated GaN PA prototype in Section IV, and measurement results in Section V.

II. MINIMUM-INDUCTANCE MATCHING NETWORK

The minimum-inductance BPF structure was first introduced in 1958 to reduce the number of expensive inductors required for the circuit implementation [11]. It can also provide higher

out-of-band attenuation than standard filter structures for the same number of inductors [12]. This filter has not received much attention mainly due to the design complexity because it cannot be directly synthesized from a low-pass prototype. However, the filter's special features, i.e., lower inductance and higher out-of-band attenuation, make it an attractive option for integrated circuit implementations, where low quality factor of inductors can limit in-band insertion loss and out-of-band attenuation. This filter can be embedded into a PA so that the large out-of-band attenuation improves efficiency by providing reactive load impedance in the second-harmonic frequency band, while the minimum-inductance feature is useful in low-loss and compact chip area implementation.

In the following, we develop a new design approach for the minimum-inductance BPF, considering bandwidth, in-band insertion loss, and out-of-band attenuation specifications, while investigating effects of limited quality factor of on-chip inductors.

A. Bandwidth

The output matching network should transform the load impedance R_L into the optimum load resistance of the transistor R_{opt} over the bandwidth $\omega_L \leq \omega \leq \omega_H$. It should provide a reactive load impedance in the second-harmonic bandwidth to maximize efficiency of the PA. We propose to use the circuit shown in Fig. 1(a) as the output matching network of the PA. It is assumed that $R_{opt} > R_L$, although the design approach can be readily extended to the $R_{opt} < R_L$ case¹. Capacitance C_1 includes the parasitic drain-source capacitance C_{ds} of the PA's output transistor while the inductance L_1 serves as the drain bias feed. It can be shown that the following conditions should be satisfied at the center of the frequency band, $\omega_c = \sqrt{\omega_L \omega_H}$, to achieve the optimum load resistance

$$X_p(\omega_c) = \pm \frac{1}{Q_o} R_{opt} \quad (1)$$

$$X_s(\omega_c) = \mp Q_o R_L, \quad (2)$$

where Q_o is the loaded quality factor of the network

$$Q_o = \sqrt{\frac{R_{opt}}{R_L} - 1}. \quad (3)$$

Assuming $C_1 = C_{ds}$, using (1) with a plus sign and $X_p(\omega) = L_1 \omega / (1 - L_1 C_1 \omega^2)$, L_1 is derived as

$$L_1 = \frac{R_{opt}}{\omega_c} \frac{1}{Q_o + Q_T}, \quad (4)$$

where $Q_T = R_{opt} C_{ds} \omega_c$ is quality factor of the transistor optimum load impedance at center of the band. Using the circuit of Fig. 1(a), reactance $X_s(\omega)$ is derived as

$$X_s(\omega) = \frac{(\omega/\omega_s)^2 - 1}{1 - (\omega/\omega_o)^2} \frac{1}{\omega C_3} \quad (5)$$

which acts as an open-circuit at $\omega_o = 1/\sqrt{L_2 C_2}$ and as a short-circuit at $\omega_s = 1/\sqrt{L_2(C_2 + C_3)}$. By choosing $\omega_o =$

¹In the case of $R_{opt} < R_L$, the network should be modified to include a parallel branch with the load resistance, which has the same circuit topology as the series branch.

Fig. 1. Output matching network of the PA: (a) circuit schematic, (b) equivalent circuit for efficiency calculation, (c) equivalent circuit for out-of-band attenuation calculation.

$2\omega_c$, an almost reactive impedance composed of $L_1 \parallel C_1$ is achieved at the second-harmonic band, which is required to achieve high efficiency. Moreover, ω_s can be adjusted within $\omega_c < \omega_s < \omega_o$ to control the bandwidth. With the chosen ω_o and ω_s , (2) with a minus sign and (5) can be used to determine C_3 , C_2 , and L_2 as follows

$$C_3 = \frac{1 - (\omega_c/\omega_s)^2}{1 - (\omega_c/\omega_o)^2} \frac{1}{\omega_c Q_o R_L} \quad (6)$$

$$C_2 = \frac{C_3}{(\omega_o/\omega_s)^2 - 1} \quad (7)$$

$$L_2 = \frac{1}{C_2 \omega_o^2}. \quad (8)$$

The circuit power transfer function (transducer power gain) can be derived using Fig. 1(a) and (4)–(8), resulting in

$$G_T(\omega) = \frac{P_{out}}{P_{in}} = \frac{4R_{opt}}{R_L} |A_v(\omega)|^2, \quad (9)$$

where $A_v(\omega)$ is the voltage transfer function derived as

$$A_v(\omega) = \frac{Z_p R_L}{(R_L + Z_s)(R_{opt} + Z_p) + Z_p R_{opt}}, \quad (10)$$

with

$$Z_p(\omega) = \frac{j(\omega/\omega_c)}{Q_o + Q_T[1 - (\omega/\omega_c)^2]} R_{opt} \quad (11)$$

$$Z_s(\omega) = -j \frac{k_o^2 - 1}{k_s^2 - 1} \frac{k_s^2 - (\omega/\omega_c)^2}{k_o^2 - (\omega/\omega_c)^2} \frac{\omega_c}{\omega} Q_o R_L, \quad (12)$$

and $k_s = \omega_s/\omega_c$, $k_o = \omega_o/\omega_c$. In Fig. 2(a), $G_T(\omega)$ is shown versus the normalized frequency ω/ω_c . The circuit parameters are chosen as $R_{opt} = 55\Omega$, $C_{ds} = 1$ pF (based on the GaN transistor that is used to design the PA), $f_L = 2$ GHz, $f_H = 4$ GHz, $k_o = 2$. The bandwidth increases for larger k_s , but amplitude in the stopband would also be higher. Moreover, as will be discussed, total inductance required to implement the circuit increases with k_s . For $k_s \geq 1.2$, the increase in 3-dB bandwidth is not significant, while the stopband attenuation can be much higher. We choose $k_s = 1.2$ as the optimum considering trade-offs between bandwidth, out-of-band attenuation, and total inductance. In Fig. 2(b), an effect of the loaded quality factor Q_o on the circuit transfer function is illustrated. Bandwidth decreases for larger Q_o as expected, but amplitude in the stopband would also be lower.

Fig. 2. Transfer function of the minimum-inductance BPF: (a) effect of the parameter $k_s = \omega_s/\omega_c$ (for $k_o = 2$, $Q_o = 0.32$), (b) effect of the loaded quality factor Q_o (for $k_o = 2$, $k_s = 1.2$).

B. In-Band Insertion Loss

We derive efficiency of the output matching network in terms of the circuit parameters and frequency². Using the equivalent circuit shown in Fig. 1(b), and assuming that resistances representing losses meet the conditions $R_p \gg R_{opt}$ and $R_s \ll R_L$, it can be shown that the efficiency is derived as

$$\eta_{omn} = \frac{1 - R_{opt}/R_p}{1 + R_s/R_L} \approx 1 - \frac{R_{opt}}{R_p} - \frac{R_s}{R_L}, \quad (13)$$

in which the two terms can be derived using (4)–(8) as

$$\frac{R_{opt}}{R_p} = \frac{Q_o + Q_T}{Q_{L1}} \frac{\omega_c}{\omega} \quad (14)$$

²The insertion loss can also be derived from $G_T(\omega)$ given by (9). However, more intuitive results can be achieved based on efficiency of the network.

Fig. 3. Efficiency of the minimum-inductance BPF for different quality factors of the inductor and for two impedance transformation ratios: (a) $R_{opt}/R_L = 1.1$, (b) $R_{opt}/R_L = 1.5$. ($k_s = 1.2$ and $k_o = 2$ are assumed.)

$$\frac{R_s}{R_L} \approx \frac{(k_o^2 - k_s^2)(k_o^2 - 1)}{k_s^2 - 1} \frac{\omega/\omega_c}{[k_o^2 - (\omega/\omega_c)^2]^2} \frac{Q_o}{Q_{L2}} \quad (15)$$

where Q_{L1} and Q_{L2} denote quality factors of the inductors. The efficiency degrades for higher impedance transformation ratios and can be improved using inductors with higher quality factors. In Fig. 3, the efficiency is shown versus frequency for different $Q_{L1,L2}$ and impedance transformation ratios.

Using (13)–(15) with $k_o = 2$ and $k_s = 1.2$, the efficiency of the output matching network is derived as

$$\eta_{omn}(\omega_c) \approx 1 - \frac{Q_o + Q_T}{Q_{L1}} - 1.94 \frac{Q_o}{Q_{L2}}, \quad (16)$$

which can be used to estimate that, for example for $Q_L = 20$ and $R_{opt}/R_L = 1.1$, the efficiency is 90%.

C. Out-of-Band Attenuation

In a merged PA-BPF circuit, high out-of-band attenuation is required to suppress the second-harmonic distortion and also to present a reactive impedance to the transistor in the second-harmonic band in order to achieve high efficiency. As shown in Fig. 1(c), the drain current contains fundamental and harmonic components. The network ability to attenuate the second-harmonic components can be evaluated using the following parameter

$$A(\omega) = \frac{G_T(2\omega)}{G_T(\omega)} \quad \omega_L \leq \omega \leq \omega_H, \quad (17)$$

where G_T is captured by (9), while Z_p and Z_s are given by

$$Z_p(\omega) = \frac{j(\omega/\omega_c)R_{opt}}{Q_o + Q_T[1 - (\omega/\omega_c)^2] + j(Q_o + Q_T)/Q_{L1}}, \quad (18)$$

$$Z_s(\omega) = \left[\frac{\alpha_1(\omega/\omega_c)}{1/Q_{L2} - j[1 - (\omega/\omega_o)^2]} - j\alpha_2(\omega_c/\omega) \right] Q_o R_L, \quad (19)$$

Fig. 4. Effect of limited quality factor of the inductors on transfer function of the minimum-inductance BPF: (a) $R_{opt}/R_L = 1.1$, (b) $R_{opt}/R_L = 1.5$. ($k_s = 1.2$ and $k_o = 2$ are assumed.)

with $\alpha_1 = (k_o^2 - k_s^2)(k_o^2 - 1)/k_o^4(k_s^2 - 1)$ and $\alpha_2 = k_s^2(k_o^2 - 1)/k_o^2(k_s^2 - 1)$. It is noted that the attenuation is dependent on the inductors' quality factor Q_{L1} , Q_{L2} , parameters Q_o , Q_T , k_s , k_o , and normalized frequency ω/ω_c . The maximum attenuation is limited by quality factor of the inductors. Fig. 4 illustrates the effect of inductors' limited quality factor on in-band insertion loss and second-harmonic attenuation.

For a practical range of the circuit parameters, it can be shown that

$$A(\omega_c) \propto \frac{1}{Q_{L2}^2}, \quad (20)$$

which indicates that Q_{L2} has a dominant effect on the attenuation, as intuitively expected from the resonance of $L_2||C_2$ network in Fig. 1(a) at $2\omega_c$. The attenuation is improved by $-20 \log_{10}(Q_{L2})$, leading to 6 dB and 3.5 dB improvements by increasing Q_{L2} from 10 to 20 and 20 to 30, respectively. It is noted that these results are consistent with Fig. 4.

D. Comparison With Standard BPF

We compare the single-section minimum-inductance BPF of Fig. 1(a) with a standard BPF, where X_p is a parallel $L_1||C_1$ network and X_s a series L_2-C_2 network. In this case, the difference between the minimum-inductance and standard BPF networks is an extra capacitor (C_2) in parallel with the inductor

Fig. 5. Comparison of transfer functions of the minimum-inductance and standard BPFs ($k_s = \omega_s/\omega_c$).

of the series branch. The design equations (1)–(4) are still valid, but the series reactance is modified as

$$X_s(\omega) = \frac{(\omega/\omega_s)^2 - 1}{\omega C_2}, \quad (21)$$

where $\omega_s = 1/\sqrt{L_2 C_2}$ is a short-circuit frequency of the series reactance. Using (2) with a minus sign and (21), C_2 is derived as

$$C_2 = \frac{1 - (\omega_c/\omega_s)^2}{\omega_c Q_o R_L}, \quad (22)$$

while $L_2 = 1/C_2 \omega_s^2$. It is noted that the series network only provides a short-circuit that can be used to adjust the bandwidth, while the minimum-inductance BPF provides an extra open-circuit which can be chosen to suppress the second-harmonic components.

In Fig. 5, transfer function of the two BPF structures are compared. The minimum-inductance BPF can provide a notch at $2\omega_c$, which is essential in achieving high efficiency and second-harmonic suppression. The standard BPF however requires a multi-section network to meet these conditions.

It is interesting to compare the total inductance required to implement the two BPF circuits. For the standard BPF, using (3), (4), (22), and $L_2 = 1/C_2 \omega_s^2$, the total inductance is derived as

$$L_{tot, std} = \left[\frac{1 + Q_o^2}{Q_o + Q_T} + \frac{Q_o}{k_s^2 - 1} \right] \frac{R_L}{\omega_c}. \quad (23)$$

Similarly, using (4)–(8), for the minimum-inductance BPF it can be shown that

$$L_{tot, min} = \left[\frac{1 + Q_o^2}{Q_o + Q_T} + \frac{(k_o^2 - k_s^2)(k_o^2 - 1)Q_o}{k_o^4(k_s^2 - 1)} \right] \frac{R_L}{\omega_c}. \quad (24)$$

In both cases, the total inductance increases by Q_o (impedance transformation ratio R_{opt}/R_L). In Fig. 6, the ratio $L_{tot, min}/L_{tot, std}$ is shown versus Q_o . The total inductance can be much smaller in the minimum-inductance BPF, especially for large Q_o . The difference between (23) and (24) is in the second term in the brackets, which for typical value of $k_o = 2$ and $k_s = 1.2$, is $0.48\times$ lower in the minimum-inductance BPF.

The efficiency of the standard BPF can be derived as (13), with the same R_{opt}/R_p , but R_s/R_L modified as $R_s/R_L = (\omega/\omega_c)/(k_s^2 - 1)Q_o/Q_{L2}$. For $k_s = 1.2$, this simplifies to

Fig. 6. Ratio of total inductance in the minimum-inductance and standard BPFs for different values of parameter $k_s = \omega_s/\omega_c$. The total inductance can be reduced by up to 40% using the minimum-inductance BPF.

Fig. 7. Comparison of theoretical (solid lines) and simulation results (markers). The insertion loss of minimum-inductance BPF is calculated using (16), while the inductance ratio is derived using (23) and (24). Simulation results are obtained using circuits designed and optimized in an integrated GaN-on-SiC process.

$2.27Q_o/Q_{L2}$ at the center of the band, which is larger than that of the minimum-inductance BPF ($1.94Q_o/Q_{L2}$). Therefore, the minimum-inductance BPF provides slightly higher efficiency, especially for large Q_o and low Q_{L2} .

A comparison of theory and simulation results is shown in Fig. 7. Theoretical insertion loss of the minimum-inductance BPF is calculated using (16), while the inductance ratio is derived using (23) and (24). Simulation results are obtained using circuits designed and optimized in an integrated GaN-on-SiC process. Good agreement between theory and simulations validates the developed approach.

In Fig. 8, performance of two output matching networks realized using single-section standard and minimum-inductance BPF are compared. The minimum-inductance network provides $0.59\times$ lower total inductance and 14 dB higher out-of-band attenuation, with slightly lower in-band insertion loss. The realized load impedance using the minimum-inductance network is closer to edge of the Smith chart in the second-harmonic frequency band, resulting in higher efficiency of the PA.

E. High-Order Network

For large impedance transformation ratios, a high-order matching network can provide wider bandwidth and lower insertion loss. A general n -section minimum-inductance BPF is shown in Fig. 9(a), where all sections have the same circuit

Fig. 8. Comparison of the output matching network performance realized using the single-section (a) standard BPF, and (b) minimum-inductance BPF. The circuits are realized using an integrated GaN-on-SiC process. The minimum-inductance BPF provides $0.59\times$ lower total inductance, 14 dB higher out-of-band attenuation (maximum A is reported), with slightly lower in-band insertion loss (IL).

structure except for the last section which is modified to a parallel LC network so that it can absorb the transistor's output parasitic capacitance and provide the drain bias feed³. This high-order minimum-inductance network can also provide higher out-of-band attenuation. An approach to maximize its bandwidth is to choose intermediate resistances such that all sections have the same impedance transformation ratio:

$$\frac{R_{in,1}}{R_L} = \dots = \frac{R_{in,k}}{R_{in,k-1}} = \dots = \frac{R_{opt}}{R_{in,n-1}}, \quad (25)$$

which can be used to derive the input resistance of the section k as

$$R_{in,k} = \left(\frac{R_{opt}}{R_L} \right)^{\frac{k}{n}} R_L. \quad (26)$$

Moreover, the loaded quality factor of all sections is given by

$$Q_o = \sqrt{\left(\frac{R_{opt}}{R_L} \right)^{\frac{1}{n}} - 1}, \quad (27)$$

which is lower than that of a single-section network given by (3). Equivalent circuit of each network section is shown in Fig. 9(b). The impedance matching conditions are given by (1) and (2), with load $R_{in,k-1}$ and input resistance of $R_{in,k}$. Both series and parallel reactances are of the form (12), where $-Q_o R_L$ is replaced with $-Q_o R_{in,k-1}$ in the series reactance and $R_{in,k}/Q_o$ in the parallel reactance. Thus, the circuit has two pass frequencies, $\omega_{o,p}$, $\omega_{s,s}$, and two

³This network is used in the case $R_{opt} > R_L$. The network should be modified such that it has a section in parallel with the load resistance for the case $R_{opt} < R_L$. It can be shown that (1)–(3) can still be used in this case provided that R_{opt} and R_L be interchanged.

stop frequencies, $\omega_{o,s}$, $\omega_{s,p}$. The stop frequencies can control lower and upper stopbands of the filter, e.g., $\omega_{o,s} = 2\omega_c$ and $\omega_{s,p} = 0.5\omega_c$, while the pass frequencies can be used to control the bandwidth, e.g., by considering two parameters $k_{op} = \omega_{o,p}/\omega_c$ and $k_{ss} = \omega_{s,s}/\omega_c$. It can be shown that $k_{op} = k_{ss} = 1.2$ results in the optimum design conditions. In Fig. 10, a transfer function of the circuit is shown, where the effect of inductors' quality factor on the in-band insertion loss and out-of-band attenuation is illustrated.

The efficiency of multi-section network can be derived as follows

$$\eta_{omn} = \prod_{k=1}^n \frac{1 - R_{in,k}/R_{p,k}}{1 + R_{s,k}/R_{in,k-1}} \quad (28)$$

where $R_{p,k}$ and $R_{s,k}$ respectively denote equivalent losses of the parallel and series reactances of the section k . In this case, $R_{in,k}/R_{p,k}$ and $R_{s,k}/R_{in,k-1}$ are derived in the form $a_k Q_o / Q_L$, where a_k is a parameter dependent on the open and short frequencies of reactances $X_{p,k}$ and $X_{s,k}$. The efficiency of each section is higher than that of a single-section network due to the reduced Q_o in multi-section network. However, the overall efficiency can be either higher or lower, depending on the impedance transformation ratio, number of stages, and quality factor of inductors.

The total second-harmonic attenuation can be similarly derived as

$$A(\omega) = \prod_{k=1}^n \frac{G_{T,k}(2\omega)}{G_{T,k}(\omega)}, \quad (29)$$

which can be used as another criterion for choosing the number of stages. It is noted that the attenuation of each stage is mainly limited by the quality factor of inductor in the series branch. Moreover, the chip area which is dependent on the size of inductors and their layout, is an important factor in choosing the number of filter sections.

III. TWO-TRANSISTOR AM-PM COMPENSATION

A. GaN HEMT Nonlinearity

GaN HEMT device exhibits a distinct nonlinear behavior, *soft gain compression*, which is especially detrimental for complex-modulated signals with large PAPR. The PA nonlinearity is dominated by a nonlinearity of the transistor's transconductance and parasitic capacitances [7]. The AM-PM distortion is mainly caused by nonlinear input capacitance of the transistor [13]. The input capacitance nonlinearity is composed of the gate-source capacitance nonlinearity and nonlinear feedback effect of the gate-drain capacitance, as follows

$$C_{in}(V_{in}) \approx C_{gs}(V_{in}) + (1 + g_m(V_{in})Z_L)C_{gd}, \quad (30)$$

where Z_L denotes the transistor's load impedance. We develop an approach to compensate nonlinearity of the gate-source capacitance and transconductance, mitigating AM-PM distortion of the PA.

Fig. 9. (a) General n -section minimum-inductance BPF. (b) Equivalent circuit of each filter section (except the last section which can be modeled as Fig. 1).

Fig. 10. Transfer function of the single-section minimum-inductance BPF circuit [Fig. 9(b)]. Effect of quality factor of the inductors on in-band insertion loss and out-of-band attenuation. ($R_{opt}/R_L = 1.1$, $k_{op} = k_{ss} = 1.2$, $\omega_{o,s} = 2\omega_c$, and $\omega_{s,p} = 0.5\omega_c$ are assumed.)

B. Two-Transistor Linearization

The linearization of transistor should be performed such that it would be effective over a *wide power range* in order to accommodate high-PAPR signals. There are two general approaches to the PA phase linearization: (1) using multi-transistor architectures as power cell, where nonlinearity profiles are combined such that they compensate each other's nonlinearities, e.g., parallel common-source devices [14], [15] or combined common-source and common-gate transistors [16], and (2) using a separate nonlinear circuit as pre/post-linearizer or using cascaded/parallel amplifier stages to equalize overall phase-power profile [17], [18]. The former approach has several advantages. The output and input matching networks can be designed to optimize the efficiency and bandwidth of the PA, without much concern about linearity. In the later, however, matching networks can have significant effects on the linearity of the PA, e.g., due to losses of the linearizer, variations of its phase and amplitude with frequency, phase mismatch of parallel/cascaded amplifier stages.

In CMOS PAs, input capacitance nonlinearity of NMOS transistors can be compensated using auxiliary PMOS transistors with complementary input capacitance nonlinearity behavior [19]. This technique has been used in extremely broadband PAs [20]. However, GaN processes offer only N-

channel transistors, rendering this technique ineffective. The parallel common-source transistors with different gate biased can be used to improve linearity of the GaN PA. We note that the form of nonlinearity, in both C_{gs} and g_m , is dependent on the transistor's mode of operation. For low (and zero) bias currents toward the class-C mode, nonlinearity is expansive with the input power, while it becomes compressive when the bias current is increased toward the class-A mode. As shown in Fig. 11, using two parallel transistors with unbalanced gate biases (e.g., -2.2 V and -2.6 V in this case), nonlinearity of the total average transconductance $g_{m1} + g_{m2}$ and average input capacitance $C_{in1} + C_{in2}$ can be compensated over a *wide power range*⁴. In practice, the gate biases $V_{G1,2}$ can be further fine-tuned at modulated-signal measurements to minimize the error vector magnitude (EVM) or adjacent channel leakage ratio (ACLR).

The proposed linearization is inherently broadband, considering that the load impedance in (30) is $Z_L(f) \approx R_{opt}$ across the bandwidth and C_{in} is independent of frequency. However, other effects, including deviation of the load impedance from R_{opt} , source impedance variations with frequency, and high-Q input matching [20], [21], as well as resistive second-harmonic load impedance [13], lead to imperfect linearization over the bandwidth. The gate bias setting can be further tuned at each frequency, when the whole bandwidth is not needed to be used simultaneously, in order to improve the AM-PM linearization.

IV. CIRCUIT IMPLEMENTATION

A. Output Matching Network

We use the developed design approach for a broadband 2–4 GHz PA in a 0.25- μ m GaN-on-SiC technology. The width of GaN transistor can be selected so as to achieve an optimum load resistance close to 50Ω , leading to a simplified output matching network structure with lower losses and extended bandwidth. In this design, two parallel transistors with 6×125 - μ m width and 28 V supply voltage are used to achieve 37 dBm output power over the bandwidth. Using load-pull simulations,

⁴It is possible to use a single transistor with an appropriate gate bias to mitigate the nonlinearity. However, using parallel transistors with separate biases allows to independently compensate the nonlinearity of transconductance and input capacitance, which may not be achieved at the same bias point.

Fig. 11. (a) AM-PM compensation technique using two parallel GaN transistors with compressive and expansive nonlinearity profiles (using different gate bias voltages). Simulated: (b) average transconductance, and (c) gate-source capacitance, versus input power.

R_{opt} and C_{ds} are derived as 55Ω and 1 pF , respectively⁵. The low impedance transformation ratio of 1.1 leads to a small Q_o of 0.32. The single-section network of Fig. 1(a) is therefore used as the output matching network. The inductor L_1 is derived using (4) for the given center frequency. The design parameter k_o is chosen as $k_o = 2$ so that the matching network provides an open-circuit at the second harmonic. The design parameter k_s is chosen as $k_s = 1.2$ based on the trade-off between bandwidth and out-of-band attenuation of the minimum-inductance BPF. Using (6)–(8) with $k_o = 2$ and $k_s = 1.2$, the elements $C_{2,3}$ and L_2 are determined. In this design, the circuit elements are derived as $[L_1 \ L_2] = [2.39 \ 0.97] \text{ nH}$ and $[C_1 \ C_2 \ C_3] = [1.00 \ 0.82 \ 1.45] \text{ pF}$. The inductor L_1 should also meet a minimum width based on electromigration current density limit ($16 \mu\text{m}$ in this process). It is realized as a meandered microstrip transmission line, while a spiral inductor structure with small chip area is chosen for L_2 . In this design, $Q_{L1} \approx 18$ and $Q_{L2} \approx 15$, leading to $\eta_{omn} \approx 88.7\%$ (0.52 dB insertion loss).

In Fig. 12, simulation and theoretical results of the load impedance presented to the transistor's drain as well as insertion loss of the output matching network are shown versus frequency. In 2–4 GHz, the real part of the load impedance is almost flat and equal to R_{opt} , while in the second-harmonic band it rolls off to zero. The insertion loss is 0.46–0.93 dB. The simulated minimum insertion loss is close to the theoretical insertion loss predicted by (16).

B. Input Matching Network

Design of the input matching network is less critical than that of the output matching network. The output power and efficiency are not that sensitive to the source impedance mismatch, while a moderate insertion loss can be exploited to improve bandwidth and gain flatness of the PA. We use a single-section minimum-inductance BPF with a reactance in parallel with the source impedance ($R_{S,opt} < R_S$) as the input matching network. The short-circuit frequency of the

⁵A slightly larger transistor width could be chosen to achieve a $50\text{-}\Omega$ optimum load resistance. However, as the transistor model provided by foundry has been verified for limited values of the gate widths, we chose $6 \times 125\text{-}\mu\text{m}$ width for higher accuracy.

Fig. 12. Load impedance presented to the transistor and insertion loss of the output matching network (solid lines: simulation, dashed lines: theory).

Fig. 13. Circuit schematic of the complete PA.

parallel reactance can be adjusted to achieve a reactive source impedance at the second-harmonic frequency band, $\omega_{s,p} \approx 2\omega_c$. Furthermore, the input matching network is designed to provide a moderate input matching, $|\Gamma_{in}| < -8 \text{ dB}$, but a low quality factor ($Q_{in} = |X_{in}|/R_{in}$) of 0.4–0.8 in the bandwidth to maintain low AM-PM. The insertion loss is 0.5–2.5 dB across 2.0–4.0 GHz.

C. Simulation Results

The PA circuit schematic is shown in Fig. 13 where both output and input matching networks are realized using the minimum-inductance BPFs. The elements $R_c||C_c$ and R_d are used to improve low-frequency stability and prevent odd-mode oscillations [10]. Simulated frequency response of the

Fig. 14. Simulated normalized gain frequency response.

Fig. 15. Simulated AM-AM and AM-PM characteristics across 2.0–4.0 GHz.

normalized gain is shown in Fig. 14. The second-harmonic rejection is better than 20 dB across 5.4–8.0 GHz. The maximum attenuation of 57.3 dB is achieved at 6.2 GHz.

Simulation results indicate 37.1–38.5 dBm output power, 45–61% drain efficiency (DE), 42–58% PAE, and 13.1–14.5 dB power gain over the bandwidth of 2.0–4.0 GHz, at a fixed input power of 24 dBm. In Fig. 15, AM-AM and AM-PM distortion characteristics are shown across 2.0–4.0 GHz. The AM-PM remains smaller than 6.4° up to 37 dBm output power (≈ 2 –4 dB gain compression), with 4° maximum variations over the bandwidth. As expected, the AM-PM characteristic changes with frequency but remains close to the results obtained using the optimum bias setting⁶.

V. MEASUREMENT RESULTS

The PA is implemented in a 0.25- μ m GaN-on-SiC technology from WIN Semiconductors (Fig. 16). The chip measures

⁶The linearity simulation results are provided to demonstrate operation of the proposed linearization technique. The accuracy of transistors' CW nonlinearity model provided by foundry and its sensitivity to PVT variations cannot be verified for prediction of the modulated-signal measurement results.

Fig. 16. Chip micrograph (1.8 mm $\times$ 1.8 mm).

Fig. 17. Measured gain and PAE versus output power.

1.8 mm $\times$ 1.8 mm, which shows a compact fully integrated realization for the 2–4 GHz band. The circuit is biased at supply voltage of 28 V and gate voltages of -2.2 V, -2.6 V. The DC current varies from 40 mA to 400 mA. The PA chip is attached to a test PCB and is wire-bonded to metal traces for measurements.

A. CW Measurements

The measured gain and PAE versus output power are shown in Fig. 17. The small-signal gain reads 13.0–17.2 dB across 2.0–4.0 GHz, while the large-signal gain is 11.3–13.4 dB at 1.5–3.5 dB gain compression. The maximum PAE of 47.9% is obtained with 37.5 dBm output power (3.5 dB gain compression) at 2.0 GHz. The saturated output power, DE, and PAE versus frequency are shown in Fig. 18 at a fixed 27 dBm input power (saturation). The PA provides 35.1–38.9 dBm output power, 45–61% DE, and 40–55% PAE in 2.0–4.0 GHz. The measured output power and efficiency are close to simulation results in 1.5–3.4 GHz, but degrade slightly at higher end of

Fig. 18. Measured and simulated saturated output power, DE, and PAE versus frequency at a fixed input power of 27 dBm.

Fig. 19. Measured and simulated second harmonic rejection versus fundamental output power.

the band, mainly due to inaccuracies of the transistor large-signal model and process variations.

The measured and simulated second harmonic rejection versus fundamental output power are shown in Fig. 19. The highest second harmonic rejection is measured at 3.0 GHz (with the maximum of 47.6 dB). This is consistent with the simulation results shown in Fig. 14 which indicates a dip around 6 GHz. The measured second harmonic rejection is typically within ≈ 20 –40 dB across 2.0–4.0 GHz. The large deviation of the measurement and simulation results at 4.0 GHz is attributed to drop in the fundamental output power (Fig. 18). It should be mentioned that due to high input/output power levels of the PA, it is connected to attenuators to protect the test equipment. Therefore, filtering characteristics of the circuit could not be derived by measurement of the S-parameters.

Fig. 20. Measured AM-PM and AM-AM characteristics for 100-MHz 256-QAM signal with 7.2-dB PAPR at 2.4 GHz.

TABLE I
SUMMARY OF MODULATED-SIGNAL MEASUREMENTS AT 2.4 GHz.

Modulation	BW _m (MHz)	P _{o,avg} (dBm)	PAE _{avg} (%)	EVM _{rms} (dB)
256-QAM	100	30.1	19.5	−32.0
256-QAM	100	31.8	24.8	−30.2
256-QAM	200	31.3	21.4	−29.6
64-QAM	100	30.7	24.5	−33.2
64-QAM	100	32.5	29.7	−30.5
64-QAM	100	33.6	33.4	−26.7

B. Modulated-Signal Measurements

The modulated-signal measurements are performed using 64-QAM and 256-QAM signals. Measured AM-AM and AM-PM characteristics, output constellation, and spectrum for a 100-MHz 256-QAM signal with 7.2-dB PAPR are shown in Figs. 20 and 21. EVM_{rms} of 2.9% (−30.7 dB) and ACLR of −35.8/−35.7 dBc are achieved without any predistortion. This linearity performance can be acceptable, depending on requirements of the target applications. If higher linearity is required, the EVM and ACLR can be respectively improved to 0.5% (−46.0 dB) and −46.4/−46.8 dBc using digital predistortion (DPD). The average output power (P_{o,avg}) and average DE/PAE are 31.8 dBm and 27.3%/24.8%, respectively. For a 100-MHz 64-QAM signal with 8.0-dB PAPR, EVM_{rms} and ACLR are measured as 3.1% (−30.2 dB) and −35.8/−36.1 dBc (without DPD), while P_{o,avg} and PAE_{avg} are respectively 32.7 dBm and 31%. A summary of the modulated signal measurements is given in Table I, where effects of output power, modulation order, and bandwidth on EVM and PAE are tabulated.

In Fig. 22, measured EVM_{rms}, ACLR (average of lower and upper channels), and DE_{avg} are shown versus average output power across the 2.0–4.0 GHz band. EVM and ACLR degrade at the higher end of the band, which is consistent with the output power drop in Fig. 18. The worse linearity at higher frequencies can be attributed to imperfect linearization arising from parasitic elements and load impedance variations with frequency.

The performance of this PA is compared with broadband highly efficient fully integrated GaN PAs in Table II. The

TABLE II
COMPARISON OF BROADBAND FULLY INTEGRATED GAN PAs

	This Work	[22]	[23]	[24]	[25]	[26]	[27]
BW (GHz)	2.0–4.0	1.0–8.0	6.4–8.3	6.0–18.0	4.9–5.9	6.8–7.2	4.6–6.0
FBW (%)	70.7	247.5	26.1	115.5	18.6	5.7	26.6
P _o (dBm)	35.1–38.9	39.4–40.6	36–36.6	44.8–47.2	37–37.7	37.7–38.0	34.7–36.2
DE (%)	45–61	30–47	40–50	14–33	48–55	62–67	45–54
PAE (%)	40–55	30–47	37–46	13–30	48–55	58–64	42–52
Gain (dB)	11.3–13.4	24.4–26	10–12	9.8–12.2	28.5–31.7	12.2–13.5	12.2–13.4
Modulation	64/256/256-QAM	—	256-QAM	—	256-QAM	256-QAM	256-QAM
BW _m (MHz)	100/100/200	—	7	—	80	60	100
PAPR (dB)	8.0/7.2/7.2	—	7.4	—	11.25	7.0	8.2
f _c (GHz)	2.4	—	7	—	5.7	7.0	5.0
EVM _{rms} (dB)	−26.7/−32.0/−29.6	—	—	—	−32	—	−28
P _{o,avg} (dBm)	33.6/30.1/31.3	—	28.7	—	30.6	32	31.1
PAE _{avg} (%)	33/19/21	—	26	—	27	30	35
Area (mm ²)	3.2	11.7	7.8	47.1	4.7	9.0	2.2
Process (μm)	0.25	0.15	0.25	0.18	0.25	0.25	0.25

Fig. 21. Measured output constellation and output spectrum for 100-MHz 256-QAM signal with 7.2-dB PAPR at 2.4 GHz. The average output power is 31.8 dBm, average DE /PAE are 27.3/24.8%, while PAPR of the output signal is 5.6 dB.

Fig. 22. Measured EVM, ACLR, and average DE versus average output power (without DPD) for a 100-MHz 256-QAM signal with 7.2-dB PAPR at 2.4 GHz. Fixed gate bias voltages are used for all frequencies, while lower EVM and ACLR can be achieved by fine-tuning gate bias voltages at each frequency.

proposed PA features high efficiency over a broad fractional bandwidth (FBW) and reports a very compact chip area for the targeted frequency range, resulting from the used minimum-

inductance BPF matching network. A high average PAE of 33% with EVM < −25 dB are achieved for 64-QAM signal. The low EVM values measured for 256-QAM signals with

up to 200 MHz modulation bandwidth are promising for high data rate 5G applications.

VI. CONCLUSION

We present a design approach for broadband fully integrated power amplifiers (PAs) merged with minimum-inductance BPF network using two-transistor architecture for AM-PM compensation. Using a new theory developed for minimum-inductance BPF, it is shown that this network, compared to the standard BPF, can provide higher out-of-band attenuation, lower in-band insertion loss, and can be realized using substantially smaller total inductance. Furthermore, using two parallel transistors with compressive and expansive nonlinearity profiles, AM-PM distortion of the PA can be compensated. A fully integrated 0.25- μm GaN-on-SiC PA prototype provides 45–61% drain efficiency and 3.2–7.7 W output power across 2.0–4.0 GHz (70.7%) bandwidth. For a 100-MHz 256-QAM signal with 7.2 dB PAPR, EVM_{rms} of -32.0 dB is achieved at 1 W average output power.

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