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Combined Effect of Loop Delay and Reference Clock Jitter in First-Order Digital Bang-Bang Phase-Locked Loops

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Abstract—Recently, several digital phase-locked loops (DPLLs) have been demonstrated to achieve the jitter performance of traditional charge-pump-based analog PLLs. This paper is concerned with a class of DPLLs employing a binary-quantized phase detector, referred to as bang-bang PLLs (BBPLLs). They are widely used in clock and data recovery circuits and have recently been implemented as digital BBPLLs for high-bandwidth synthesis. Given that a DPLL implementation typically suffers from (excess) loop delay, this paper investigates the combined effect of loop delay and reference clock jitter in a first-order digital BBPLL. To statistically characterize the loop's timing jitter we formulate it as a discrete-time vector Markov process and numerically solve the associated Chapman-Kolmogorov equation. This allows us to compute the timing jitter probability density function in steady-state and to evaluate the jitter performance (timing offset and RMS timing jitter) for varying loop detuning, RMS reference clock jitter and loop delay.

I. INTRODUCTION

Analog phase-locked loops (PLLs) based on the predominant charge-pump architecture continue to achieve the high performance needed in modern applications. However, the benefits gained from a digital implementation, such as scalability and easy redesign, have resulted in several (all-)digital PLLs that achieve the performance of their analog counterparts (see [1] and references therein). A simplified block diagram of a digital PLL (DPLL) used for integer- N frequency synthesis is shown in Fig. 1. Instead of the charge-pump-based loop filter driving the voltage-controlled oscillator in an analog PLL, a DPLL employs a digital loop filter (DLF) which tunes the frequency of a digitally controlled oscillator (DCO) by a digital control word. Advantages of a DLF include compact circuit realization and easy programmability of loop dynamics. Because the loop filter is digital, the phase detector is a time-to-digital converter (TDC) [1], which directly produces a digital word proportional to the time (phase) difference between the reference clock and the divided clock.

This paper is concerned with a class of DPLLs whose TDC has a resolution of 1-bit, giving it the name binary (or bang-bang) phase detector (BPD). The resulting class of bang-bang PLLs (BBPLLs) is widely used in clock and data recovery circuits due to its high-speed capabilities [2]. Recently, a digital BBPLL (DBBPLL) has been demonstrated to be suitable for high-bandwidth synthesis [3], and will be the focus of our study. Typical in a DPLL implementation is (excess) loop delay due to the latency of the digital building blocks and, in particular, the arithmetic operations performed by the DLF (pipelining). Loop delay is known to degrade the loop's jitter performance and stability margin [4]. For a wide class of DPLLs, the loop can be linearized in steady state, and linear transfer functions can then be applied to analyze the effect of loop delay on the stability margin [4]. In a DBBPLL, however, the hard nonlinearity introduced by the BPD makes this linearization no longer valid, and a nonlinear analysis is needed to obtain stability conditions [5] or to describe limit cycles [6]. Although the BPD may be linearized in the presence of

Fig. 1. Digital PLL for integer- N frequency synthesis.

reference clock jitter [7], the highly nonlinear behavior of the timing jitter remains unexplained.

In our recent work [8] we have investigated a first-order DBBPLL with Gaussian reference clock jitter by modeling the timing jitter process as a discrete-time Markov process. The analysis showed that the timing jitter in steady state is non-Gaussian and is Gaussian-like only for some RMS clock jitter values. The main contribution of the present paper is to extend that approach and investigate the combined effect of loop delay and reference clock jitter in a first-order DBBPLL. In particular we model the timing jitter process as a discrete-time vector Markov process and derive the associated Chapman-Kolmogorov (CK) equation. The numerical solution of this equation allows us to compute the timing jitter PDF in steady state and to investigate how varying RMS clock jitter and loop detuning affects the timing jitter performance for different loop delays.

II. FIRST-ORDER DBBPLL MODEL

A time-domain model of a first-order DBBPLL with loop delay is shown in Fig. 2 [5], [9]. Since a BPD (1-bit TDC) can be implemented as a sampling register in which the divided clock samples the reference clock [3], it is sufficient to consider only the time instants of the rising clock edges, denoted by t_r and t_d , respectively. The bit stream from the BPD, whose binary quantization operation is modeled by the signum function sgn , is fed into the DLF which, for our first-order loop, consists of a proportional path with gain K_P . The loop delay due to the sources mentioned in Sec. I is modeled by the delay element of D reference clock cycles. The DCO is considered as a linear block, with the free-running clock period T_{v0} and the period gain constant K_T . The feedback divider divides the high-frequency DCO clock by N , resulting in a gain N in the time domain. A more comprehensive model of a DBBPLL is given in [9].

The quantity of interest in our study is the timing jitter Δt between the reference clock and the divided clock. Because updating the BPD output and clocking the DLF occurs only every divided clock cycle, the dynamics of Δt can be described at discrete time instants $n = 0, 1, \dots$, and is governed by the difference equation [5]

$$\Delta t(n+1) = \Delta t(n) + T_r(n) - NT_{v0} - NK_P K_T \text{sgn} \Delta t(n-D) \quad (1)$$

where $\Delta t(n) = t_r(n) - t_d(n)$ is the timing jitter at the n th sampling

Fig. 2. Time-domain model of a first-order DBBPLL with loop delay.

instant, $T_r(n)$ is the n th reference clock period, and $\text{sgn } x = 1$ for $x \geq 0$ and $\text{sgn } x = -1$ for $x < 0$. Following the approach in [10], reference clock jitter can be modeled by relating each region of the reference oscillator's phase noise profile to a corresponding time domain description. In particular, the white electronic noise ($1/\omega^0$ -region) corresponds to non-accumulative jitter in the time domain and has been considered in [11]. In the present paper we focus on the upconverted thermal noise ($1/\omega^2$ -region) which corresponds to accumulative jitter (timing wander) in the time domain and can be visualized as a reference oscillator whose nominal clock period T_{r0} varies randomly from cycle to cycle. Thus, we write the n th reference clock period as $T_r(n) = T_{r0} + \tau(n)$, where $\tau(n)$ is a zero-mean random variable with variance σ_τ^2 modeling the random variation of the n th clock period. Substituting this expression into (1) and normalizing by the quantization step $NK_P K_T$ of the divided clock period gives the first-order stochastic difference equation

$$u(n+1) = u(n) + m - \text{sgn } u(n-D) + \xi(n) \quad (2)$$

where $u(n) = \Delta t(n)/(NK_P K_T)$ is the (normalized) timing jitter at the n th sampling instant and $m = (T_{r0} - NT_{v0})/(NK_P K_T)$ is the (normalized) loop detuning due to a frequency offset between the reference clock and the divided free-running DCO clock. The (normalized) jitter sequence $\{\xi(n)\}$ is assumed to be a sequence of independent and identically distributed Gaussian random variables with zero mean and variance σ^2 , such that the RMS reference clock jitter (or simply called clock jitter) $\sigma = \sigma_\tau/(NK_P K_T)$. Since the loop is stable for $|m| < 1$ [5], we assume that m is either zero or, without loss of generality, an irrational number in $(0, 1)$; the latter assumption is justified since the natural tolerances in an implementation make the exact period of the reference clock and the free-running DCO clock unknown, and with probability 1 they will be irrational.

III. CHAPMAN-KOLMOGOROV EQUATION FOR A FIRST-ORDER DBBPLL WITH LOOP DELAY

In this section we derive the CK equation of a vector Markov process associated with the stochastic difference equation (2). Since the next timing jitter state $u(n+1)$ in (2) does not only depend on the current state $u(n)$ and the current value of the jitter random variable $\xi(n)$ but also on the state $u(n-D)$ in the past, the timing jitter sequence $\{u(n)\}$ is non-Markov. By introducing the variables $x_i(n) = u(n-i)$, $0 \leq i \leq D$, we can transform (2) into the set of first-order stochastic difference equations

$$\begin{aligned} x_0(n+1) &= x_0(n) + m - \text{sgn } x_D(n) + \xi(n) \\ x_1(n+1) &= x_0(n) \\ &\vdots \\ x_D(n+1) &= x_{D-1}(n). \end{aligned} \quad (3)$$

By defining the state vector $\mathbf{x} := (x_0, \dots, x_D)$, the sequence $\{\mathbf{x}(n)\}$ governed by (3) forms now a discrete-time, continuous-valued vector Markov process of dimension $D+1$. Let $p_n(\mathbf{x}|\mathbf{x}(0))$ be the joint PDF of the state vector $\mathbf{x}(n)$ at time instant n conditioned on the initial state vector $\mathbf{x}(0)$. Since the vector process is Markov, $p_n(\mathbf{x}|\mathbf{x}(0))$ satisfies the (vector) CK equation [12]

$$p_{n+1}(\mathbf{x}|\mathbf{x}(0)) = \int_{-\infty}^{\infty} dz_D \cdots \int_{-\infty}^{\infty} dz_0 q_n(\mathbf{x}|\mathbf{z}) p_n(\mathbf{z}|\mathbf{x}(0)) \quad (4)$$

where $q_n(\mathbf{x}|\mathbf{z})$ is the joint transition PDF of $\mathbf{x}(n+1)$ given $\mathbf{x}(n) = \mathbf{z} := (z_0, \dots, z_D)$. Since at each time instant n , the jitter random variable $\xi(n)$ in (3) is independent of $\mathbf{x}(n)$, the joint transition PDF $q_n(\mathbf{x}|\mathbf{z})$ in (4) is given by

$$\begin{aligned} q_n(\mathbf{x}|\mathbf{z}) &= \frac{1}{\sqrt{2\pi}\sigma} \exp[-(x_0 - z_0 - m + \text{sgn } z_D)^2/(2\sigma^2)] \\ &\times \prod_{i=0}^{D-1} \delta(x_{i+1} - z_i) \end{aligned} \quad (5)$$

where $\delta(\cdot)$ is the Dirac delta function. The independence of n in (5) means that the vector Markov process is time-homogeneous. By substituting (5) into (4) and integrating with respect to z_0 we obtain

$$\begin{aligned} p_{n+1}(\mathbf{x}) &= \int_{-\infty}^{\infty} dz_D K(x_0, x_1, z_D) \int_{-\infty}^{\infty} dz_{D-1} \cdots \int_{-\infty}^{\infty} dz_1 \\ &\times \prod_{i=1}^{D-1} \delta(x_{i+1} - z_i) p_n(x_1, z_1, \dots, z_D) \end{aligned} \quad (6)$$

where the kernel $K(x_0, x_1, z_D)$ is given by

$$K(x_0, x_1, z_D) = \frac{1}{\sqrt{2\pi}\sigma} \exp[-(x_0 - x_1 - m + \text{sgn } z_D)^2/(2\sigma^2)] \quad (7)$$

and conditioning on $\mathbf{x}(0)$ is understood throughout. Integrating (6) with respect to $z_1, \dots, z_{D-1}$ yields the final form of the CK equation

$$p_{n+1}(\mathbf{x}) = \int_{-\infty}^{\infty} K(x_0, x_1, z_D) p_n(x_1, \dots, x_D, z_D) dz_D \quad (8)$$

which, together with the joint PDF $p_0(\mathbf{x})$ of the initial state vector $\mathbf{x}(0)$, gives a complete statistical description of the vector Markov process $\{\mathbf{x}(n)\}$. In practice we are interested in the behavior of the timing jitter in steady state, i.e., after sufficiently long time. Let

$$p(\mathbf{x}) = \lim_{n \rightarrow \infty} p_n(\mathbf{x}) \quad (9)$$

be the joint steady-state PDF of the vector Markov process. Assuming that a unique $p(\mathbf{x})$ exists, it follows from (8) that $p(\mathbf{x})$ satisfies

$$p(\mathbf{x}) = \int_{-\infty}^{\infty} K(x_0, x_1, z_D) p(x_1, \dots, x_D, z_D) dz_D \quad (10)$$

which is independent of $\mathbf{x}(0)$. The steady-state timing jitter PDF, i.e., the PDF of the timing jitter sequence $\{u(n)\}$ in steady state, can be obtained from $p(\mathbf{x}) = p(x_0, x_1, \dots, x_D)$ by marginalization as

$$p(u) = p(x_0) = \int_{-\infty}^{\infty} dx_D \cdots \int_{-\infty}^{\infty} dx_1 p(x_0, x_1, \dots, x_D). \quad (11)$$

Similar to the case $D=0$ in [8], the numerical integration of (8) requires splitting up the domain of integration, since the signum function in (7) makes the integrand discontinuous in z_D . Thus, by dividing the domain of integration into the two disjoint intervals

Fig. 3. Comparison of the steady-state timing jitter PDF $p(u)$ obtained numerically (solid) and estimated from simulation (histogram). Parameters: $m \approx 0.8168$ (irrational) and $\sigma = 0.3$.

$(-\infty, 0)$ and $[0, \infty)$, over each of which the integrand is continuous in z_D , we can write (8) as

$$p_{n+1}(\mathbf{x}) = K^-(x_0, x_1) \int_{-\infty}^0 p_n(x_1, \dots, x_D, z_D) dz_D + K^+(x_0, x_1) \int_0^{\infty} p_n(x_1, \dots, x_D, z_D) dz_D \quad (12)$$

where

$$K^\pm(x_0, x_1) = \frac{1}{\sqrt{2\pi}\sigma} \exp[-(x_0 - x_1 - m \pm 1)^2 / (2\sigma^2)]. \quad (13)$$

IV. NUMERICAL AND SIMULATION RESULTS

This section compares the results obtained by numerically solving the CK equation (12) with the results obtained from Monte-Carlo simulation of the stochastic difference equation (2). For the Monte-Carlo simulation, 10^7 realizations of length 100 were generated, and the statistics (histogram, mean, variance) were computed for the last time instant, except for the low-jitter case which will be discussed in Sec. IV-C. For the recursive numerical integration of (12), the joint PDF was defined as a $(D+1)$ -dimensional array, with the length of each dimension (the domain of integration) equal to the difference between the maximum and minimum bin number of the histogram. The initial state vector $\mathbf{x}(0)$ was assumed to be zero, giving an initial joint PDF $p_0(\mathbf{x}) = \delta(\mathbf{x})$. The joint steady-state PDF defined in (9) was assumed to have been obtained when the maximum absolute difference between two consecutive joint PDFs in the iteration was less than a predefined amount. The steady-state timing jitter PDF was then obtained from the joint steady-state PDF using (11). Note that despite the generality of the CK equation (12), numerical results will be presented only for $D=1$ and $D=2$, and compared with those for $D=0$ in [8]. All plots show good agreement between numerical and simulation results, except when either of m , σ or D was large, in which case numerical inaccuracies were significant.

A. Effect of Loop Delay on the Steady-State Timing Jitter PDF

An example of a steady-state timing jitter PDF for a single-delay loop ($D=1$) is shown in Fig. 3. The plot shows that the numerical PDF (solid) matches the estimated PDF (histogram) obtained from Monte-Carlo simulation. The shape of the PDF can be qualitatively explained as follows. If the reference clock is jitter-free, a deterministic timing jitter sequence will lie in the interval $[(1+D)(m-1), (1+D)(m+1))$ in steady state (the dashed vertical lines) and, since m is irrational, will densely fill subsets of it [5]. If the reference clock is subject to Gaussian jitter, a stochastic timing jitter sequence will be unbounded and leave this interval on both

Fig. 4. Steady-state timing jitter PDF $p(u)$ for zero loop detuning ($m=0$) and two RMS reference clock jitter values σ .

sides so that the probability mass is spread out on the real line. Since the clock jitter σ is relatively small, the deterministic and stochastic dynamics interact notably, causing the peculiar PDF shape.

The effect of loop delay on the PDF shape is further illustrated in Fig. 4 (see also Fig. 3(a) in [8]). For small clock jitter ($\sigma=0.2$), the PDFs resemble a uniform PDF, the width of which increases with D . For larger clock jitter ($\sigma=2$), the PDFs are more spread out and appear Gaussian-like. Moreover, independent of D , the PDFs are symmetric about zero since the zero detuning makes it equally likely for a stochastic timing jitter sequence to leave the steady-state interval on either side.

B. Jitter Performance: Timing Offset and RMS Timing Jitter

To evaluate the loop's timing jitter performance we computed the mean $\mu_u = Eu$ (timing offset) and the standard deviation $\sigma_u = (Eu^2 - \mu_u^2)^{1/2}$ (RMS timing jitter) of the steady-state timing jitter PDF $p(u)$, where the k th moment

$$Eu^k = \int_{-\infty}^{\infty} u^k p(u) du \quad (14)$$

and E denotes the statistical expectation operator. In the following two figures, each marker represents the result of this computation, with Eu and Eu^2 obtained from (14) using numerical integration.

Figure 5 plots the timing offset μ_u as a function of (irrational) detuning $m \in (0, 1)$ for two σ values. The figure shows that the clock jitter causes the timing offset to be larger than the detuning m in the jitter-free case. In particular, large clock jitter ($\sigma=1$) causes the timing offset to rise more rapidly with m than small clock jitter ($\sigma=0.4$), corresponding to a PDF with a long right tail.

Figure 6 shows the RMS timing jitter σ_u as a function of clock jitter σ for zero loop detuning. The plot is divided into three regions, the boundaries of which are arbitrary but were chosen to aid the qualitative understanding of the curves (compare Fig. 21 in [2]). For the following explanations, recall that the normalized and unnormalized RMS clock jitter are related by $\sigma = \sigma_\tau / (NK_P K_T)$.

Region 1): Timing jitter σ_u is (approximately) independent of reference clock jitter σ . This occurs when σ_τ is sufficiently smaller than the quantization step $NK_P K_T$ of the divided clock period, such that hunting jitter—the self-generated timing jitter due to the hard nonlinearity in the BPD—dominates [2]. Comparing the asymptotes depicted by the horizontal dashed lines, whose derivation will be outlined in Sec. IV-C, shows that timing jitter increases with loop delay in this region. More specifically, a single-delay loop exhibits a $\sqrt{3}$ times higher timing jitter than a zero-delay loop; a double-delay loop, a $\sqrt{7}$ times higher. This behavior is also evident from Fig. 4

Fig. 5. Timing offset μ_u vs. loop detuning m for two RMS reference clock jitter values σ and different loop delays D .

by the broader steady-state PDF for increasing D , and corresponds to the larger steady-state interval in the jitter-free case. Observe also in Fig. 6 that the transition to region 2 occurs at higher σ values when D is large; more reference clock jitter is needed to overcome the higher hunting jitter when the loop delay is large.

Region 2): Timing jitter σ_u increases with reference clock jitter σ . Since σ_τ is of the same order as the quantization step $NK_P K_T$, the Gaussian and hunting jitter contributions are roughly equal. Although the timing jitter PDF appears to be Gaussian in this region, as seen in Fig. 4 for $\sigma = 2$, the PDF is strictly speaking Gaussian for only one σ value and is Gaussian-like only in a range about this value; this was shown in [8] for $D = 0$ by computing the skewness and kurtosis excess of the PDF, and a similar computation for arbitrary D leads to this conclusion.

Region 3): Timing jitter σ_u increases proportionally to the square of reference clock jitter σ —independent of the loop delay D . Since σ_τ is much larger than the quantization step $NK_P K_T$, the loop delay shows little influence on the timing jitter PDF, implying that the PDF will have the same shape, and thus the same variance, independent of D . As part of our ongoing investigation, the asymptote depicted by the dashed line was analytically determined to be $\sigma_u = \sigma^2/\sqrt{2}$; contrast this with a loop in the presence of non-accumulative reference clock jitter where the timing jitter σ_u increases proportionally to σ , independent of the loop delay D (see Fig. 7 in [11]).

C. Periodic Orbits and Low-Jitter Case

A DBBPLL has the inherent property that even in the absence of jitter and noise, the loop exhibits timing jitter in the locked state. In particular, a deterministic timing jitter sequence of a first-order loop with zero detuning and jitter-free reference clock is characterized by a periodic orbit on the interval $[-(1+D), 1+D]$ in steady state [5]. For $D = 1$, for example, the periodic orbit has period 6 with values in the set $\{-2+u_0, -1+u_0, u_0, 1+u_0\}$, where $u_0 \in [0, 1)$. For each period, the (triangular) trajectory will visit the intervals $[-1, 0)$ and $[0, 1)$ twice, and the intervals $[-2, -1)$ and $[1, 2)$ once. Assuming a reference clock with sufficiently low jitter, a stochastic timing jitter sequence will show periodic-like behavior in that the histograms computed for consecutive time instants will have the same periodicity. To obtain the horizontal asymptote in Fig. 6 for this low-jitter case we computed the average histogram over one period, which can be approximated by a piecewise-constant PDF on $[-2, 2)$ whose value on $[-1, 1)$ is twice as large as that on $[-2, -1) \cup [1, 2)$. Setting the area of that PDF to one gives the height of the two pieces, from which the asymptote $\sigma_u = 1$ follows. Similar considerations lead to the asymptotes for $D = 0$ and $D = 2$ shown in the figure.

Fig. 6. RMS timing jitter σ_u vs. RMS reference clock jitter σ for zero loop detuning ($m = 0$) and different loop delays D .

V. CONCLUSIONS

Modeling the timing jitter process as a discrete-time vector Markov process has enabled us to statistically describe the combined effect of loop delay and Gaussian reference clock jitter in a first-order DBBPLL. The numerical solution of the associated CK equation has revealed that the steady-state timing jitter PDF is non-Gaussian due to the binary PD, and has allowed us to evaluate the loop's jitter performance (timing offset and RMS timing jitter), with emphasis on a single and double loop delay. For zero detuning, an asymptotic analysis has shown that RMS timing jitter is constant for small RMS clock jitter, and grows quadratically with large RMS clock jitter.

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