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Output-Jitter Performance of Second-Order Digital Bang-Bang Phase-Locked Loops with Nonaccumulative Reference Clock Jitter

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Abstract—Bang-bang phase-locked loops (BBPLLs) are inherently nonlinear systems due to the binary phase detector (BPD). While they are typically used for clock and data recovery, the ongoing trend toward digital loop implementations has resulted in several digital BBPLLs (DBBPLLs) suitable for frequency synthesis. This brief investigates the effect of nonaccumulative reference clock jitter (due to white phase noise) in second-order DBBPLLs, comparing the output jitter with that of first-order DBBPLLs. For small clock jitter, the nonlinear loop behavior is modeled as a two-dimensional Markov chain, and the output jitter is smaller than but close to that of a first order loop. For large clock jitter, the BPD nonlinearity is linearized, and the output jitter is larger than that of a first order loop; it is proportional to clock jitter and inversely proportional to the square root of the stability factor—the ratio of the proportional-path gain to the integral-path gain of the digital loop filter.

Index Terms—Bang-bang phase-locked loop, binary phase detector, Markov chain, timing jitter.

I. INTRODUCTION

Bang-bang phase-locked loops (BBPLLs) are a class of PLLs using a binary phase detector (BPD) and are widely used for clock and data recovery (CDR) [1]. While they are usually implemented based on the charge-pump architecture [2]–[4], the continuing trend to replace analog functions by digital blocks has resulted in digital BBPLL (DBBPLL) implementations suitable for high-bandwidth frequency synthesis [5]–[9]. A block diagram of a second-order DBBPLL is shown in Fig. 1 [10]. The binary output of the BPD is directly fed into the digital loop filter (DLF), whose output tunes the frequency of a digitally controlled oscillator (DCO)—the only analog block [5]. Advantages of this digital approach include compact circuit realization and easy programmability of loop dynamics.

Despite these recent DBBPLL implementations, an understanding of the loop's output-jitter performance remains incomplete. The analysis is complicated by the BPD nonlinearity which generates limit cycles in the noise-free case

Fig. 1. Second-order DBBPLL architecture [10].

[10]. In practice, phase noise on the clock sources causes random jitter on the clock edges [11]. The effect of jitter can be accurately analyzed using Markov models [12], but their applicability has been limited to first-order loops to date [13]–[16]. It is more common to linearize the BPD nonlinearity and apply linear transfer functions in the analysis [13], [17]–[20]. The loop linearization for the case of nonaccumulative reference clock jitter (due to white phase noise) has been developed in [13] and applied to the analysis of a second-order loop in [18]. When the reference clock jitter is small, however, the loop behaves nonlinearly, making the linear analysis inapplicable for applications where a clean reference is used [7]. Furthermore, little is known about the output-jitter performance when the reference clock is the dominant jitter source, as typically occurs in CDR applications [1].

This brief investigates the effect of nonaccumulative reference clock jitter (referred to as input jitter throughout) on the output jitter in second-order DBBPLLs. The nonlinear behavior for small input jitter is modeled as a two-dimensional Markov chain (2D MC), the stationary distribution of which is obtained in closed form. The linear behavior for large input jitter is analyzed using linear transfer functions [18], showing that the output jitter is determined by the stability factor—the ratio of the proportional-path gain to the integral-path gain of the DLF. It is shown that a first-order loop gives an upper bound for the output jitter of a second-order loop for small jitter, and a lower bound for large jitter. For small input jitter, however, the dominance of the proportional path entails that the output jitter of a second-order loop is well approximated by that of a first-order loop. For large input jitter, the output jitter of a second-order loop is proportional to input jitter and inversely proportional to the square root of the stability factor—a dependence obtained empirically by Walker [1].

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II. SECOND-ORDER DBBPLL AND LINEAR ANALYSIS

This section describes the output-jitter model of a second-order DBBPLL when the reference clock is subject to non-accumulative jitter, and briefly reviews the linear analysis of [13] and [18]. As shown in Fig. 1, the BPD output and the DLF are updated every divided clock cycle; thus it suffices to describe the loop behavior at discrete time instants $n = 0, 1, 2, \dots$. Denoting the time instant of the n th rising reference-clock and divided-clock edge by $t_{r,n}$ and $t_{d,n}$, respectively, and the timing jitter seen at the BPD input by Δt_n , the loop is modeled by the set of equations [10, (1)]

$$\Delta t_n = t_{r,n} - t_{d,n} \quad (1)$$

$$\psi_{n+1} = \psi_n + \text{sgn } \Delta t_n \quad (2)$$

$$T_{v,n} = T_{v0} + K_T K_I \psi_n + K_T K_P \text{sgn } \Delta t_n \quad (3)$$

$$t_{d,n+1} = t_{d,n} + N T_{v,n} \quad (4)$$

where $T_{v,n}$ is the n th DCO clock period and ψ_n the n th integrator state in the DLF¹. The BPD is modeled as the signum function, defined as $\text{sgn } x = 1$ for $x \geq 0$ and $\text{sgn } x = -1$ for $x < 0$. The DCO is considered as a linear block, with free-running clock period T_{v0} and period gain constant K_T .

To investigate the effect of input jitter on the output jitter, we assume ideal PLL blocks [13]. Jitter at the input (the reference clock) is modeled by setting $t_{r,n} = nT_{r0} + t_{j,n}$, where T_{r0} denotes the nominal reference clock period and the random variable $t_{j,n}$ accounts for random timing errors added to the n th ideal clock edge [11]. Throughout the brief we make the following assumptions.

- A1: The gain coefficients of the DLF are integer powers of two satisfying $K_P > K_I$.
- A2: The input jitter sequence $\{t_{j,n}\}$ is a sequence of independent, identically distributed Gaussian random variables with mean zero, variance σ^2 and distribution function F .

Assumption A1 is typically made in a practical loop design, where it is common to choose $K_P \gg K_I$ [2]–[4]. Moreover, since the LF is implemented in the digital domain, the gain coefficients K_P and K_I are integer powers of two [5], [6], [8]. Assumption A2 corresponds to nonaccumulative jitter, because consecutive random timing errors do not influence each other; the Gaussian distribution accounts for the random timing errors being caused by thermal electronic noise [11].

The quantity of interest in our analysis is the absolute output jitter, i.e., the absolute jitter of the DCO clock, defined as $j_{\text{out},n} = t_{v,n} - nT_{v0}$ [21], where $t_{v,n}$ is the n th rising DCO clock edge. To relate the output jitter to the input jitter, let us instead consider $j_{d,n} = t_{d,n} - nT_{r0}$, the absolute jitter of the divided clock. Assuming that the loop is in lock ($T_{r0} = NT_{v0}$), we can use (3) and (4) to derive the recursion $j_{d,n+1} = j_{d,n} + NK_T K_I \psi_n + NK_T K_P \text{sgn } \Delta t_n$. Because $\Delta t_n = t_{j,n} - j_{d,n}$ using (1), we obtain

$$\begin{aligned} j_{d,n+1} &= j_{d,n} + NK_T K_I \psi_n + NK_T K_P \text{sgn}(t_{j,n} - j_{d,n}) \\ \psi_{n+1} &= \psi_n + \text{sgn}(t_{j,n} - j_{d,n}). \end{aligned} \quad (5)$$

¹Different from [10], the integrator in Fig. 1 contains the delay in the forward path which is typical for a practical implementation [5], [19].

Fig. 2. Linearized jitter model of the second-order DBBPLL in Fig. 1 [18].

Together with $j_{\text{out},n} = j_{d,n}/N$, the stochastic recursion (5) models the output jitter of a second-order DBBPLL. In the next section, an exact analysis of (5) will be given using MC theory. Previous works along this line are [13] and [14] which analyzed a MC model of a first-order loop.

The more common approach is to linearize (5) and apply transfer functions in the analysis [18]. The BPD nonlinearity is linearized by replacing it with an equivalent BPD gain K_{bpd} and an additive, input-referred BPD jitter source t_{bpd} which models the jitter introduced by the binary phase-error quantization [13]. Figure 2 shows the linearized jitter model corresponding to the DBBPLL architecture of Fig. 1 [18]. The equivalent input jitter is the sum of input jitter t_j and BPD jitter t_{bpd} . A linear analysis presupposes that superposition can be applied, i.e., that t_j and t_{bpd} are uncorrelated. Based on simulation results, it was concluded in [18] that the two sources are almost completely uncorrelated if σ is larger than the threshold value $0.5NK_T K_P$. Furthermore, it was stated that below this threshold value, the dynamics are mainly nonlinear and the output jitter of the DBBPLL has to be determined by investigating the nonlinear map, maybe with the help of MCs [18]. The goal of the next section is to provide such an analysis.

III. 2D MC MODEL

In this section we define a 2D MC that describes the statistical time behavior of the output jitter, and derive the stationary distribution for small input jitter. To this end, it is convenient to normalize (5). On defining $v_n = -\psi_n$ and the normalized variables $u_n = -j_{d,n}/(NK_T K_I)$ and $\tau_n = t_{j,n}/(NK_T K_I)$, where $K_I > 0$, we obtain

$$\begin{aligned} u_{n+1} &= u_n + v_n - r \text{sgn}(u_n + \tau_n) \\ v_{n+1} &= v_n - \text{sgn}(u_n + \tau_n). \end{aligned} \quad (6)$$

The ratio $r = K_P/K_I$, called the stability factor², is an important parameter in the loop design [1], as it determines performance metrics such as output jitter, loop stability and locking time. Note that assumption A1 implies that the stability factor is an integer satisfying $r > 1$.

Due to assumption A2, the sequence $\{(u_n, v_n)\}$, $n \geq 0$, generated by (6) defines a homogeneous first-order 2D MC, the state space being the integer lattice $S = \mathbb{Z} \times \mathbb{Z}$. Let $\mathbb{P}(A|B)$ denote the conditional probability of A given B [12], and define the one-step transition probabilities $p_{ij,kl} = \mathbb{P}(u_{n+1} = k, v_{n+1} = l | u_n = i, v_n = j)$ for any two pairs $(i, j), (k, l) \in S$; i.e., $p_{ij,kl}$ is the probability that the MC will

²In the deterministic analysis in [10], the ratio $R = 1/r$ was used instead.

Fig. 3. State transition diagram of the restricted 2D MC for $r = 2$.

move from state (i, j) to state (k, l) in one step. From (6) it can be seen that the transition probabilities are given by

$$p_{ij,kl} = \begin{cases} F(-i) & k = i + j + r, l = j + 1 \\ F(i) & k = i + j - r, l = j - 1 \\ 0 & \text{else} \end{cases} \quad (7)$$

where $F(-i) = 1 - F(i)$ due to assumption A2.

Supposing the stationary case, the MC is described by $q(i, j) = \mathbb{P}(u_n = i, v_n = j)$, $(i, j) \in S$, the stationary joint distribution of the state variables (u_n, v_n) . Then $q(i, j)$ satisfies the balance equation [12]

$$q(k, l) = \sum_{(i,j) \in S} q(i, j) p_{ij,kl}, \quad (k, l) \in S. \quad (8)$$

Combining (7) and (8), the stationary joint distribution is a solution to the partial difference equation

$$q(i, j) = F(i - j + r - 1) q(i - j + r - 1, j + 1) + F(j - i + r - 1) q(i - j - r + 1, j - 1) \quad (9)$$

subject to the normalization condition $\sum_{(i,j) \in S} q(i, j) = 1$. Based on assumption A2, it can be shown that the joint distribution satisfies the reflection-symmetry relation

$$q(i, j) = q(-i, -j), \quad (i, j) \in S. \quad (10)$$

The solution to (9) provides a complete statistical description of the output jitter and may be obtained numerically. However, for the small-jitter regime where the linear analysis of [18] cannot be applied, we show next how to obtain a closed-form solution.

A. Stationary Distribution for the Small- σ Regime

For sufficiently small input jitter σ , the integrator state v_n will change only between the values $-1, 0$ and 1 , and we may therefore define a MC on the restricted state space $S = \mathbb{Z} \times \{-1, 0, 1\}$ with the one-step transition probabilities

$$p_{ij,kl} = \begin{cases} 1 & j = 1; k = i - r + 1, l = 0 \\ F(-i) & j = 0; k = i + r, l = 1 \\ F(i) & j = 0; k = i - r, l = -1 \\ 1 & j = -1; k = i + r - 1, l = 0 \\ 0 & \text{else} \end{cases} \quad (11)$$

where $i \in \mathbb{Z}$. Figure 3 plots the state transition diagram of this restricted 2D MC for $r = 2$. Arrows leaving a state (i, j) indicate the possible transitions; the weight of each arrow is the transition probability in (11). For example, if the MC is in state $(1, 0)$, it will move to state $(-1, -1)$ with probability $F(1)$ and to state $(3, 1)$ with probability $F(-1)$. If the MC is in a state with $j = 1$ or -1 , it will always move to a state with $j = 0$, so that the corresponding arrows have weight 1.

Let us now derive the stationary distribution $p(i) = \mathbb{P}(u_n = i)$, $i \in \mathbb{Z}$, associated with the restricted MC of Fig. 3. Substituting (11) into (8) yields the set of equations

$$q(i, -1) = F(i + r) q(i + r, 0) \quad (12)$$

$$q(i, 0) = q(i + r - 1, 1) + q(i - r + 1, -1) \quad (13)$$

$$q(i, 1) = F(-i + r) q(i - r, 0) \quad (14)$$

for $i \in \mathbb{Z}$. These equations can be combined into the second-order difference equation

$$q(i, 0) = F(-i + 1) q(i - 1, 0) + F(i + 1) q(i + 1, 0) \quad (15)$$

the solution of which is

$$q(i, 0) = q(0, 0) \prod_{k=0}^{i-1} \frac{F(-k)}{F(k+1)}, \quad i \geq 1 \quad (16)$$

where $q(i, 0) = q(-i, 0)$ follows from (10). For $q(i, j)$ to be a joint distribution, the arbitrary constant $q(0, 0)$ must be chosen such that $q(i, j)$ satisfies the normalization condition from before. Clearly, on inserting (12), (14) and (16) into the normalization condition, the constant is found to be

$$q(0, 0) = \frac{1}{2} \left(1 + 2 \sum_{i=1}^{\infty} \prod_{k=0}^{i-1} \frac{F(-k)}{F(k+1)} \right)^{-1}. \quad (17)$$

Having obtained the stationary joint distribution, the stationary distribution $p(i)$ is found by marginalization: $p(i) = \sum_{j=-1}^1 q(i, j)$. Substitution of (12) and (14) gives

$$p(i) = F(i + r) q(i + r, 0) + q(i, 0) + F(-i + r) q(i - r, 0). \quad (18)$$

Due to (10), the distribution is symmetric, i.e., $p(i) = p(-i)$, and so we may take $i \geq 0$. Setting $q(i - r, 0) = q(|i - r|, 0)$ in (18) and substituting (16) gives finally

$$p(i) = q(0, 0) \left[\left(F(i + r) \prod_{k=i}^{i+r-1} \frac{F(-k)}{F(k+1)} + 1 \right) \times \prod_{k=0}^{i-1} \frac{F(-k)}{F(k+1)} + F(-i + r) \prod_{k=0}^{|i-r|-1} \frac{F(-k)}{F(k+1)} \right] \quad (19)$$

for $i \geq 0$, where $q(0, 0)$ is given in (17). Equation (19) is the stationary distribution of the output jitter in the small- σ regime; similar expressions for a first-order loop appeared in [13] and for a first-order loop with delay in [14].

To compare (19) with Monte-Carlo simulations, let us consider a practical example of a second-order DBBPLL with parameters as in [18, Sec. III-F]. The (noise-free) DCO has a free-running clock period of $T_{v0} = 1/(91.6 \text{ MHz})$ and a period gain constant of $K_T = 5.8 \text{ ps}$, and the divider value is $N = 24$. The gain coefficients of the DLF are $K_P = 2^{-7}$

Fig. 4. Stationary output-jitter distribution for a second-order DBBPLL. The lines with unfilled markers are analytical predictions from (19). Notice that most of them are covered by the filled markers from simulation. Parameters: $K_P = 2^{-7}$, $K_I = 2^{-9}$, $r = 4$, $K_T = 5.8$ ps, $N = 24$.

and $K_I = 2^{-9}$. Compared to the value -143 dBc/Hz used in the linear analysis in [18], the power spectral density (PSD) of the reference clock's white phase-noise floor is taken to be $S_{\phi_r} \in \{-170, -160, -155, -150\}$ dBc/Hz. Because $\sigma^2 = T_{r0}/(4\pi^2)10^{S_{\phi_r}/10}$ [11], the corresponding nonaccumulative jitter is $\sigma \in \{53, 166, 296, 526\}$ fs which is below the threshold $0.5NK_TK_P = 544$ fs. For the simulation we generated a realization of the stochastic recursion (5) of length 10^6 and estimated the stationary output-jitter distribution using a histogram. The result is depicted in Fig. 4, showing good agreement with the analytical predictions from (19). The discrepancy between the predictions and the simulation results as σ increases is due to the reduced MC model becoming inaccurate, as v_n changes between more than the values $-1, 0$ and 1 . Note that the bang-bang phase updates of the proportional path cause the probability mass to be concentrated not only around zero but also around $\pm r$.

IV. OUTPUT-JITTER PERFORMANCE

In this section, by investigating the small and large-jitter regime separately, we derive an approximate formula for the total output jitter of a second-order loop, $\sigma_{\text{out,so}}$.

A. Small- σ Regime

The MC analyzed in the previous section describes the nonlinear loop behavior in the small- σ regime. An expression for the output jitter in this regime can be obtained from the stationary distribution $p(i) = \mathbb{P}(u_n = i)$ plotted in Fig. 4. Inspection of the figure shows that for small input jitter (circle markers), the stationary probability of the states $\pm 1, \pm(r-1)$ and $\pm r$ is 0.125, while the probability of the state 0 is 0.25. By definition of the variance we have $\sigma_u^2 = \sum_i i^2 p(i) = (1/2)(r^2 - r + 1)$, $r > 1$, and using $\sigma_{\text{out,so}}^2 = (K_T K_I)^2 \sigma_u^2$ yields the formula

$$\sigma_{\text{out,so}}^2 = \sigma_{\text{out,fo}}^2 - \frac{1}{2} K_T^2 K_I (K_P - K_I) \quad (20)$$

where $\sigma_{\text{out,fo}} = K_T K_P / \sqrt{2}$ is the small- σ asymptote for a first-order DBBPLL [14, Fig. 7]. Since $K_P > K_I$ by assumption A1, it follows from (20) that a second-order loop has a lower output jitter for small σ than a first-order loop. For the loop design, since typically $K_P \gg K_I$, the second term in (20) can be neglected and $\sigma_{\text{out,so}} \approx \sigma_{\text{out,fo}}$ to a good approximation.

B. Large- σ Regime

Based on the linearized loop analysis in [13] we now derive a formula for the output jitter in the large- σ regime, extending the formula for a first-order loop [1], [18]. For the linearized jitter model of Fig. 2, the transfer function from the input to the output is given by

$$H(z) = \frac{1}{N} \frac{K_1 z^{-1} + (K_2 - K_1) z^{-2}}{1 + (K_1 - 2) z^{-1} + (K_2 - K_1 + 1) z^{-2}} \quad (21)$$

where $K_1 = NK_T K_P K_{\text{bpd}}$ and $K_2 = NK_T K_I K_{\text{bpd}}$. The gain K_{bpd} and the jitter t_{bpd} of the linearized BPD depend on the steady-state timing-jitter probability density function $p_{\Delta t}$ [18]. Simulation results show that under assumption A1, $p_{\Delta t}$ of a second-order loop is largely determined by the proportional path or, equivalently, by a first-order loop. Thus K_{bpd} and t_{bpd} can be replaced by the expressions obtained for a first-order loop in [13] and [18], respectively. In particular, the PSD of the equivalent input jitter $t_j + t_{\text{bpd}}$ is given by $S_{\text{in}}(f) = (25/16)T_{r0}\sigma^2$ [18, Sec. III-H]. Since the loop is linearized, the PSD of the output jitter j_{out} is $|H(f)|^2 S_{\text{in}}(f)$, where $H(f) = H(z)|_{z=\exp(i2\pi f T_{v0})}$. The output-jitter variance follows from integration:

$$\sigma_{\text{out,so}}^2 = \int_{-f_{v0}/2}^{f_{v0}/2} |H(f)|^2 S_{\text{in}}(f) df = \frac{25}{16} \frac{\sigma^2}{2\pi i} \int_{|z|=1} f(z) dz \quad (22)$$

where $f(z) = H(z)H(z^{-1})z^{-1}$ is integrated over the unit circle $|z| = 1$ in the complex plane. By the residue theorem [22], it can be shown that

$$\frac{1}{2\pi i} \int_{|z|=1} f(z) dz = \frac{(K_3 - 1)(2K_1^2 - K_2(2K_1 + K_3 - 2))}{N^2 K_3 (K_1 + K_3 - 4)} \quad (23)$$

where $K_3 = K_1 - K_2$. To simplify (23), we note that the coefficients K_1 and K_2 depend on the BPD gain which, according to the analysis in [13], is given by $K_{\text{bpd}} = 2p_{\Delta t}(0)$. As argued above we can replace K_{bpd} by the expression $2/(2\pi\sigma)$ valid for a first-order loop for large σ [13]. Inserting this expression into (23), the result into (22), and assuming $\sigma > NK_T(2K_P - K_I)/(2\sqrt{2\pi})$ yields the formula

$$\sigma_{\text{out,so}}^2 = \sigma_{\text{out,fo}}^2 + \frac{25}{32} \frac{K_I}{K_P - K_I} \frac{\sigma^2}{N^2} - \frac{25}{32\sqrt{2\pi}} K_T K_I \frac{\sigma}{N} \quad (24)$$

where $\sigma_{\text{out,fo}} = 5/(4\sqrt{2\pi})\sqrt{K_T K_P \sigma/N}$ is the large- σ asymptote for a first-order DBBPLL [18, (17)]. Since the second term in (24) is larger than the third term, we see that a second-order loop has a higher output jitter for large σ than a first-order loop. Furthermore, the dominance of the second

Fig. 5. Output jitter $\sigma_{\text{out,so}}$ versus σ for varying stability factor r . Parameters: $K_P = 1$, $K_I \in \{2^{-3}, 2^{-5}, 2^{-7}, 2^{-9}, 2^{-11}, 0\}$, $N = K_T = 1$.

term as σ grows yields the large- σ asymptote for a second-order loop ($1 < r < \infty$):

$$\sigma_{\text{out,so}} = \frac{5}{\sqrt{32} N \sqrt{r-1}} \sigma \approx 0.88 \frac{\sigma}{N \sqrt{r}}. \quad (25)$$

Interestingly, the output jitter is proportional to the input jitter and inversely proportional to the square root of the stability factor; this dependence was obtained empirically by Walker [1, Fig. 21, Region II]. For the loop design, (25) implies that for fixed N and large σ , the output jitter can be halved by quadrupling the stability factor.

C. Prediction of Total Output Jitter

Having obtained expressions for the small and large-jitter regime, the total output jitter $\sigma_{\text{out,so}}$ can be approximately predicted by simple addition of the expressions (20) and (24). Figure 5 plots $\sigma_{\text{out,so}}$ as a function of σ , the parameter being the stability factor $r = K_P/K_I$ (see also [1, Fig. 21]). For fixed $K_P = 1$, the stability factor is increased by decreasing the integral-path gain K_I . The good agreement between theory and simulation results (obtained from Monte-Carlo simulation of (5)) for the whole σ range validates our analysis. The figure illustrates that for small (large) input jitter, the output jitter of a first-order loop is an upper (lower) bound for the output jitter of a second-order loop. In the small- σ regime, however, the negligible dependence on r for fixed K_P implies that a second-order and a first-order loop (dash-dotted line) have practically the same performance. In the large- σ regime, by contrast, the dependence on r is significant, and a second-order loop performs worse than a first-order loop.

V. CONCLUSIONS

This brief has shown how a combined MC and linear analysis provides a more thorough understanding of the output-jitter performance of second-order DBBPLLs. For small input jitter, the nonlinear loop behavior can be modeled as a first-order 2D MC, the stationary distribution of which is given in (19). In this regime, the output jitter of a second-order loop is smaller than but close to that of a first-order loop. For large input jitter, the output jitter of a second-order loop is higher than that of

a first-order loop, and is inversely proportional to the square root of the stability factor. Simple addition of the small-jitter formula (20) and the large-jitter formula (24) gives a good prediction of the total output jitter.

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