<table>
<thead>
<tr>
<th>Title</th>
<th>An CMOS impedance sensor for MEMS adaptive antenna matching</th>
</tr>
</thead>
<tbody>
<tr>
<td>Authors(s)</td>
<td>Tavakol, Armin; Staszewski, Robert Bogdan</td>
</tr>
<tr>
<td>Publication date</td>
<td>2015-05-19</td>
</tr>
<tr>
<td>Publisher</td>
<td>IEEE</td>
</tr>
<tr>
<td>Link to online version</td>
<td><a href="http://www.rfic-ieee.org/">http://www.rfic-ieee.org/</a></td>
</tr>
<tr>
<td>Item record/more information</td>
<td><a href="http://hdl.handle.net/10197/7298">http://hdl.handle.net/10197/7298</a></td>
</tr>
<tr>
<td>Publisher's statement</td>
<td>© 2015 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.</td>
</tr>
</tbody>
</table>
A CMOS Impedance Sensor for MEMS Adaptive Antenna Matching

Armin Tavakol and Robert Bogdan Staszewski
1 Delft University of Technology, The Netherlands 2 University College Dublin, Ireland

Abstract — This paper proposes a new calibration mechanism for passive adaptive cellular antenna matching network containing MEMS-based tunable devices. To avoid expensive and bulky couplers and reference circuitry, the tuner contains voltage and current sensors inserted before the antenna matching network. The sensed complex impedance generates 2-bit update controls for the tuning algorithm, which drives the MEMS-based tunable devices. The impedance sensing IC is designed to operate in the frequency range of 1.7–2.7 GHz and the clock frequency is 50 kHz.

Index Terms — Antenna tuner, matching network, impedance matching, sensing element, transmitter.

I. INTRODUCTION

Adaptive antenna matching networks are now used in cellular transmitters. They allow wideband operation with narrowband high-quality antennas of varying impedances. However, environmental changes also affect the antenna’s characteristics and can result in decreased maximum transmitted power and increased reflections. These changes are by nature unpredictable and increase VSWR. Therefore, a dynamic tuning system is required to estimate this reflected power and try to minimize it. Coupler-based architectures have been reported that can continuously measure the reflected power and tune the matching network by a control loop using exhaustive or genetic algorithms [1][2]. The main drawback in those systems is bulky and expensive couplers.

Other reported methods measure the impedance at the input of the matching network. By using a “sensing element” (or two [3]), two voltage signals are sampled. Based on those, the real and imaginary parts of the impedance are evaluated [4]. The challenging part is to generate reference signals for comparison with the measured ones for making the tuning decision. These reference voltages or impedances have strict stability requirements over PVT and frequency. Other tuning algorithms, such as an LMS algorithm with a control loop are also reported [5]. If the mismatch is only affecting the imaginary part of the antenna impedance, it is possible to use tunable devices to bring the phase difference between the input current and voltage to zero and thus forcing the impedance to the center of the Smith chart. However, any mismatch in the real part of the impedance cannot be corrected.

A new tuner is proposed in this paper that senses the input impedance in order to iteratively update the tunable devices. The impedance sensor allows the tuning algorithm based on a sign-sign LMS to be able to converge the input impedance to the center of the Smith chart. The control loop is shown in Fig. 1 and contains three main units: a very simple off-chip passive circuitry which senses the current and voltage input of the matching network input (Section II), an impedance sensor IC which generates 2-bit data corresponding to the input impedance of the matching network (Section III), and a tuning algorithm which tunes the MEMS varactors of the matching network (Section IV).

II. CURRENT AND VOLTAGE SENSING

To estimate the complex input impedance of the matching network on the Smith chart, a sensing unit is used to sample its input voltage and current.

![Fig. 1. Overview of the proposed antenna tuning system.](image1)

![Fig. 2. Voltage and current (VI) sensing unit.](image2)

1) Voltage Sensing: The voltage sensing circuit is a capacitive divider, as shown in Fig. 2. Disregarding parallel parasitics, the sensed voltage, $V_{S,v_in}$, has the same phase as the input of the matching network, $v_{in}$. The amplitude of the sensed voltage is proportional to the input voltage by an attenuation factor $K_{atten}$:

$$V_{S,v_in} = K_{atten} \cdot v_{in} = \frac{C_s}{C_s + C_b} \cdot v_{in}$$

where, $C_s$ and $C_b$ are the small and big capacitors of the capacitive divider. In this implementation, $C_s$ is off-chip, whereas $C_b$ is an on-chip MIM capacitor. It can be shown...
that any series inductance between the capacitors can only affect the denominator of $K_{atten}$ by adding a small real value. These parasitics will not affect the phase of $V_{S,vin}$.

2) Current Sensing: The current sensing circuitry is based on magnetic coupling between the transmission line connecting the PA output to the matching network. A narrow wire is placed very closely to the transmission line in order to achieve maximum magnetic coupling $k$. As shown in Fig. 2, a small portion of $i_{in}$ flows through the “sensing wire” via mutual inductance. The sensing wire has a finite inductance and is connected to a large resistive impedance, $R_b$ which is placed on-chip for biasing purposes. If the current through the sensing wire is disregarded, the differential voltage across the sensing wire is calculated as:

$$V_{S,iin} = j\omega M \cdot i_{in}$$  \hspace{1cm} (2)

where $M = k\sqrt{L_1L_2}$. $L_1$ and $L_2$ are the inductances of the coupled portion of the transmission line and the sensing wire, accordingly. Therefore, $V_{S,iin}$ contains both the phase and amplitude information of the input current.

III. IMPEDANCE SENSOR CHIP

The off-chip sensing circuitry provides two signals for the impedance sensor chip: $V_{S,vin}$ and $V_{S,iin}$, which correspond to the input voltage and current of the matching network respectively. The phase and amplitude of these signals can be expressed by the phase and amplitude of $v_{in}$ and $i_{in}$ as in the following equations:

$$|V_{S,vin}| = \frac{C_s}{C_s + C_b} \cdot |v_{in}|$$ \hspace{1cm} (3a)

$$\angle (V_{S,vin}) = \angle (v_{in})$$ \hspace{1cm} (3b)

$$|V_{S,iin}| = \omega \cdot M \cdot |i_{in}|$$ \hspace{1cm} (3c)

$$\angle (V_{S,iin}) = \angle (i_{in}) + 90^\circ$$ \hspace{1cm} (3d)

The sensor chip contains two independent paths, both providing 1-bit information for the tuning algorithm. The first path (“X-path”) contains a phase detector, which determines whether the $v_{in}$ phase leads or lags the $i_{in}$ phase. In other words, the phase difference between $V_{S,vin}$ and $V_{S,iin}$ ($\varphi_S = \angle V_{S,vin} - \angle V_{S,iin}$), is recognized to be whether less or more than 90 degrees. The second path (“R-path”) is only active when the impedance at the input of the matching network is real, i.e., on the horizontal axis of the Smith chart. The R-path then determines whether the current real impedance at the input is closer to or further away from the center of the Smith chart as compared to the previous state. These two paths are explained in detail below.

3) X-Path: The X-path detects the sign of the input impedance imaginary part. As shown in Fig.3, the phase detector followed by a passive low-pass filter and a comparator determines whether $\varphi_S$ is higher or lower than $90^\circ$. $P_{out}^+$ and $P_{out}^-$ are both biased at $V_{dd}$. During the positive half cycle of $V_{S,vin}$, when $Mn_1$ is on, $P_{out}^+$ and $P_{out}^-$ voltages are pulled down by $Mn_1$ and $Mn_2$, respectively, each for a period dependent on $\varphi_S$. Fig.4 shows the sign of the waveforms and the timing mechanism of the phase detector outputs.

The outputs of the low-pass filters indicate these periods and the comparator generates a 1-bit data indicating the comparison result between these two periods. The X-path output shows whether the input impedance is in the top-half or bottom-half of the Smith Chart, i.e., inductive or capacitive.

4) R-Path: The amplitude of the transmitted power at the input of the matching network can be written as in:

$$P_{in} = |v_{in}| |i_{in}| \cos(\varphi_{in}) = |v_{in}| |i_{in}| \sin(\varphi_S)$$ \hspace{1cm} (4)

When the input impedance lies on horizontal axis of the Smith chart, $\varphi_S$ is $90^\circ$ and $P_{in} = |v_{in}| |i_{in}|$, i.e., the product of input current and voltage amplitudes. As previously shown in (3), the amplitudes of $V_{S,vin}$ and $V_{S,iin}$ are linearly related to the input current and voltage amplitudes. Therefore, by maximizing the product of $|V_{S,vin}|$ and $|V_{S,iin}|$, the magnitude of the input power is also maximized. The maximum transmitted power corresponds to the impedance at the center of the Smith chart. It is important
to emphasize that this approach is only valid when dealing with real impedances.

As shown in Fig. 5, the R-path starts with two linear peak detectors, adapted from [6]. Their outputs are DC voltages corresponding to maxima of $|V_{S}\sin|$, (i.e., $v_{\sin}$) and $|V_{S'}\sin|$, which are then fed to a DC product estimator (DCPE) containing two cascoded NMOS transistors loaded by a small PMOS transistor with grounded gate. The transistors are sized such that the input values corresponding to the sensed I/V peak values will produce an output voltage profile containing a minimum. This minimum directly corresponds to those I/V peak values which have the maximum product of (4), that guaranteeing that the center of the Smith chart would eventually be reached.

After the algorithm completes the X-path to land the input impedance onto the horizontal axis of the Smith chart, the sample-and-hold (S/H) circuit is then activated and compares the new DCPE output to the previous minimum value found and stored in the S/H capacitor. If the new value is lower than the held one, it means that new impedance on the horizontal axis of the Smith chart is closer to the center. The new DC value will be stored in the S/H capacitor and the R-path output informs the tuning algorithm that a new optimal point is discovered. The tuning algorithm will then decide on the direction change of the MEMS control words.

**IV. Tuning Algorithm**

The tuning algorithm outputs are mostly dependent on the architecture of the matching network. However, the algorithm employs the same approach for all matching networks: It is based on two steps repeatedly performed in succession to force the input impedance to converge to the center of the Smith chart:

1) Bring the imaginary part of the impedance to zero: By monitoring the X-path output, the imaginary part of the impedance is considered to be as close as possible to zero when the output bit toggles. This means the sign of the imaginary part is changed and the input impedance lies as close as possible to the horizontal axis.

2) Finding the optimal point: After landing on the horizontal axis, the DCPE output indicates whether the new landing point is closer or further from the previous one. This will determine whether the direction which the algorithm has chosen is correct or not. The output bit of the R-path provides the algorithm with this information and the algorithm decides on the next state.

In this demonstrator, a $\pi$-shaped matching network with two shunt digitally controlled MEMS capacitors is used (in the range of 1–5 pF), as shown in Fig. 2. Control words for $C_1$ and $C_2$ are provided by the tuning algorithm. It can be seen that the first step of the algorithm is performed mostly via controlling $C_1$, as shown in Fig. 6. The algorithm is developed in such a way that if $C_1$ tuning range is unable to bring the impedance to the horizontal axis, the algorithm will use $C_2$ to push the input impedance to another location on the Smith chart where $C_1$ is able to toggle the output of the X-path by either decreasing or increasing its control word.

For the second step, $C_2$ is used to adjust the location of the impedance on the horizontal axis. $C_2$ capacitive step during the second tuning phase is set to be different from the first phase in order to prevent possible locking on an undesirable state.

A reset signal is used to reset the S/H circuit and to start over the algorithm. This is necessary in a dynamic operation since the previous optimal value stored in the S/H circuit might prevent the R-path from discovering a new optimal point. This would result in a confusion in the tuning algorithm in determining the direction in which $C_2$ should be increased or decreased. A reset signal is then used to reset the algorithm every hundreds of clock cycles to assure the correct dynamic tuning.

**V. Experimental Verification**

The sensor chip was fabricated in TSMC 0.18 um CMOS. The micrograph of the chip is shown in Fig. 7.

To test the sensor chip, an FR4 PCB was designed. A 50-Ω microstrip line with electrical length of 180° is placed between two SMA connectors: one connected to an external PA and the other connected to a passive slug tuner terminated with 50Ω. The $\pi$-matching network is placed in-between the transmission line for de-embedding purposes. An RF power of 30 dBm is fed to the transmission line. The tuning algorithm was implemented on Xilinx FPGA.
The current sensing wire is placed as close as possible to the transmission line in order to achieve maximum magnetic coupling. Since the ground plane of the PCB is connected to the ground of the chip and also due to the high-impedance path seen by $V_{S,\text{in}}$, both $V_{S,\text{in}}^+$ and $V_{S,\text{in}}^-$ voltages are dominated by electrical coupling instead of magnetic coupling. In order to solve this problem, the middle point of the sensing wire is biased by a low-impedance path. This ensures that proper signals are delivered to the chip. The simulated value for the coupling coefficient is 0.22.

As an example of tuning, Fig. 8 illustrates the convergence to the center of the Smith chart. The convergence target is $V_{\text{SWR}} \leq 2$. To thoroughly test the tuning algorithm, the load impedance was placed at different locations on the $V_{\text{SWR}}=10$ circle and then the algorithm was executed. Fig. 9 clearly demonstrates the reduction in $V_{\text{SWR}}$ to the target area. As compared to the exhaustive search approach (e.g., [1]), a 1–2 orders of magnitude improvement in the number of steps can be achieved.

VI. CONCLUSION

We have proposed and demonstrated a low-complexity IC sensor for an adaptive antenna matching network that avoids any expensive and bulky couplers and reference circuitry. The input $V_{\text{SWR}}$ of the antenna tuner can be greatly improved in mismatched conditions using an iterative approach with 2-bit directional information. The tuning algorithm allows this convergence in much less number of steps than previously reported. The dynamic operation of the system ensures maximum power transmission in any mismatched condition.

ACKNOWLEDGMENT

We thank Cor Schepens from Cavendish Kinetics for technical discussions and for providing RF-MEMS used in the demonstrator. We also thank Xilinx for providing FPGA Zedboard to implement the tuning adaptation algorithm.

This work was financially supported by EU ENIAC grant 270683-2 ("Artemos").

REFERENCES


