A Wideband 60 GHz Class-E/F2 Power Amplifier in 40nm CMOS

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Abstract — This paper presents a fully integrated 60 GHz power amplifier in 40 nm CMOS that reaches the highest reported product of power-added efficiency and bandwidth. It is achieved through low/moderate coupling-factor transformers in the preliminary stages and a proper second harmonic termination of the output stage, such that it can operate as a class-E/F2 switched-mode PA at the saturation point. The three-stage PA delivers 17.9 dBm saturated output power with 20% peak PAE. It demonstrates a bandwidth of 9.7 GHz with a peak gain of 21.6 dB.

Index Terms — Power amplifier, mm-wave, class-E/F2, switched-mode, transformer, PA stability

I. INTRODUCTION

A key challenge of 60 GHz CMOS radios is a poor efficiency of their power amplifier (PA). Employing nonlinear switched-mode PAs within digitally intensive transmitter architectures, such as outphasing and direct digital-to-RF conversion [1], can improve the total system efficiency. However, switching at mm-wave is not trivial due to the large output capacitance and low current driving capability of CMOS transistors.

In this paper we propose a new architecture of a fully integrated switched-mode wideband 60 GHz PA in standard digital 40 nm CMOS. By a proper second-harmonic termination of its output matching network, the required systematic peak current of the final stage is reduced such that it can act as a class-E/F2 switched-mode PA at saturation. Transformers of low/moderate coupling are also utilized in the preliminary stages to improve the overall bandwidth. We also propose a technique to stabilize transformer-based mm-wave amplifiers against various modes of undesired oscillations.

II. BENEFITS AND CONSTRAINTS OF CLASS-E/F PA

It is shown in Kee et al. [2] that drain efficiency \(\eta_D\) of zero-voltage switching (ZVS) PA of Fig. 1(a) can be written in terms of a set of technology dependent parameters \((R_{on}, C_{out})\) and a set of matching network or waveform dependent parameters \((F_C, F_{P1}, F_I)\). To better understand the tradeoffs in mm-wave designs, we extend the results of [2] to:

\[
\eta_D = 1 - \frac{R_{on} I_{rms}^2}{V_{DD} I_{DC}} = 1 - \left(\frac{I_{rms}}{I_{DC}}\right)^2 \frac{I_{DC}}{C_S \omega_0 (V_{DD} - V_{sat})} \left(\frac{C_S}{C_{out}}\right) (R_{on} C_{out}) \omega_0. \quad (1)
\]

where \(R_{on}\) and \(C_{out}\) are, respectively, on-state channel resistance and off-state output capacitance of \(M_1\) transistor. Note that \(R_{on} \times C_{out}\) is invariant to changes of \(M_1\)'s width. \(I_{DC}\) and \(I_{rms}\) are defined as the average and RMS values of \(M_1\) drain current, and \(C_S\) is the PA desired shunt capacitance to satisfy the ZVS criterion. \(V_{sat}\) represents the transistor’s average \(V_{DS}\) in on-state. Note that since \(F_C\) should not change over the \(\omega_0 = 2\pi f_0\) operating frequency, \(C_S\) has to reduce with increasing \(f_0\). Hence, \(C_S\) limits the transistor’s width at mm-wave, which leads to a dramatic increase in \(R_{on}\) and thus \(V_{sat}\) of the switching device. Consequently, we include the effect of \(V_{sat}\) in \(\eta_D\) and \(F_C\) definitions in (1) and (2) to achieve more practical analytic results than in [2]. \(V_{sat}\) can be calculated from

\[
P_{loss} = V_{sat} I_{DC} = R_{on} I_{rms}^2 \rightarrow V_{sat} = R_{on} I_{DC} F_I^2. \quad (3)
\]

By replacing \(I_{DC} = F_C C_S \omega_0 (V_{DD} - V_{sat})\) in (3),

\[
V_{sat} = V_{DD} \frac{F_C F_I^2 R_{on} C_{out} \omega_0}{\alpha + F_C F_I^2 R_{on} C_{out} \omega_0}. \quad (4)
\]

where \(\alpha = C_{out}/C_S\) denotes how much the required \(C_S\) for the class-E/F operation is occupied by \(M_1\)'s self-capacitance. It is also instructive to go one step further than [2] and calculate the class-E/F PA characteristics.
realized as open circuit at the 2nd harmonic, 2
and remains below during switching while its output capacitance $C_{\text{out}}$ must be capable of providing the required systematic peak current. First, transistor based on waveform and technology parameters of Fig. 2. Schematic and layout of the proposed 60 GHz PA.

By substituting (4) in (1), $\eta_D$ is simplified to

$$\eta_D = \frac{\alpha}{\alpha + F_C F_1^2 R_{\text{on}} C_{\text{out}} \omega_0}.$$  (7)

Eqs. (4) and (7) indicate that $V_{\text{sat}}$ and $\eta_D$ improve by using a matching network with lower $F_1$ and $F_C$, which is in line with $f_m$ optimization. Eq. (7) also predicts $\eta_D=65\%$ for 40 nm class-E/F2 PA at 60 GHz. The switch size is relatively small such that its $R_{\text{on}}$ degrades $\eta_D$ to somewhere between class-A and B. It can be shown that PA's output power and gain can be calculated by

$$P_{\text{out}} = \eta_D P_{\text{DC}} = \left(\frac{\alpha V_{\text{DD}}}{\alpha + F_C F_1^2 R_{\text{on}} C_{\text{out}} \omega_0}\right)^2 F_C C_S \omega_0.$$  (8)

$$G_p = \frac{P_{\text{out}}}{V_{\text{DD}}^2/2R_{\text{on}}} = \frac{2\alpha F_1^2 R_{\text{on}} C_{\text{out}} \omega_0}{(\alpha + F_C F_1^2 R_{\text{on}} C_{\text{out}} \omega_0)^2}.$$  (9)

Unfortunately, both $P_{\text{out}}$ and $G_p$ reduce almost linearly with $F_C$. Consequently, higher $f_m$ of class-E/F2 operation is achieved through painful reduction of $P_{\text{out}}$ and precious device $G_p$, which can potentially reduce the total PAE.

### III. Power Amplifier Design

Figure 2 shows the schematic of the proposed PA. A 3-stage common-source pseudo-differential pair is chosen to compensate for the gain penalty $G_p$ of the class-E/F2 operation in the last stage. A transformer-based power splitter converts the single-ended $S_{in}$ input to two differential signals feeding pre-drivers. Another set of splitters is added before the four parallel units of the output stage. A combination of series-parallel combining is used in the output matching network. A 2-way differential series combining is achieved by a distributed active transformer [3] to reduce the resistive load seen by each transistor such that the systematic $P_{\text{out}}$ reduction of class-E/F2 is partially compensated. By exploiting parallel combining, the output devices can be smaller for the same $P_{\text{out}}$, which effectively improves the transistors’ internal loss and $f_{\text{max}}$. Hence, they can generate a stronger 2nd harmonic current which is beneficial for the class-E/F2 operation.

Figure 3 (a) shows the half-circuit model of the output matching network. The total effective inductance at the output of the matching network ($4L_{s3}+L_{as3}+L_{asp}/2$ must resonate with the parasitic capacitance of the pad ($C_L$) to optimize its insertion loss. Furthermore, the combination of the transformer leakage inductance $L_{p3}(1-k_{m3}^2)$ and the effective inductance of differential strip-lines $L_{PT}$ along $C_S$ must satisfy zero-voltage and zero-slope class-E switching criteria by [2]

$$L_{p3}(1-k_{m3}^2) + L_{PT} = 1/4.74\omega_0^2.$$  (10)

The matching network behavior is entirely different for the common-mode (CM) input signals. The transformer’s coupling factor is negligible in CM excitation and thus $R_L$, $C_L$ and $L_{s3}$ cannot be seen by the even harmonics. Hence, the transmission line and transformer primary inductance, which is seen by CM signals, has to resonate with $C_S$ at $2\omega_0$ to satisfy the class-E/F2 operation. Figure 3 (c) indicates $F_C$ is just slightly degraded when CM resonance lies 25% away from $2\omega_0$. Thus, this PA is quite insensitive to the precise CM inductance value, which promotes a wide bandwidth operation.
that neither adding an RC stabilization network at the MOS gate nor matching network loss can dampen the oscillation without affecting the precious power gain at $\omega_0$. Fortunately, using relatively large resistors ($R_B \sim 3 \text{k}\Omega$) between the center tap of the secondary windings of the input and inter-stage transformers and gate bias voltage can cancel out the CM currents at the transformer secondary winding. Hence, any CM oscillation will be damped. Nevertheless, a combination of CM and differential-mode (DM) oscillation can potentially happen in the transformer splitter. As shown in Fig. 4 (b), each differential pair could oscillate in CM but with 180° phase shift to each other. Hence, neither neutralization capacitors nor $R_B$ will damp this oscillation. We propose adding a weak cross connection between the splitter’s in-phase ports to reduce the loop gain in this oscillation mode without affecting the splitter’s main function. Another solution would be to add a lossy path between the ground connections of two pseudo-differential pairs across the splitter.

The effective Q-factor of the PA input/output matching network is degraded by the 50Ω load and RF pad parasitic capacitance, $C_L \leq 50 \text{fF}$, to about 1–2 at 60 GHz, thus making these networks wideband. However, the input impedance of MOS transistors is considered as load to the inter-stage matching network, where $Q_{eff} = R_{in}/C_{in}/\omega_0 \approx 10$ at 60 GHz. Hence, the impedance seen at the input of the transformer network $(r_{in}+jX_{in}$ in Fig. 5(a)) changes significantly over frequency and thus limits the PA BW. Figure 5(b) depicts the position of zeros and poles of the $X_{in}$ transfer function. Under a high $k_m$ case ($\geq 0.7$), the conjugate zeros pair occurs at much higher frequency than the poles of the system. Hence, a large variation is seen in $X_{in}$ (see Fig. 5(c)). However, the zero/pole pairs come closer together with lower $k_m$ and a flatter region is observed in the $X_{in}$ plot. Hence, the transistor sees its desired impedance over a wider frequency range. The additional insertion loss penalty is only $\leq 1.5 \text{dB}$ over the BW by using a $k_m=0.25$ transformer. That penalty happens at the primary stages where it has negligible effect on the total PAE [4].
S-parameters are shown in Fig. 6 (b). With 1 V supply, the PA achieves a peak power gain of 21.6 dB at 58 GHz with BW of 9.7 GHz (51.5 to 61.2 GHz). The $S_{11}$, $S_{22}$ and $S_{12}$ are respectively better than -6, -7 and -42 dB within 50–67 GHz. The large-signal measurements are done by a mixed-signal active load-pull setup [5]. Consuming $\leq 0.3$ A from a 1 V supply, the measured $P_{1\text{dB}}$ and $P_{\text{sat}}$ are respectively 14.9 dBm and 17.9 dBm with 20.5% PAE at 60 GHz. The power performance is characterized in Fig. 6 (d). The following parameters are maintained over 52–63 GHz: 16.9 dBm $P_{\text{sat}}$, 13.8 dBm $P_{1\text{dB}}$, and 16% PAE. Figure 7 illustrates PA’s constant gain and PAE contours and also verifies the PA stability over load variation.

Table I shows a comparison of state-of-the-art 60 GHz CMOS PAs. Our PA achieves comparable BW as in a 28 nm PA [4], but with a much higher PAE. For $P_{\text{sat}} \approx 18$ dBm, only class-AB PA in [6] shows better PAE, but at a lower gain and BW. Furthermore, the product of PAE and BW reaches the best reported.

V. CONCLUSION

The benefits, constraints and trade-offs of different flavors of class-E/F PAs have been investigated from the mm-wave viewpoint. The resulting new proposed architecture of a fully integrated 60 GHz power amplifier was realized in 40-nm bulk CMOS. This PA utilizes a proper second-harmonic termination in the last stage and low/moderate magnetic coupling factor transformers in the intermediate stages to reach the best product of PAE and BW. The PA is also stabilized against the combination of DM and CM oscillation mode.

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