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A Fully Integrated 28nm Bluetooth Low-Energy Transmitter with 36% System Efficiency at 3dBm

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Abstract—We propose a new transmitter (TX) architecture for ultra-low power radios. An all-digital PLL employs a digitally controlled oscillator with switching current sources to reduce supply voltage and power without sacrificing its phase noise and startup margins. It also reduces 1/f noise allowing the ADPLL, after settling, to reduce its sampling rate or shut it off entirely during direct DCO data modulation. The switching power amplifier integrates its matching network while operating off entirely during direct DCO data modulation. The switching ADPLL, after settling, to reduce its sampling rate or shut it and startup margins. It also reduces 1/f noise allowing the supply voltage and power without sacrificing its phase noise controlled oscillator with switching current sources to reduce ultra-low power radios. An all-digital PLL employs a digitally

I. INTRODUCTION

Ultra-low power (ULP) transmitters are key subsystems for wireless sensor networks and internet-of-things (IoT). However, the system lifetime is severely limited by their power consumption and available battery technology. Energy harvesting can enable further applications but provides lower supply voltages (on-chip solar cells: 0.2–0.8V) than deep-nanoscale CMOS supply of 1V. Although dc-dc converters can boost the voltage, their poor efficiency (≤80%) introduces significant power penalty. Hence, the following new techniques are exploited in this work to enhance the ULP transmitter (TX) efficiency: First, the most power-hungry circuitry, such as digitally controlled oscillator (DCO) and output stage of power amplifier (PA), can operate directly at low voltage of harvesters. Second, a new switching current source oscillator optimized for 28 nm CMOS reduces power and supply voltage without compromising the robustness of the oscillator start-up or loading its tank quality factor. Third, thanks to the low wander (i.e., low flicker noise) of the DCO, digital power consumption of the rest of all-digital PLL (ADPLL) is saved by scaling the rate of sampling clock to the point of its complete shut-down. Last, a fully integrated differential class-E/F2 switching PA is utilized to optimize high power added efficiency (PAE) at low output power of 0–3 dBm.

II. SWITCHING CURRENT SOURCE OSCILLATOR

The phase noise (PN) specifications are quite trivial for IoT applications and can be easily met by LC oscillators as long as the Barkhausen start-up criterion is satisfied over process, voltage and temperature (PVT) variations. Consequently, reducing DCO’s power consumption (PDCO) is the ultimate goal of IoT applications. The PDCO can be calculated by [1]

\[ P_{DCO} = V_{DD}^2 \cdot \frac{\alpha_v}{\alpha_i} \cdot \frac{1}{R_{in}}. \]  

where, \(R_{in}\) is an equivalent input parallel resistance of the tank modeling its losses; \(\alpha_i\) is the current efficiency, defined as ratio of the fundamental component of tank’s current \(I_{tank}\) over the oscillator DC current \(I_{DC}\); and \(\alpha_v\) is the voltage efficiency, defined as ratio of the drain oscillation amplitude \(V_{osc}\) (single-ended) over the supply voltage \(V_{DD}\).

Lower \(P_{DCO}\) is typically addressed by scaling up \(R_{in} = L_{1}\omega_0 Q_1\) simply via a large multi-turn inductor [2]. However, (1) indicates that topology parameters such as oscillator’s \(\alpha_i\) and minimum supply voltage \((V_{DD_{min}})\) can also play an important role in the minimum achievable \(P_{DC}\). Fig. 1 illustrates the proposed oscillator that combines best features of the traditional cross-coupled NMOS oscillator (i.e., low \(V_{DD}\)) and the complementary push-pull oscillator (i.e., high \(\alpha_i\)) from the ULP standpoint. As can be gathered from Fig. 1, oscillation voltage at \(G_{12}\) is high within the first half-period. Hence, only \(M_2\) and \(M_4\) transistors are on and the current flows from left to right side of the tank’s primary inductor \(2L_P\). However, \(M_1\) and \(M_3\) are turned on for the second half-period and tank’s current direction is reversed. Consequently, like in the push-pull structure, the tank current flow is reversed every half-period thus doubling the oscillator’s \(\alpha_i\) to 4/\(\pi\).

The minimum \(V_{DD}\) is determined by the bias voltage \(V_B = V_{OD1} + V_g3\). Hence, \(M_{3,4}\) should work in weak-inversion keeping \(V_{g3} < V_t\) to achieve lower \(V_{DD_{min}}\). Since \(M_{1-4}\)
have the same DC gate voltage, M3,4 sub-threshold operation also provides enough VOD overdrive for the switching current source devices M1,2 to operate in the saturation region at the DC operating point. Hence, unlike traditional oscillators, the dimension of M3,4 devices must be a few times (i.e., 8×) larger than current source devices to guarantee their weak-inversion operation. Furthermore, the oscillation swing cannot go further than VOD1,2 at DA/DB nodes, which is chosen ∼150 mV to satisfy the system’s phase noise spec by a few dB margin. Consequently, as with cross-coupled NMOS oscillator, the proposed structure can operate at VDD as low as 0.5 V.

The transformer voltage gain (A) enhances the oscillation swing at M1,4 gates to even >VDD and guarantees the startup over PVT variations. Furthermore, the combination of A and the effective trans-conductance gain of M1,4 must compensate the tank losses. Hence, the contribution of M1,4 to the oscillator PN reduces by A, which compensates the effect of lower voltage efficiency (αV) of this structure on the oscillator PN and FoM.

Larger tank input impedance, Rp is also beneficial to reduce the oscillator’s power consumption. Rp reaches its maximum when LpCp/LpCp=1 for Qp ≈ Qp. Hence, the PVT tuning capacitors are divided in the transformer’s primary and secondary to roughly satisfy this criterion.

Switching the bias of M1,4 devices reduces both their 1/f noise and also the DC component of their effective ISF function. Consequently, a much lower 1/f3 PN corner is expected than in the traditional oscillators [1].

### III. CLASS-E/F2 POWER AMPLIFIER

Designing a fully integrated PA optimized for low output power (Pout < 3 dBm) with PAE > 40% is very challenging, especially when differential structure is needed to satisfy the stringent 2nd harmonic emissions. To realize such a low Pout, one needs to employ a matching network with a large impedance transformation ratio (ITR) to increase the load resistance, rL, seen by the PA transistor drains of Fig. 2.

\[
\text{ITR} = r_L / R_L = 0.5 \cdot n^2 \cdot k_m^2
\]  

Unfortunately, the differential structure and imperfect magnetic coupling factor km of the matching network’s transformer exhibit reverse effect of reducing rL and thus ITR. Hence, the transformer turns ratio (n:1) should be large n>4 to compensate for them. However, Q-factor of transformer windings, and thus its efficiency, drops dramatically with n>2. Consequently, the PAE of published integrated PAs is relatively low (<30%) or off-chip components are used in their matching networks [2]-[6].

The drain efficiency ηD of class-E/F switch-mode PA can be calculated by [7]

\[
\eta_D = \left( \frac{C_{out}/C_1}{C_{out}/C_1 + F_C F_T R_{on} C_{out} \omega_0} \right)
\]  

where, C1 is PA’s required shunt capacitance to satisfy class-E/F zero-voltage and zero-slope (ZVS) switching [8]. Ron and Cout are, respectively, on-state channel resistance and output capacitance of M1 transistor. Note that Ron×Cout is a constant at a given technology and invariant to changes of M1’s width. Fiat is defined as ratio of RMS over DC values of M1 drain current. FC is the PA waveform factor. Both Fiat and FC are merely a function of matching network strategy and do not change over technology or PVT variations [8].

A smaller Pout can also be realized by using a lower VDD for the PA’s drains (e.g., 0.5 V) without any degradation of ηD, as gathered from (3). As a consequence, the required ITR will be smaller, which results in better efficiency of PA’s output matching network. Furthermore, the drain voltage of the switching transistor is also limited to ≤1.5 V, alleviating reliability issues due to gate-oxide breakdown [9]. Eq. (3) also indicates that the switching amplifiers with smaller FC/FT (see Table 1) inherently demonstrate higher efficiency. For example, class-E PA efficiency can be improved by realizing an additional open circuit as the PA switches’ effective load at 2nd harmonic 2ω0 (i.e., class-E/F2 operation). Furthermore, class-E/F2 shows a better tolerance to Cout variations [7] due to the role of 2nd harmonic tuning in smoothing the drain voltage waveform [8]. These benefits come at the expense of
\( \omega \) differently to the common-mode (CM) and differential-mode criteria.

The inductance of a class-E/F PA to satisfy its ZVS switching criteria of drain current. Furthermore, CM inductance cannot be seen by the PA transistors is mainly determined by the dimension of the trace between the transformer center-tap and decoupling capacitors at the output, after decoding, is normalized to \( T \) phase error \( \phi_E \). The DCO tuning word is updated based on \( \phi_E \).

The following architectural innovations allow the ADPLL to support ULP operation (highlighted in blue): The effective sampling rate of the phase detector and its related DCO update is dynamically controlled by scaling-down the frequency reference (FREF) clock and simultaneously adjusting the loop gain. During ADPLL settling, the full FREF rate is used, but afterwards its rate could get substantially reduced (e.g., 8x), thus saving power consumption of the digital circuitry. The resulting in-band PN degradation is tolerable due to low PN of the DCO. In fact, freezing FREF would incur sufficiently low frequency drift during Bluetooth 625\( \mu \)s packets, while keeping in operation the bare minimum of circuitry highlighted in red.

### IV. ALL-DIGITAL PHASE-LOCKED LOOP ARCHITECTURE

Fig. 4 shows a block diagram of the proposed ultra-low power (ULP) all-digital PLL (ADPLL) adapted from a high-performance cellular 4G ADPLL [10]. The \( \sim 2.45 \) GHz 2 divider output of 4 phases, CKV\( ^{0...3} \) vector clock to sample the variable DCO phase \( \frac{\theta V[k]}{} \) to calculate the phase error, \( \phi_E[k] \). To avoid metastability in FREF retiming, FREF is simultaneously oversampled by different phases of CKV and an edge selection signal chooses the path farther away from metastability. The \( \phi_E[k] \) is fed to the type-II loop filter (LF) with 4th order IIR. The LF is dynamically switched during frequency acquisition to minimize the settling time while keeping the phase noise (PN) at optimum. The built-in DCO gain, \( K_{DCO} \), and TDC gain, \( K_{TDC} \), calibrations are autonomously performed to ensure the wideband FM response.

The long string of \( 417 \) ps/7 ps >60 inverters is shortened 4x by running the DCO at 2x the carrier frequency and dividing its output by 2 to create a CKV clock vector, CKV\( ^{0...3} \). A phase predictor ensures the TDC input CKV\( ^{+} \) is < \( T_V/4 \) by selecting a CKV phase that is closest to FREF. The TDC output, after decoding, is normalized to \( T_V \) by the \( \Delta_{TDC}/T_V \) multiplier and the octal estimation, normalized to \( T_V/4 \), is added to produce the phase error \( \phi_E \). The DCO tuning word is updated based on \( \phi_E \).

The following architectural innovations allow the ADPLL to support ULP operation (highlighted in blue): The effective sampling rate of the phase detector and its related DCO update is dynamically controlled by scaling-down the frequency reference (FREF) clock and simultaneously adjusting the loop gain. During ADPLL settling, the full FREF rate is used, but afterwards its rate could get substantially reduced (e.g., 8x), thus saving power consumption of the digital circuitry. The resulting in-band PN degradation is tolerable due to low PN of the DCO. In fact, freezing FREF would incur sufficiently low frequency drift during Bluetooth 625\( \mu \)s packets, while keeping in operation the bare minimum of circuitry highlighted in red.

### V. MEASUREMENT RESULTS

Fig. 5 shows the die photo of the 0.75mm\(^2\) ULP TX in TSMC 1P9M 28nm CMOS. Both DCO and PA transformer’s windings are realized with top ultra-thick metal. However, they include a lot of dummy metal pieces on all metal layers (M1–M9) to satisfy very strict minimum metal density manufacturing rule of advanced (\( \leq 28 \) nm) technology nodes.
**TABLE II**

**Performance summary and comparison with state-of-the-art.**

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<tr>
<th></th>
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<th>ISSCC’13</th>
<th>ISSCC’12</th>
<th>ISSCC'14</th>
<th>ISSCC’15</th>
<th>Renesas[8]</th>
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<tr>
<td>CMOS technology</td>
<td>28nm</td>
<td>90nm</td>
<td>130nm</td>
<td>65nm</td>
<td>55nm</td>
<td>40nm</td>
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<tr>
<td>DAC PN (dBc)</td>
<td>-116</td>
<td>-111</td>
<td>-107</td>
<td>-108.2</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>PLL PN (dBc)</td>
<td>-85</td>
<td>87</td>
<td>-87.5</td>
<td>-87.5</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Integrated PN (dBc/Hz)</td>
<td>-87.5</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<tr>
<td>Output power (dBm)</td>
<td>-5 to +3</td>
<td>-23 to -1</td>
<td>-30 to +5</td>
<td>-10 to -3</td>
<td>-20 to 0</td>
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<tr>
<td>Maximum PAE</td>
<td>41%</td>
<td>25%</td>
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<td>&lt;25%</td>
<td>&gt;25%</td>
<td>&gt;25%</td>
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<td>On-chip matching network</td>
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<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Supply voltage (V)</td>
<td>0.5/1</td>
<td>1.2</td>
<td>1</td>
<td>1.1</td>
<td>0.9/3.3</td>
<td>1.1</td>
</tr>
<tr>
<td>Power consumption (dBm)</td>
<td>0.2/0.1</td>
<td>0.2mW</td>
<td>0.2mW</td>
<td>0.2mW</td>
<td>0.2mW</td>
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<tr>
<td>Efficiency (%)</td>
<td>28%</td>
<td>32%</td>
<td>15%</td>
<td>10%</td>
<td>10%</td>
<td>13%</td>
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</table>

VI. CONCLUSION

We have proposed an ultra-low power Bluetooth LE transmitter that demonstrates the best ever reported power efficiency and phase purity, while abiding by the strict 28 nm CMOS technology manufacturing rules. A new switching current source oscillator combines advantages of low supply voltage of the conventional NMOS cross-coupled oscillator with high current efficiency of the complementary push-pull oscillator to reduce the oscillator supply voltage and dissipated power further than practically possible in the traditional oscillators. Furthermore, due to the low wander of DCO, digital power consumption of ADPLL was saved by scaling the rate of sampling clock to the point of its complete shut-down. A fully integrated differential class-E/F2 switching PA is utilized to improve system efficiency at low output power of -3 dBm. Its required matching network was realized by exploiting different behaviors of a 2:1 step-down transformer in differential and common-mode excitations.

**REFERENCES**