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Ultra Wideband Dual-Mode Doherty Power Amplifier Using Reciprocal Gate Bias for 5G Applications

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Abstract—A novel architecture to extend the bandwidth of the Doherty power amplifier (DPA) is presented in this paper. It is illustrated that two DPA modes at different frequency bands can be realized by simply swapping the gate biases of the transistors without changing the matching circuits, and hence ultra wide bandwidth can be achieved by using a single load modulation network in DPA. A dual-mode DPA with 2.8-4.1 GHz bandwidth for Mode I and 2.2-2.7/4.2-4.8 GHz bandwidth for Mode II using commercial GaN transistors is designed and implemented to validate the proposed architecture. The fabricated DPA attains a measured 7.5-11.7 dB gain and 39.2-41 dBm saturated power. 35.0% to 49.7% drain efficiency is obtained at 6 dB output power back-off for the designed dual-mode bands. When driven by a 10-carrier 200 MHz OFDM signal with 7.7 dB peak to average power ratio, the proposed DPA achieves adjacent channel leakage ratio of better than -50 dBc after digital predistortion at 2.5/3.5/4.5 GHz with average efficiency of 46.0/35.7/33.0%. This simple configuration provides a promising solution for 5G, where multiple frequency bands in sub-6 GHz will be deployed.

Index Terms—Broadband, Doherty power amplifier, dual-mode, high efficiency, multi-band, wideband, 5G

I. INTRODUCTION

MODERN wireless communication systems often employ modulated signals with high peak to average power ratio (PAPR) to improve spectrum efficiency. It demands high efficiency from radio frequency (RF) power amplifiers (PAs) at back-off power in order to enhance the average power efficiency of the system. Many back-off power efficiency improvement techniques for RF PAs have been developed in past decades. Doherty power amplifier (DPA), firstly introduced in [1], is one of the most widely used architectures in modern wireless transmitters, especially in cellular base-stations [2]–[5].

Driven by specific applications, e.g., 3GPP and 4G Long-Term-Evolution (LTE), most DPA developments have been focused on frequency bands below 3 GHz [6]–[12]. The next generation wireless communication system, i.e., 5G, will employ new core air-interfaces with frequency bands from 3 to 6 GHz, e.g., Band N77 from 3.3 GHz to 4.2 GHz and Band

N79 from 4.4 GHz to 5.0 GHz [13], [14], to provide larger signal bandwidths. In the meantime, the LTE bands, e.g., 3GPP Bands No. 40 of 2300 MHz - 2400 MHz and No. 41 of 2496 MHz - 2690 MHz [14], will continue to be used in the 5G system. It is thus desirable to have DPAs operated in a wide range of frequency bands.

To support multimode/multiband operations, bandwidth extension techniques for DPAs have received widespread attention recently. By employing techniques such as post-matching networks [7]–[9], integrated compensating reactance [10] and continuous mode operations [11], [12], bandwidth of the DPAs can be greatly extended. These mentioned techniques mainly focus on the design of broadband load modulation networks. The bandwidth expansion of DPAs at architecture level has also been explored, such as dual input [2], [3] or bias adaptation [15]. Other techniques for improving average efficiency such as load modulated balanced PAs [16] and Doherty-like multi-transistors combing PAs [17] also extend the bandwidth to higher than 3 GHz to meet the requirements for the 5G systems. Nevertheless, the bandwidths of DPAs are still limited and it is very challenging to design a high efficiency Doherty PA to cover the full bandwidth of 5G, e.g., from 2 to 5 or 6 GHz.

In this paper, a new Doherty configuration is presented to extend the bandwidth of the DPA to cover a multi-GHz range. It is illustrated that, with a proper design, the same broadband load modulation network can be used for the DPA to operate at two modes at different frequency bands by using a pair of reciprocal gate biases without any changes in the circuits. A DPA using commercial GaN devices with bandwidth of 2.8-4.1 GHz for Mode I and 2.2-2.7/4.2-4.8 GHz for Mode II is designed and implemented employing the proposed structure. For the fabricated PA, Doherty operation can be well obtained for both the two designed modes and more than one octave bandwidth is achieved. The combined bandwidth of the two modes of the proposed DPA covers almost all the sub-6 GHz frequency bands for 5G applications.

The remaining part of the paper is organized as follows, Section II demonstrates the operation theory of the proposed DPA. Section III shows the detailed procedures of realizing the DPA with the Cree40006s transistor on a 31 mil Rogers 5880 substrate. In Section IV, the experimental results are presented with a conclusion given in Section V.
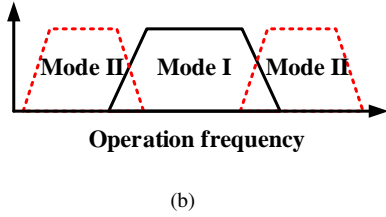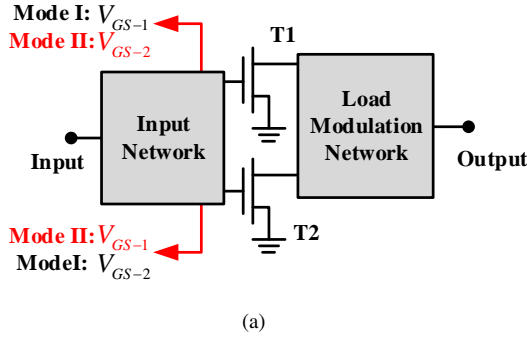
(a)

(b)

Fig. 1. Concept of the proposed dual-mode DPA (a) block diagram; (b) frequency bands coverage.

II. THEORETICAL ANALYSIS OF THE PROPOSED DPA

The Doherty power amplifier usually combines two amplifiers through a load modulation network at output. In a conventional design, one of the amplifiers, i.e., carrier amplifier, is biased for class AB operation, while the other, i.e., peaking amplifier, is biased at class C mode. At high input power levels, both amplifiers are active and deliver power to the load. When the input power is low, only the carrier amplifier is active. To maintain the efficiency at power back-off , the load resistance appearing to the carrier amplifier must be increased via the load modulation network when the input power is reduced. Due to intrinsic limits of the circuits, it is difficult to provide the optimum matching across wide bandwidth at a single operation mode in DPA. Multimode and multiband designs have been proposed to extend the bandwidth but these designs usually involve complicated circuits or control units.

In this work, we propose a simple broadband dual-mode DPA architecture, shown in Fig. 1. The core idea is to realize the Doherty characteristics in different modes at different frequency bands by simply switching the gate voltages, V_{GS-1} and V_{GS-2}, shown in Fig. 1(a), of two identical transistors without changing the circuits. In Mode I, the transistor 1 (T1) is biased with V_{GS-1} at class AB mode as the carrier amplifier while the transistor 2 (T2) is biased with V_{GS-2} at class C mode as the peaking amplifier. In Mode II, the matching networks are the same, but the gate biases of T1 and T2 are swapped and thus the carrier and peaking amplifiers are exchanged, namely, T1 becomes peaking and T2 becomes carrier. The frequency responses of the load modulation network at different modes are different. With a proper design, if in Mode I the PA can cover the middle frequency band, while in Mode II it can cover the remaining two bands at the two ends, as shown in Fig. 1(b), the combined frequency band of the DPA will be very wide.
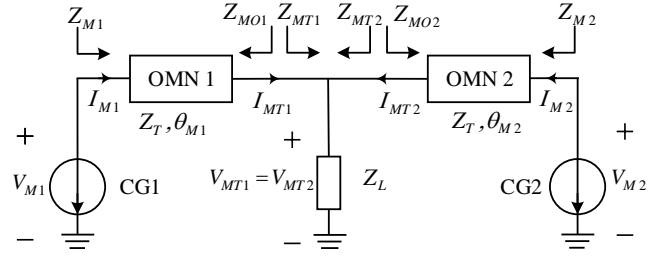

Fig. 2. Load modulation network of the proposed DPA.

A. Load Modulation Analysis

To implement the above idea, we propose a symmetric configuration and use a generalized output matching network (OMN) for carrier and peaking amplifier, respectively, as shown in Fig. 2, where the two transistors are represented by current generators (CG).

To simplify analysis, we assume that the parasitic of the transistors and package parameters can be entirely absorbed into the OMNs. For this schematic, the proposed two modes are defined as followed: in Mode I, CG1 is biased at Class-AB mode as the carrier device and CG2 is biased at Class-C mode as the peaking device while in Mode II, CG1 becomes the peaking device and CG2 is the carrier device.

Let's assume the OMNs can realize matching from Z_T to Z_T in the designed band and θ_{M1} and θ_{M2} is the phase shift of OMN 1 and OMN 2, respectively. The ABCD matrix of the lossless OMNs can be described as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T\sin\theta \\ j\frac{\sin\theta}{Z_T} & \cos\theta \end{bmatrix} \quad (1)$$

where Z_T can be set to R_{opt}, the optimum load impedance for Class-B operation of the device.

Therefore, the voltage and current relationship between CG plane and the combining node can be expressed as,

$$\begin{bmatrix} V_M \\ I_M \end{bmatrix} = \begin{bmatrix} \cos\theta_M & jZ_T\sin\theta_M \\ j(\sin\theta_M)/Z_T & \cos\theta_M \end{bmatrix} \begin{bmatrix} V_{MT} \\ I_{MT} \end{bmatrix} \quad (2)$$

From (2), we can calculate the current at CG plane as,

$$I_M = V_{MT} \cdot (j\sin\theta_M/Z_T) + \cos\theta_M \cdot I_{MT} \quad (3)$$

where the voltage at the combining node is,

$$V_{MT} = (I_{MT1} + I_{MT2}) \cdot Z_L \quad (4)$$

Z_L represents the combining load of the two branches, which is equal to $Z_T/2$.

To meet the equal-phase combining condition at saturation (at the combining node) for the symmetrical Doherty operation, the following current relationship should be satisfied,

$$I_{MT2,sat} = I_{MT1,sat} \quad (5)$$

From (3), (4) and (5) we can obtain,

$$I_{M,sat} = I_{MT,sat} \cdot (\cos\theta_M + j\sin\theta_M) = I_{MT,sat} \cdot e^{j\theta_M} \quad (6)$$

Therefore, in both Mode I and Mode II, the current generated by CG1 and CG2 should satisfy the following relationship,

$$I_{M1,sat} = I_{M2,sat} \cdot e^{j(\theta_{M1} - \theta_{M2})} \qquad (7)$$

Equation (7) indicates that the equal-phase combining condition at saturation can be satisfied by adding a phase compensation network with the phase shift of $(\theta_{M1} - \theta_{M2})$ at the input of CG1 for both Mode I and Mode II.

When the equal-phase combining condition in (5) is satisfied, the load impedance at the combining node can be calculated as,

$$Z_{MT1,sat} = Z_{MT2,sat} = Z_T \qquad (8)$$

On the other hand, the matching impedance of the OMN at CG plane Z_M can be expressed as,

$$Z_M = \frac{Z_{MT}A + B}{Z_{MT}C + D} \qquad (9)$$

where Z_{MT} is the load impedance of each amplifier branch before the combining point. Substituting (1) into (9), we obtain

$$Z_{M1} = Z_T \frac{Z_{MT1} + jZ_T tan\theta_{M1}}{Z_T + jZ_{MT1} tan\theta_{M1}} \qquad (10)$$

$$Z_{M2} = Z_T \frac{Z_{MT2} + jZ_T tan\theta_{M2}}{Z_T + jZ_{MT2} tan\theta_{M2}} \qquad (11)$$

where Z_{M1} and Z_{M2} are the matching impedances of OMNs at the CG planes.

Substituting (8) into (10) and (11) we can know,

$$Z_{M1,sat} = Z_{M2,sat} = Z_T \qquad (12)$$

which means that the required impedance for the carrier and peaking branches are both matched to R_{opt}, meeting the condition for Doherty operation at saturation for both Mode I and Mode II.

In Mode I, only CG1 is active at back-off, CG2 is not yet turned on and it presents an open circuit at CG2 plane. The branch impedance $Z_{MT1,bo} = Z_L // Z_{MO2,bo}$, in which $Z_{MO2,bo}$ represents the output impedance of CG2 branch and can be expressed as,

$$Z_{MO2,bo} = Z_T \frac{1}{jtan\theta_{M2}} \qquad (13)$$

Substituting (13) into (10), we can obtain the back-off matching impedance $Z_{M1,bo}$ of Mode I as

$$Z_{M1,bo} = Z_T \frac{1 - tan\theta_{M1} tan\theta_{M2} + j2 tan\theta_{M1}}{2 + jtan\theta_{M1} + jtan\theta_{M2}} \qquad (14)$$

To satisfy Doherty operation, $Z_{M1,bo}$ should be matched to $2R_{opt}$. As we know, the phase of the OMN is frequency dependent. Let's set $\theta_{M1} = -90°$ and $\theta_{M2} = -180°$ at the center frequency. If we sweep θ_{M1} and θ_{M2} with the normalized frequencies, the normalized resistance of $Z_{M1,bo}$ can be shown in Fig. 3(a), where we can see the DPA can operate within a wide frequency band.

In Mode II, CG2 becomes the carrier while CG1 is the peaking. Equation (12) can still be established at saturation, as the proposed DPA employs a symmetric structure. At back-off, the carrier branch is changed to the CG2 branch and the
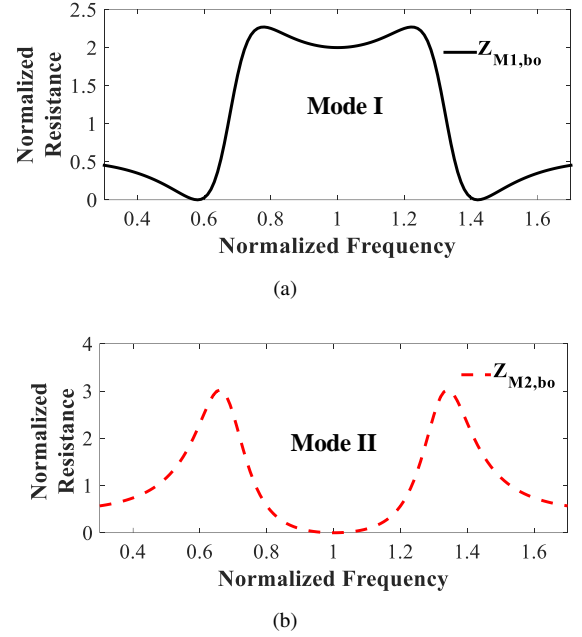

(a)

(b)

Fig. 3. The normalized back-off resistance vs. normalized frequency of (a) Mode I (b) Mode II.

CG1 is turned off. Thus, $Z_{MT2,bo} = Z_L // Z_{MO1,bo}$, where $Z_{MO1,bo}$ can be expressed as,

$$Z_{MO1,bo} = Z_T \frac{1}{jtan\theta_{M1}} \qquad (15)$$

Substituting (15) into (11), the back-off matching impedance $Z_{M2,bo}$ of Mode II can be calculated as,

$$Z_{M2,bo} = Z_T \frac{1 - tan\theta_{M1} tan\theta_{M2} + j2 tan\theta_{M2}}{2 + jtan\theta_{M2} + jtan\theta_{M1}} \qquad (16)$$

As mentioned earlier, in the proposed DPA, we only switch the biases but do not change the circuits when moving from Mode I to Mode II. Therefore, θ_{M1} and θ_{M2} stay the same. If we sweep θ_{M1} and θ_{M2} with the normalized frequencies again, the normalized resistance of $Z_{M2,bo}$ is shown in Fig. 3(b), where we can see that, although the PA can no longer operate as Doherty at the center frequency band, at each sideband, the output impedance can still be made close to the optimum and thus Doherty operation can still be achieved. Therefore, from Fig. 3, we can see that if the bandwidth characteristics can be combined properly between two modes, a wideband DPA can be obtained. Further design considerations will be discussed in detail in the following subsections.

B. Bandwidth Analysis

From the above equations, we can see that the required impedance of the proposed DPA at saturation for both Mode I and Mode II can be automatically achieved when the equal-phase combining condition is satisfied. Therefore, the bandwidth performance is mainly determined by the back-off impedance. In Doherty design, the bandwidth of a DPA can be defined with power contours relating to a certain back-off

output power level, which is called "power bandwidth" [18]–[20]. In addition, the back-off output power level of a DPA can be defined as,

$$BO_p = 10 \log_{10}(2\gamma) \tag{17}$$

where γ represents the ratio of the back-off resistance related to R_{opt}. The δ dB power bandwidth can be defined by determining the frequency range in which the back-off impedance stays within the δ dB power contour on the Smith chart. Therefore, to obtain the δ dB power bandwidth for the proposed DPA, the real part of the back-off impedance and admittance are required to satisfy the following two equations [21], [22]:

$$Re(Z_{bo}) \geq \gamma R_{opt} 10^{-\delta/10} \tag{18}$$

$$Re(Y_{bo}) \geq \frac{10^{-\delta/10}}{\gamma R_{opt}} \tag{19}$$

The required back-off impedances of the proposed DPA are expressed by phases θ_{M1} and θ_{M2} and Z_T of OMNs in (14) and (16). Thus, to define the bandwidth of the proposed DPA, it is crucial to discuss the impact of θ_{M1} and θ_{M2}. θ_{M1} and θ_{M2} are frequency dependent and can be defined as,

$$\theta_{M1} = \theta_1 + \alpha\pi(1-f) \tag{20}$$

$$\theta_{M2} = \theta_2 + \beta\pi(1-f) \tag{21}$$

where f refers to the operation frequency, which is normalized to the center frequency f_c, θ_1 and θ_2 is the reference phase at f_c and α and β is the changing factor of the phase change with the operation frequency of OMN 1 and OMN 2, respectively.

From (14), (16), (20) and (21), we can see that $Z_{M1,bo}$ and $Z_{M2,bo}$ can be expressed by using α, β, θ_1, θ_2 and f. If these parameters are substituted into (18) and (19), the resistances of $Z_{M1,bo}$ and $Z_{M2,bo}$ are now restricted to the condition (18) and the conductances of $Y_{M1,bo}$ and $Y_{M2,bo}$ are restricted to the condition (19). With fixed γ and δ, and with the certain selection of α, β, θ_1 and θ_2, the bandwidth of Mode I can be solved by inequalities in relation to $Z_{M1,bo}$ and $Y_{M1,bo}$, and the bandwidth of Mode II can be solved by inequalities relating to $Z_{M2,bo}$ and $Y_{M2,bo}$. To clearly illustrate the impact of different parameters, further discussions are given below:

1) Selection of α and β: To simplify the analysis, θ_1 is fixed to $-90°$, and θ_2 is set to $-180°$. Let's take an example with $\beta = 1.3$ and vary α to show the bandwidth variations, assuming $\alpha < \beta$. The normalized resistances and conductances values versus the normalized frequencies are shown in Fig. 4(a) and Fig. 4(b), respectively. If we use $\gamma = 2.5$ and $\delta = 1.5$ to define the boundary condition in (18) and (19), the bandwidth of the DPA in Mode I can be found as the frequency bands where the resistance and conductance values are higher than the boundary, as shown in Fig. 4(a) and Fig. 4(b). Following the same rule, the bandwidth of the DPA in Mode II can be found in the same way as shown in Fig. 4(a) and Fig. 4(b).

Table I summarizes the obtained bandwidth shown in Fig. 4(a) and Fig. 4(b). Mode I-R and Mode I-C represents the bandwidth of Mode I obtained from the intersection of resistance and conductances line with the boundary line in Fig. 4(a)
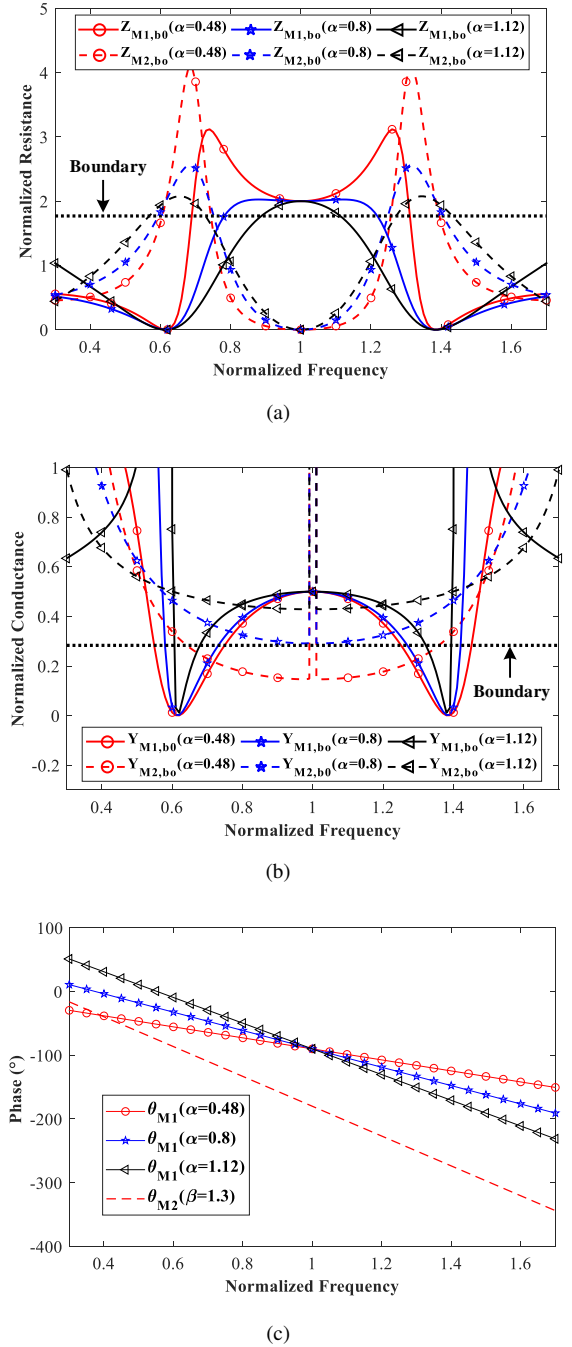

(a)

(b)

(c)

Fig. 4. Bandwidth of (a) normalized resistance, (b) normalized conductance and (c) phase relationship of dual-modes with constant $\beta=1.3$ and varied α.

and Fig. 4(b), respectively. The Doherty operation of Mode II appears as dual-band, thus Mode II-L and Mode II-H are introduced to represent the lower and higher frequency bands for Mode II. The total bandwidth of the proposed DPA is the combined bandwidth of Model I and Mode II.

From Fig. 4(a) and Table I, we can see that the impedance distribution is symmetric to the center frequency, which means the bandwidth is also symmetric. In addition, the bandwidth of Mode I is decreased with α rising from 0.48 to 1.12, while Mode II bandwidth is increased. Moreover, when α is far from 0.8, the invalid bands between Mode II and Mode I are wider.

TABLE I
NORMALIZED BANDWIDTH OF MODE I AND MODE II FOR DIFFERENT
VALUES OF α WHEN $\beta = 1.3$

α	Mode I-R	Mode II-L-R	Mode II-H-R
0.48	0.69-1.31	0.61-0.74	1.26-1.39
0.8	0.78-1.22	0.59-0.75	1.25-1.41
1.12	0.89-1.11	0.57-0.73	1.27-1.43
α	Mode I-C	Mode II-L-C	Mode II-H-C
0.48	0.3-0.55&0.75-1.25&1.45-1.7	0.3-0.64	1.36-1.7
0.8	0.3-0.58&0.73-1.27&1.42-1.7	0.3-1.7	0.3-1.7
1.12	0.3-0.61&0.68-1.32&1.39-1.7	0.3-1.7	0.3-1.7
α	Mode I	Mode II-L	Mode II-H
0.48	0.75-1.25	0.61-0.64	1.36-1.39
0.8	0.78-1.22	0.59-0.75	1.25-1.41
1.12	0.89-1.11	0.57-0.73	1.27-1.43

TABLE II
NORMALIZED BANDWIDTH OF MODE I AND MODE II FOR DIFFERENT
VALUES OF θ_1 WHEN $\theta_2 = -180°$

θ_1	Mode I	Mode II-L	Mode II-H
$-72°$	1.07-1.25	058-0.72	1.26-1.34
$-90°$	0.78-1.22	0.59-0.75	1.25-1.41
$-108°$	0.75-0.93	0.6-0.66	1.28-1.42

the proposed DPA.

When $\alpha \geq \beta$, from (14), (16), (20) and (21), we can see that the bandwidth of Mode I becomes narrower and be concentrated around f_c. When β is smaller than a certain α, the bandwidth of Mode II will disappear.

2) Selection of θ_1 and θ_2: The bandwidths are also impacted by θ_1 and θ_2. To simplify the analysis, α and β are fixed to 0.8 and 1.3, when considering the impact of the reference phases. The normalized resistance and normalized conductance with different values of θ_1 when $\theta_2 = -180°$ are shown in Fig. 5(a) and Fig. 5(b). Using the same method mentioned above, the bandwidths for different modes are calculated in Table II. From Fig. 5(a) and Fig. 5(b), the lines shape of the impedance becomes asymmetric to f_c. The bandwidths are impacted by this asymmetry, as shown in Table II.

From the above results, we can see that the realized bands can be flexibly configured based on different value of the parameters of OMNs. In order to cover a bandwidth as wide as possible using Mode I and Mode II, symmetrical bandwidth is required. In this situation, $\theta_{M1} = -90°$ and $\theta_{M2} = -180°$ should be set. In addition, the value of α and β shall be determined to facilitate a easy implementation of OMNs.

C. Back-Off Efficiency Performance

In the conventional symmetric DPA configuration, back-off matching impedance of $2R_{opt}$ for the carrier amplifier is usually required to achieve high efficiency performance at 6 dB back-off. However, in the proposed DPA, larger than $2R_{opt}$ back-off matching resistance can occur within the wide operation bandwidth. For example, when the configuration of $\theta_{M1} = -90°$, $\theta_{M2} = -180°$, $\alpha = 0.5$ and $\beta = 1$ is used, the normalized resistances of Mode I and Mode II are shown in Fig. 3. Within the operation bandwidth, the back-off matching resistance is close to $2R_{opt}$ in Mode I, while it ranges from $2R_{opt}$ to $3.045R_{opt}$ in Mode II.

To obtain high back-off efficiency in a Doherty PA, the gate bias of the peaking amplifier is usually configured according to the back-off resistance value. While the back-off level is defined by (17), when the back-off matching resistance is higher than $2R_{opt}$, high efficiency can be obtained over larger than 6 dB output power range if the gate bias is properly configured based on the resistance value $3.045R_{opt}$ in Mode II [23], [24]. However, this may lead to a narrow operation bandwidth because the back-off resistance value decreases at other frequencies in Mode II. To achieve a wider bandwidth for Mode II, the proposed DPA can be over-driven to a certain extent at back-off [25].
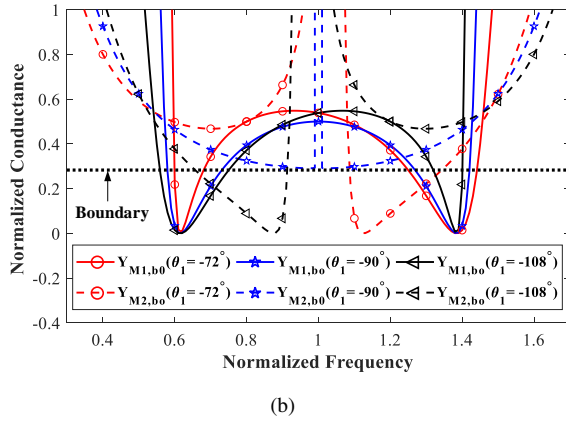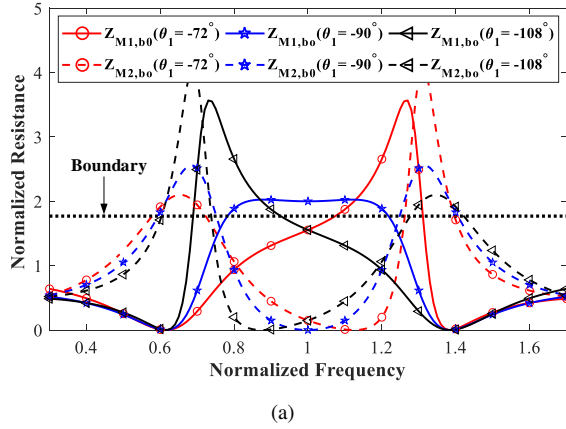

(a)

(b)

Fig. 5. (a) Normalized resistance of dual-mode with constant $\theta_{M2}=180°$ and varied θ_{M1} (b) Normalized conductance of dual-mode with constant $\beta=1.3$ and varied α.

The corresponding phase variations of OMN 1 and OMN 2 versus the normalized frequencies are shown in Fig. 4(c). For example, when α=0.8 and β=1.3, the phase of OMN 1 changes from -10.8° to -190.8° with the normalized frequency changing from 0.3 to 1.7. The phase of OMN 2 changes from $-16.2°$ to $-343.8°$. These figures can be utilized to design
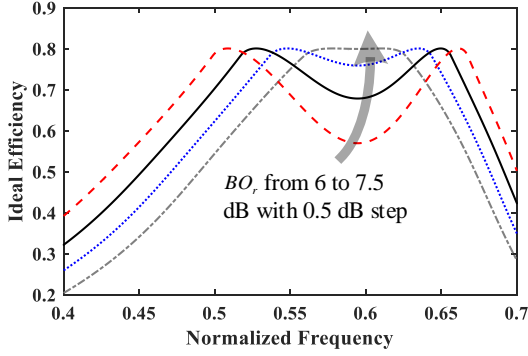
Fig. 6. Ideal back-off efficiency for Mode II versus frequency for different values of BO_r.
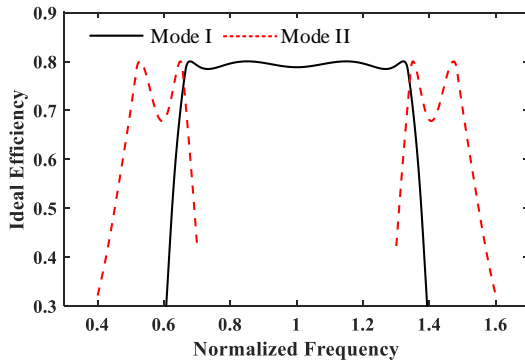

Fig. 7. Ideal back-off efficiency for Mode I and Mode II versus frequency when BO_r is equal to 6 dB for Mode I and 6.5 dB for Mode II when $\theta_{M1} = -90°$, $\theta_{M2} = -180°$, $\alpha = 0.5$ and $\beta = 1$.

Let's assume the gate bias is set to make the peaking device turn on at BO_γ dB back-off. The over-driven level of the proposed DPA at back-off can be defined as $BO_p - BO_\gamma$. From (14), (16) and (17), the over-driven level can be easily calculated. By employing the over-driven current waveform introduced in [25], [26], we can obtain the back-off efficiency performance of the proposed DPA. Fig. 6 presents the ideal back-off efficiency versus frequency for different values of BO_r in Mode II. Due to the symmetry of the two bands in Mode II, Fig. 6 only shows the lower band. It can be seen that both efficiency and bandwidth change with BO_r, which indicates that in practice, BO_r and the gate bias value of the peaking amplifier should be selected based on the performance trade-off between the bandwidth and back-off efficiency.

In the proposed design, we can set BO_r as 6.5 dB, which gives the minimum back-off efficiency of 67% in the Mode II bands. On the other hand, for Mode I, the normalized matching resistance at back-off is close to $2R_{opt}$ within a wide frequency range, so $BO_r = 6$ dB can be set. We can obtained the back-off efficiency performance of the proposed DPA in both Mode I and Mode II, as shown in Fig. 7. It can be seen that, using the proposed configuration, the high-efficiency bandwidth can be obviously extended. The fractional bandwidth with higher than 67% ideal back-off efficiency is expanded from 70% to 101%.
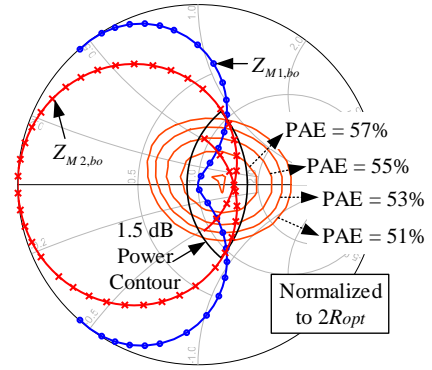

Fig. 8. Simulated back-off impedance with power and efficiency contours when $\theta_{M1} = -90°$, $\theta_{M2} = -180°$, $\alpha = 0.5$ and $\beta = 1$.

The above analysis shows the ideal back-off efficiency performance of the proposed dual-mode DPA. However, for a practical transistor, the efficiency will drop to some extent at the back-off region. Moreover, the bandwidth analysis in the previous subsection is based on the power contours, the back-off efficiency performance within the working bandwidth might not be clearly obtained. In order to observe the back-off efficiency performance of the proposed DPA clearly within the resulting bandwidth, the efficiency contours at the back-off can be introduced. As an example, in Fig. 8, the de-embedded back-off efficiency contours of a commercial GaN transistors from load-pull simulation at 4.5 GHz are used to observe the efficiency performance of the proposed DPA when $\theta_{M1} = -90°$, $\theta_{M2} = -180°$, $\alpha = 0.5$ and $\beta = 1$. It should be noticed that, the bandwidth defined by the 1.5 dB power contour in Fig. 8 is almost the same to the 67% ideal efficiency bandwidth obtained from Fig. 7. From Fig. 8, we can see that, by employing the back-off impedance within the defined power contour, the back-off efficiency can be kept higher than 51% PAE, which illustrates that the proposed architecture can achieve high back-off efficiency.

D. Phase Compensation

From the above analysis we can know, the bandwidth extension of the DPA can be realized by using the proposed dual-mode method. However, as shown in (7), the signals of two branch amplifiers can only be combined properly with suitable phase compensation networks and then the Doherty operation can be satisfied. Thus, the phase compensation network should be designed properly.

Depending how the load modulation network is designed, the phase compensation network can be simple or becomes very complex. To simplify the design, in this work, we divide OMN 2 into two parts: one part is the same as OMN 1 and the other is an off-set network which can be realized by using a transmission line. The schematic of this configuration is shown in Fig. 9, where the OMN 1 is realized by using an equivalent quarter wavelength network (EQWN) with characteristic impedance of R_{opt}, where $\theta_1 = -90°$. The OMN 2 includes two parts: the EQWN and an off-set line, and let the phase of OMN 2 satisfy the condition of $\theta_2 = -180°$. By using this
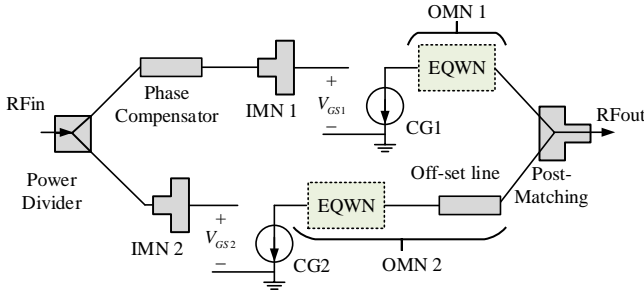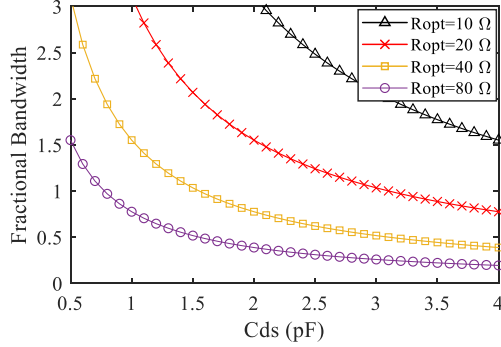
Fig. 9. Proposed dual-mode DPA structure with phase compensator

Fig. 10. Fractional bandwidth under Bode-Fano limitation for different R_{opt} and C_{ds} at 3.5 GHz centre frequency.

design, the phase compensation conditions in (7) can be easily satisfied.

In Mode I, the phase of the off-set line is $-\frac{\pi}{2}f$. Therefore, the relationship between θ_{M1} and θ_{M2} in this situation can be expressed as,

$$\theta_{M2} - \theta_{M1} = -\frac{\pi}{2} \cdot f \qquad (22)$$

which presents the phase need to be compensated. It is obvious that this phase characteristic can be compensated by another off-set line setting in front of the input network of CG1 as the phase compensator shown in Fig. 9. In Mode II, equation (22) is also established, thus the phase can be compensated. In addition, substituting (22) into (20) and (21) we can obtain $\beta = \alpha + 0.5$. With this relationship, it is easy to determine the specific value of α and β according to the network structure of OMN 1.

It is worth mentioning that, the above simple structure is just one example of the proposed dual-mode configurations. With different α and β, various distributions of normalized carrier resistances can be obtained and thus the PA can be designed to be operated at different frequency ranges. This flexibility can be used to design different dual-mode DPAs based on the specific applications.

E. Practical Bandwidth Limitation Discussion

In subsection II-A and II-B, we assume the parasitic and package parameters of the active device can be absorbed in the OMNs. The absorption may limit the bandwidth of the DPA because the frequency response of the network depends on

the required R_{opt} and the capacitance values of the parasitic. Generally, the fundamental bandwidth limitation of a matching network is determined by the Bode-Fano limitation. If only the drain to source capacitor C_{ds} is the main concern here, for the matching target with a capacitive load, the following equation can be obtained based on the Bode-Fano limitation as,

$$\int_0^\infty ln(\frac{1}{|\Gamma|})d\omega \leq \frac{\pi}{RC} \qquad (23)$$

where we can set $R = R_{opt}$, $C = C_{ds}$ and $\Gamma = \Gamma_{min}$ indicates inside of the operation band, while $\Gamma = 1$ represents outside of the band. The center frequency is defined as $\omega_0/2\pi$. The fractional bandwidth $\Delta\omega$ can be described as followed,

$$\Delta\omega \leq \frac{\pi}{\omega_0 R_{opt} C_{ds} \ln(1/\Gamma_{min})} \qquad (24)$$

Let $\Gamma_{min} = 0.1$ and set the center frequency at 3.5 GHz, the fractional bandwidth versus C_{ds} can be obtained as shown in Fig. 10, where we can see that the bandwidth limitation does not affect the DPA design significantly if R_{opt} and C_{ds} are sufficiently small. In fact, in most commercial GaN devices, R_{opt} can vary from tens to a few ohms, while the related C_{ds} varies from fractional picofarad to a few picofarads. And in practical design, the realisable fractional bandwidth for Doherty in each mode is usually not over one octave. From the Bode-Fano limitation equation (24) and Fig. 10, we can conclude that the bandwidth of the proposed DPA is not limited by R_{opt} and it is reasonable to absorb C_{ds} into OMN design if C_{ds} is small.

It should be noticed that, the above analysis does not consider the circuits structure of the matching network. To further verify whether the proposed DPA architecture is still workable when different values of R_{opt} and C_{ds} are used, it is more practical to consider the impact of designed matching networks. Two matching examples with different OMN1 and OMN2 are simulated here. The circuits structure is the same as that shown in Fig. 9. The impedance ratio of the entire output network is mainly realized by the post-matching network. Because high-order matching networks can be used to design the post-matching network, the bandwidth limitation mainly arises from the two OMNs. Moreover, because the impedance ratio of the two OMNs is equal to 1 (from R_{opt} to R_{opt}), the bandwidth is not limited by different values of R_{opt}. In this situation, the limitation is mainly from the impact of the value of C_{ds} when a specific value of R_{opt} is used.

Two examples of matching for devices with different power levels are given here to verify the adaptability of the proposed DPA architecture. R_{opt} of 32 and 15 Ω and C_{ds} of 1.22 and 2.6 pF are chosen to model two different active devices with 10 and 25 watts output power, respectively. The target bandwidths are supposed to cover wider than 40% fractional bandwidth in Mode I. Following the analysis in subsection II-B, $\alpha = 0.7$ and $\beta = 1.25$ are chosen, the related phase variation is from $-40°$ to $-140°$ for OMN1, and from $-90°$ to $-270°$ for OMN2. A low-pass circuits structure with drain bias line is used to design the required OMN1 for both the two devices. The OMNs are designed in two different frequency bands for the two devices. The back-off impedance of the related dual
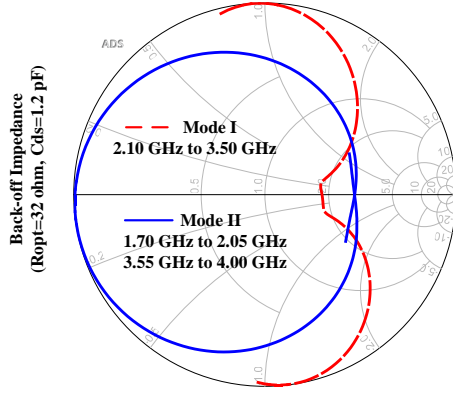
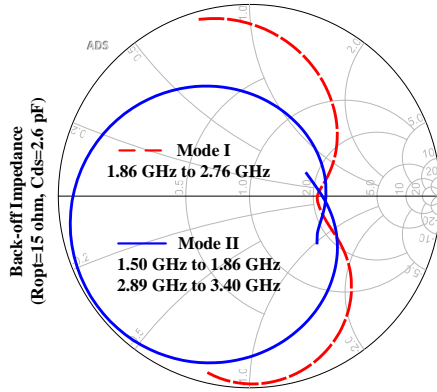Fig. 11. Simulated back-off impedance in the proposed two Modes when $R_{opt} = 32\ \Omega$ and $C_{ds} = 1.22$ pF.

Fig. 12. Simulated back-off impedance in the proposed two Modes when $R_{opt} = 15\ \Omega$ and $C_{ds} = 2.6$ pF.

modes are shown in Fig. 11 and Fig. 12 on the Smith chart. The related reference impedance of the Smith chart is set to 32 and 15 Ω, respectively. From the results shown in Fig. 11 and Fig. 12, we can see that bandwidth of 1.7 to 4.0 GHz and 1.5 to 3.4 GHz can be achieved for the 32 and 15 Ω R_{opt} devices. The simulated dual-mode impedance is close to that predicted by the theory. The above examples illustrate that the proposed architecture is applicable to devices with different R_{opt} and C_{ds}.

III. DESIGN OF ULTRA WIDEBAND DUAL-MODE DPA

To demonstrate the proposed design, commercial GaN HEMTs CGH40006s from Wolfspeed were used for the proposed DPA because its good performance when operating at frequencies higher than 4 GHz. The DPA was fabricated on 31 mil Rogers 5880 substrates with dielectric constant of 2.2. The drain supply voltage V_{DS} was set as 28 V. The package parasitic of the device was de-embedded first. The circuit that was used to model the parasitic and package is shown in Fig. 13. Based on the load-pull simulation and S-parameters of transistor when the device is turned off, the capacitance and inductance values of 0.8 pF, 0.5 nH, 0.1 pF, 0.1 nH are estimated over frequencies ranging from 2.0 to 5.0 GHz. The method of estimation introduced in [27] is used. In addition,
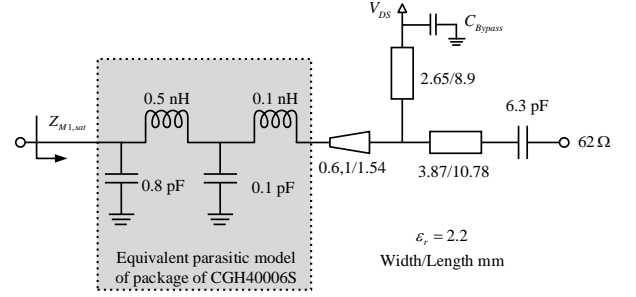

Fig. 13. Circuit of EQWN design.

the knee voltage of the transistor was estimated as 4.5 V and the maximum drain current was 0.75 A. R_{opt} was calculated as 62 Ω.

A. Design Parameters Calculation

From the discussion in Section II we can know, the bandwidth of the proposed architecture depends on the network parameters θ_1, θ_2, α and β. To achieve ultra-wideband Doherty operation, θ_1 and θ_2 were chosen as $-90°$ and $-180°$ at the center frequency of 3.6 GHz. To satisfy the equal phase condition mentioned in section II and achieve wide high efficiency bandwidth at back-off, $\alpha = 0.93$ and $\beta = 1.43$ were set, covering the frequency band from 2.344 to 4.856 GHz with higher than 67% ideal back-off efficiency. In this configuration, the range of θ_{M1} in the target band changes from $-31.58°$ to $-148.4°$, and θ_{M2} changes from $-90.17°$ to $-269.8°$. Once these parameters were determined, the OMNs and the phase compensation network can be designed.

B. Dual-Mode DPA Design

The schematic of the designed dual-mode DPA is shown in Fig. 14. The design details are given as follows.

Firstly, an EQWN was designed as OMN 1 with the consideration of absorbing the parasitic parameters of transistor. A T-shape transmission line (TL) structure was utilized, as shown in Fig. 13. In the proposed design, since the matching target of EQWN was simple, the specific parameters of the TLs in EQWN were therefore directly optimized to achieve the required phase range and the target matching impedance with the same load value of R_{opt}. For OMN 2, the same EQWN circuit was employed with an added TL with characteristic impedance of R_{opt} to tune the phase of OMN 2, as shown in Fig. 14. Drain bias lines for T1 and T2 were included in both OMN 1 and OMN 2. All the widths and lengths of the used TLs are given in Fig. 14.

Fig. 15(a) demonstrates the phase shift of EQWN (OMN 1) and EQWN plus an off-set line (OMN 2). From Fig. 15(a), the phase range of OMN 1 in the target band is from $-30°$ to $-156°$. For OMN 2 the phase range is from $-85°$ to $-286°$. The designed phase ranges of these two networks are close to what are required. In Fig. 15(b), the simulated matching impedance of OMN 1 and OMN 2 is shown on the Smith chart with the load impedance set to R_{opt}. The
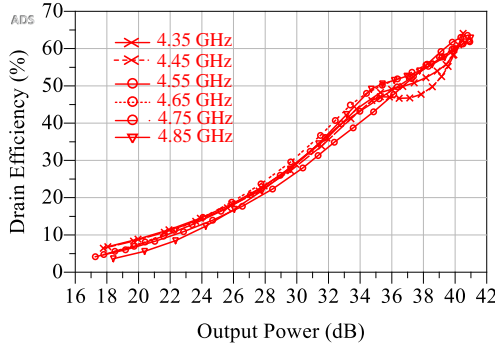
Fig. 14. Schematic of the proposed DPA.

Fig. 15. EM simulation results of the designed OMNs (a) phase shift of OMN 1 and OMN 2 (b) matching impedance of OMN 1 when its load equal to R_{opt}.

Fig. 16. Back-off impedance of the designed DPA (a) Mode I (b) Mode II.

Fig. 17. Simulated drain efficiencies and gains of the fabricated DPA versus output power at different frequencies of (a) Mode I and (b) Mode II.

reference impedance is also set to R_{opt}. Fig. 15(b) shows that the matching impedance of the OMNs is close to R_{opt} across 2.35 to 4.85 GHz.

Secondly, after designing OMN 1 and OMN 2, a post-matching network which realizes the matching from 50 Ω to $R_{opt}/2$ in the designed frequency band covering the two modes was designed by using a stepped TL structure. Once these networks were designed, the back-off impedance of the carrier branch at back-off region for Mode I and Mode II can be obtained, the simulated impedance at back-off region is shown on Smith chart in Fig.16, where we can see that

the impedances are located close to the region defined by the output power contours.

Thirdly, because the proposed DPA uses reciprocal gate biases to set the operations into two different modes, the same input matching networks (IMNs) were used in both RF chains to guarantee the DPA operation in Mode I and Mode II. To compensate for the phase difference between OMN 1 and OMN 2, a 50 Ω transmission line is applied in front of the IMN of T1. Besides, the circuits of the used power divider are shown in Fig. 14. EM simulation of the entire DPA was run in ADS Momentum from Keysight. The V_{GS-1} was set

Fig. 18. Simulated drain efficiencies and gains of the DPA versus output power at high frequency bands with different bias of Mode II.

Fig. 19. Circuits of the OMNs of the dual-mode DPA using Cree 40010F

to -2.9 V with the quiescent current 70 mA, while V_{GS-2} was set to -6 V. It should be noticed that the dimensions of the circuits have been optimized to a certain degree for better DPA performance.

Finally, the simulation results of Mode I and Mode II are shown in the Fig. 17. All simulations in the design procedure were performed with ADS. Frequency range from 2.85 to 4.25 GHz is achieved for Mode I and 2.3-2.75/4.35-4.9 GHz is achieved for Mode II. From Fig. 17(a) and Fig. 17(b), we can see that higher than 40% drain efficiency can be achieved at 6 dB back-off region throughout the entire band.

From the above simulation results, we can see that, in both modes, Doherty operation can be observed, though at some frequencies, e.g., in the higher frequency band of Mode II, the Doherty operation is not obvious. This might be caused by several factors such as the non-ideal second harmonic control and mismatch of the fundamental impedance due to the imperfect parasitic absorbing over wide bandwidth. Moreover, we targeted to cover a very wide bandwidth in the design, the gain of the designed DPA can vary at different frequencies. From Fig. 17(b), we can see that the gain of designed DPA at high frequency band of Mode II is lower than that in lower frequency bands, which leads the peaking amplifier is turned on earlier, and thus decreases the back-off efficiency of the designed DPA. To resolve this, the gate voltage can be slightly adjusted. By setting V_{GS-2} to -7.3 V, the back-off efficiency at higher frequency band can be improved as shown in Fig. 18.

C. Different R_{opt} Application Simulation

To further verify whether the proposed DPA architecture is workable under different R_{opt} conditions, the transistor CGH 40010F has been selected as the active device for another simulation example. The design method is the same as that introduced in the previous two sections. The R_{opt} of the transistor is 32 Ω. $\alpha = 0.7$ and $\beta = 1.25$ are chosen, the related phase variation is from $-40°$ to $-140°$ for OMN1, and from $-90°$ to $-270°$ for OMN2.

The target band is from 1.8 GHz to 4 GHz, and the same Rogers substrate is employed for the design. The schematic of OMN 1 and OMN 2 is shown in Fig. 19. The PMN realize the matching from 50 Ω to 16 Ω. High-order stepped-TL structure
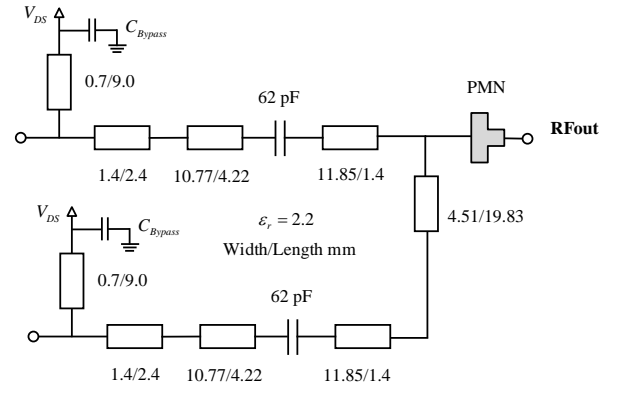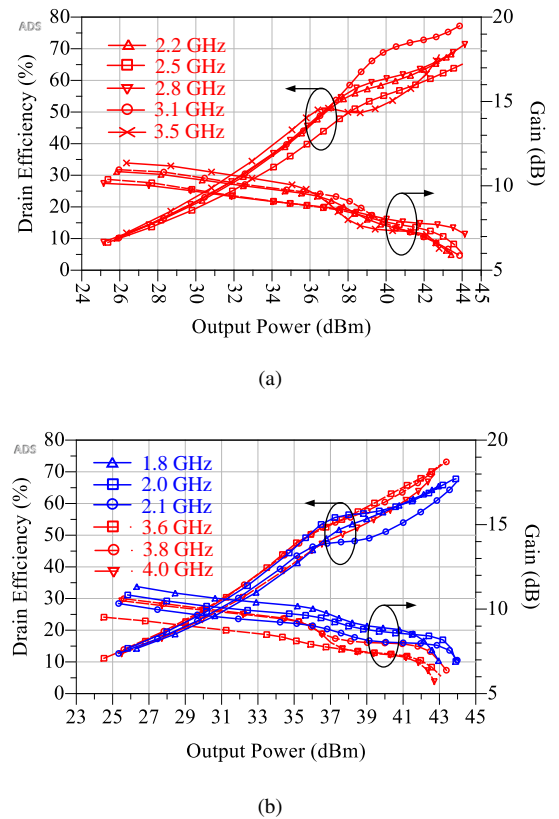

(a)

(b)

Fig. 20. Simulated drain efficiency and gains of the proposed DPA with CGH 40010 versus output power at different frequencies of (a) Mode I and (b) Mode II.

is used to design the PMN and IMNs. The simulated drain efficiency and gains versus output power are shown in Fig. 20, where we can see that the simulated efficiencies at 6 dB back-off are from 47.8% to 58.5% with maximum output power of 43 dBm to 44 dBm throughout the entire designed band. This proves that the proposed design methodology is generic and it can be applied to various different devices.

IV. EXPERIMENTAL RESULTS

To better present the ultra-wideband performance of the proposed architecture, especially for 5G new air-interface
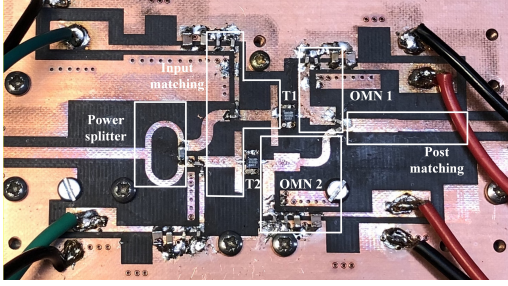
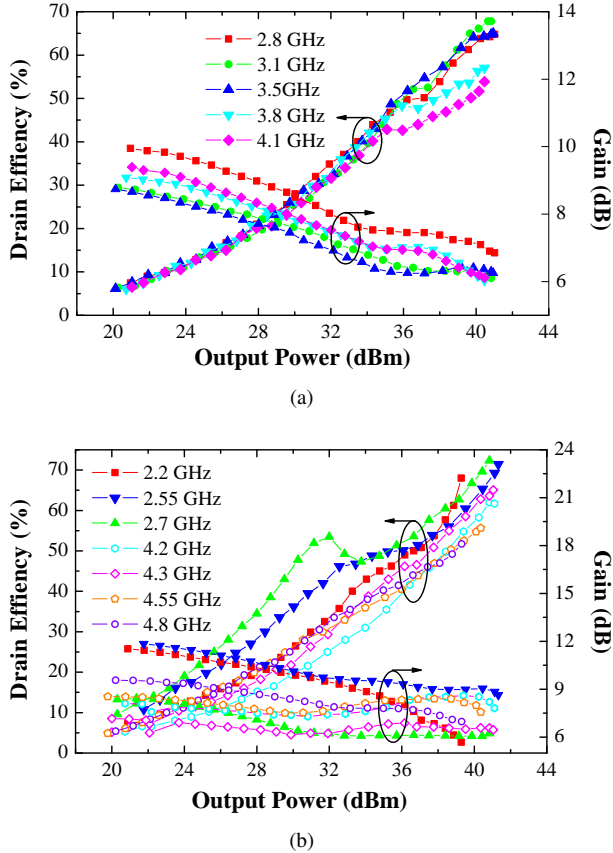Fig. 21. Photo of the proposed DPA circuit.

(a)

(b)

Fig. 22. Measured drain efficiency and gains of the fabricated DPA versus output power at different frequencies of (a) Mode I and (b) Mode II.

applications, the design with CGH40006s which has higher operation frequency was fabricated. The photo of the implemented DPA is shown in Fig. 21. To evaluate the performance, the fabricated PA was measured with both continuous-wave (CW) and modulated signals. Measurements were performed in 2.7-4.2 GHz band for Mode I and 2.2-2.7/4.2-4.8 GHz band for Mode II. In the measurements, the quiescent current of device T1 was set to 70 mA for Mode I, and the gate bias voltage of T2 was set to -6.2 V. For Mode II, the gate biases condition of T1 and T2 was swapped. The CW and modulated signals were both generated by a vector signal generator, and the output power was measured using a spectrum analyzer. To drive the implemented DPA with enough input power, a broadband linear driver amplifier was employed to amplify the test signal.

TABLE III
PERFORMANCE OF THE PROPOSED DPA WITH A 10-CARRIER 200 MHZ
MODULATED SIGNAL WITH 7.7 DB PAPR

| Center Freq (GHz)	Ave. Pout (dBm)	Ave. DE/PAE (%)	ACPR w/o DPD (dBc)	ACPR w/ DPD (dBc)	NMSE w/o DPD (dB)	NMSE w/ DPD (dB)
2.5	33.3	46.0/40.8	-17.3/ -19.0	-51.5/ -52.3	-14.0	-43.4
3.5	33.0	35.7/29.3	-21.0/ -22.8	-50.7/ -51.1	-20.6	-43.1
4.5	33.0	33.0/27.7	-29.6/ -24.3	-51.5/ -51.2	-19.0	-41.2

A. Measurement Results with CW Signal Excitation

The fabricated DPA was firstly tested using single tone CW signal to validate the Doherty operation. The measured drain efficiency and gains of the fabricated DPA with respect to output power at different bands are shown in Fig. 22(a) for Mode I, and Fig. 22(b) for Mode II, where we can see that Doherty operations are achieved in both two modes. There are some drops in back off efficiency at the higher operation band in Mode II. This might be caused by the performance degradation of the transistor in the high frequencies. The over-driven condition in Mode II also causes efficiency degradation.

To better present the wideband characteristics of the proposed DPA, performance at saturation and back-off was measured from 2.2 to 4.8 GHz with a frequency step of 0.1 GHz. Fig. 23 shows the simulated and measured small signal gain of the proposed DPA versus frequency. The simulated and measured output power and drain efficiency at saturation and back-off are presented along with frequency in Fig. 24. From Fig. 23 and 24, we can see that the measured performance is in good agreement with the simulation results with a small frequency offset. In Mode I, the DPA achieves operation bandwidth of 2.8-4.1 GHz with small signal gain of 8.5-9.6 dB and maximum output power of 40.4-41.0 dBm. In the Mode I frequency band, saturated drain efficiency of 52.0-68.0% is obtained. Meanwhile, at 6 dB output power back-off region, 42.0-49.7% drain efficiency is achieved. In Mode II, the PA operates as a dual-band DPA with two different frequency bands of 2.2 to 2.7 GHz and 4.2 to 4.8 GHz. Maximum output power of 39.2 to 41.0 dBm is achieved with small signal gain from 7.5 to 11.7 dB in these two bands. In Mode II frequency bands, saturated drain efficiency of 50.0-72.0% is obtained. Meanwhile, at 6 dB output power back-off region, 35.0-48.0% drain efficiency is achieved. It appears that the agreement between the measurements and simulations is not very good at some operation frequencies. This might be caused by the deviation of the fabrication and the inaccuracy of the transistor model especially for the Class-C operation.

B. Measurement Results with Modulated Signal Excitation

To verify the capability of the proposed DPA under modulated signal stimulation, targeting 5G wideband applications, a 10-carrier 200 MHz OFDM signal with 7.7 dB PAPR was employed to test the fabricated DPA. Digital pre-distortion (DPD)
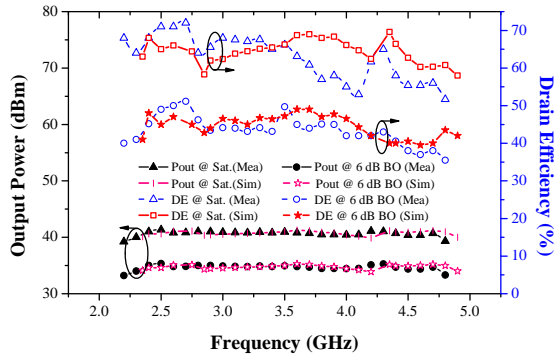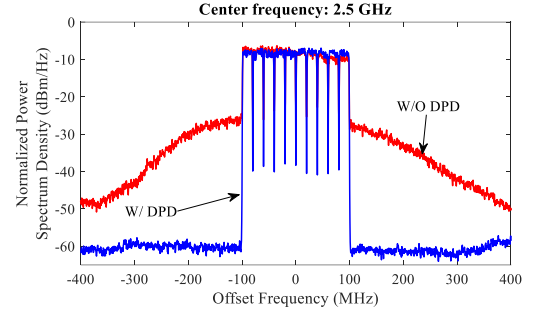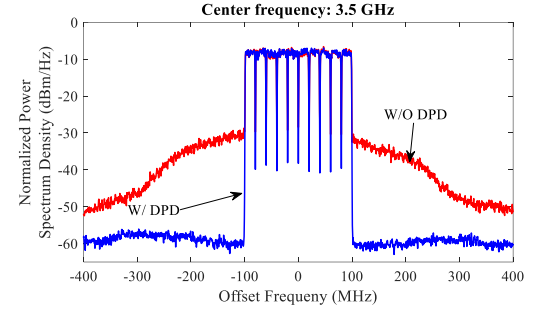
(a)

(b)

Fig. 23. Simulated and measured small signal gain of the fabricated DPA at different frequencies
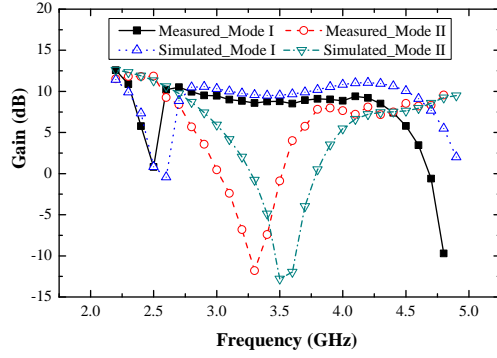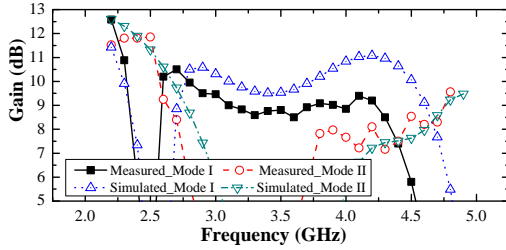
Fig. 24. Simulated (S) and measured (M) drain efficiency and output power of the fabricated DPA at different frequencies

(a)

(b)

(c)

Fig. 25. Output spectrum of the proposed DPA with and without DPD at (a) 2.5 GHz (b) 3.5 GHz (c) 4.5 GHz

was performed in the measurement to check if the proposed DPA is linearizable with wideband modulated signals. A non-parametric iterative learning control based DPD method [28] was adopted, which iteratively adjusts the predistorted signal to achieve an ideal linear response at PA output.
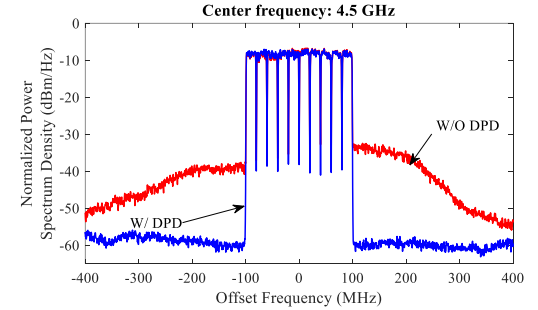
The fabricated DPA was measured at the designed two modes, centring at 3.5 GHz for Mode I and 2.5/4.5 GHz for Mode II. Fig. 25 shows the output spectra of the proposed DPA at these measured frequencies with and without DPD. Further details of the performance under modulated signal excitation are summarized in Table III. From the results, we can see that, excited with very wide modulated signals, e.g., 200 MHz OFDM signals, the PA is effectively linearizable while maintaining high efficiency after DPD. The proposed DPA achieves average efficiency of 46.0%, 35.7%, 33.0% with around 33 dBm average output power (7.3 to 8 dB back-

off) at 2.5, 3.5 and 4.5 GHz, respectively. The AM/AM and AM/PM characteristic of the proposed DPA with and without DPD at 3.5 GHz is also given here to present more feature under modulated signal stimulation, as shown in Fig. 26. As the same as that in CW test, the average efficiencies at higher frequency bands are lower, which is mainly caused by the device performance degradation at higher frequencies and over-driving operation in Mode II. Although the linearity performance of the fabricated DPA varies in different working bands, it can be well compensated by DPD. The adjacent channel power ratio (ACPR) can be improved to be better than -50 dBc after DPD at all these frequency bands.

C. Performance Comparison

A performance comparison between the proposed DPA and some recently reported broadband PAs with high back-off efficiency is summarized in Table IV. η_{sat} and η_{6dB} represent the drain efficiency at saturation and back-off, respectively. It can be seen that the proposed DPA exhibits excellent wideband
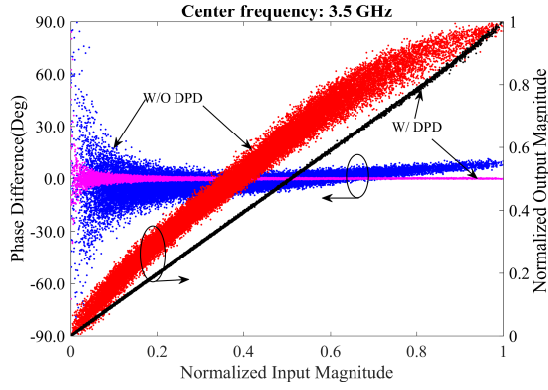
Fig. 26. Measured AM/AM and AM/PM curves of the proposed DPA at 3.5 GHz

TABLE IV
PERFORMANCE COMPARISON

Ref	Freq (GHz)	Pout (dBm)	Gain (dB)	η_{sat} (%)	η_{6dB} (%)
[7]	1.7-2.6	44.6-46.3	10.2-11.6	57-66	47-57
[10]	1.7-2.8	44-44.5	13.2-15.7	57-71	50-55
[11]	1.65-2.75	44.5-46.3	9.3-11.7	60-77	52-66
[16]	1.8-3.8	42-44	7.5-11	46-70	33-49
[17]	1.8-3.8	44.3-46.5	7.6-10.8	42-62	41-51**
[29]	3.0-3.6	43-44	8-11	55-66	38-56
[30]	4.7-5.3	39.0-39.5	7-7.5	52-67	29.7-33.1*
[31]	1.5-3.8	42.3-43.4	8-11	42-63	33-55
[32]	2.2-3.7	43-44.6	11	55-69	45-53
This Work	**2.2-4.8**	**39.2-41.0**	**7.5-11.7**	**50-72**	**35.0-49.7**

* 8 dB back-off efficiency, ** 9 dB back-off efficiency

operation and achieves comparable performance with other PAs by employing the dual-mode architecture.

It is worth mentioning that, the proposed idea is completely new and it is very different from what are used in conventional Doherty design. Although some trade-offs between two modes need be considered in the matching network design, the bandwidth of the proposed DPA is almost doubled by using the reciprocal gate biases configuration, without increasing much the complexity of the matching circuits or the design procedures. The practical operation of the PA is also very simple. Switching from one mode to the other, only swapping the supply voltages of the gate biases is required. It provides a simple alternative solution to the usual complex designs and it can be attractive for sub-6 GHz 5G applications where a large range of operation bandwidths are required.

Furthermore, the fabricated PA is for proof of concept only and its performance can be improved with further optimization. The device itself is also not our main concern. The main contribution of this paper is to present the new architecture and the related design methodology. The proposed approach is not constrained by the device used. The same configuration/architecture can be applied to any Doherty designs.

Although the performance and complexity may be different by using different devices, the proposed idea will still work in the same way.

V. CONCLUSION

A new configuration of DPA for extending its bandwidth is presented in this paper. Reciprocal gate biases are used to switch the DPA between two modes at different frequency bands. Consequently, the proposed structure can maintain Doherty operation with high back-off efficiency across a wide range of frequency bands. With broadband load modulation and post-matching networks, the designed DPA achieves 6 dB back-off efficiency of 35.0-49.7% from 2.2 to 4.8 GHz. The proposed DPA can cover various 5G and LTE frequency bands and thus it provides a promising solution for 5G in wideband operations.

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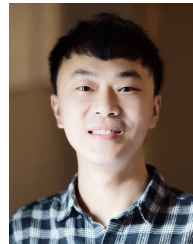
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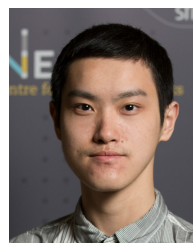
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