

A Broadband High-Efficiency Doherty Power Amplifier with Integrated Compensating Reactance

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Abstract — This paper presents a high-efficiency Gallium Nitride (GaN) Doherty power amplifier (DPA) using an integrated compensating reactance for broadband operation. With an additional quarter-wavelength transmission line integrated in the peaking amplifier output, a compensating reactance is generated to compensate the load impedance of the carrier amplifier in the low-power region and thus enhance the back-off efficiency over a wide frequency range without affecting the Doherty load modulation at saturation. For this purpose, a peaking output matching network (OMN) is employed to convert the output impedance of the peaking device to quasi short-circuit when it is off and achieve proper impedance matching when it is on. A two-point matching technique using the transmission (*ABCD*) matrix is employed to design such desired OMN. Measurement results show that the DPA has a 6 dB back-off efficiency of 50%–55% and saturated efficiency of 57%–71% over the frequency band of 1.7–2.8 GHz (49% fractional bandwidth). When driven by a 20 MHz Long Term Evolution (LTE) modulated signal at 6.5 dB back-off power, the DPA can achieve an average efficiency of more than 50% and with high linearity after linearization over the design frequency band.

Index Terms—Broadband, digital linearization, Doherty, high efficiency, integrated compensating reactance, power amplifiers.

I. INTRODUCTION

THE ever increasing demand for high transmission data rate and low power consumption imposes significant challenges in radio frequency (RF) power amplifier (PA) design for future mobile communication systems, in terms of bandwidth, average efficiency and linearity. When driven by modulated signals with high peak-to-average power ratios (PAPRs), Doherty power amplifier (DPA) has attracted significant attentions because of its simplicity and significant enhancement of the average efficiency at back-off operation [1]–[6]. However, the quarter-wavelength impedance transformer after the carrier amplifier, that is used to achieve proper load modulation, limits the operation bandwidth of conventional DPAs [7]. This is because, due to the dispersion effect of the impedance transformer, the effective load impedance seen by the carrier amplifier in low-power region can be the anticipated value of $2Z_0$ only at the center frequency

f_0 , and it will be reduced as the operation frequency deviates from f_0 , which leads to degradation of the back-off efficiency and hence limits the operation bandwidth of the DPA.

To overcome this problem, various design approaches have been proposed to extend the bandwidth of DPA [7]–[21]. A transformer-less load-modulated architecture was proposed in [8], which extended the bandwidth by eliminating the use of output impedance transformer and offset lines. The DPA topology based on branch-line couplers has been exploited to achieve up to 36.3% fractional bandwidth [15]. To maintain back-off impedance of the carrier amplifier, a novel output combiner employing a resonance LC tank was introduced in [17]. Recently, a band-pass auxiliary transformer was employed to design wideband DPA, achieving 40% bandwidth and high back-off efficiency [19]. Moreover, a closed-form design technique for ultra-wideband DPAs has also been proposed for bare-die device design, demonstrating greater than 83% fractional bandwidth with some degradations of the back-off efficiency [21]. And yet, to effectively amplify future wideband or multi-band modulated signals, it is desirable to further extend the operation bandwidth of the DPAs and achieve high back-off efficiency over the entire frequency band.

In this paper, after analyzing the influence of the reactance in the common load on the carrier back-off load impedance in wideband operation, a broadband DPA topology with an integrated compensating reactance is proposed. By using a quarter-wavelength transmission line in the output of the peaking amplifier, an equivalent quasi-short circuit stub can be generated to compensate the impedance variation of the carrier amplifier in the low power operation when the peaking amplifier is off. Because the quarter-wavelength transmission line has a characteristic impedance of Z_0 , it does not affect the Doherty load modulation in the high power operation when the peaking amplifier is on. To satisfy the impedance matching requirements for the peaking and carrier output matching networks (OMNs) simultaneously in the low-power region and at saturation, a two-point matching OMN design method by using *ABCD* matrix is proposed and a systematic design procedure is given. To validate the proposed approach, a 1.7–2.8 GHz GaN DPA is designed, implemented and measured. Experimental results show that high back-off efficiency can be maintained over the entire operation bandwidth by employing the proposed design, which allows the DPA to be operated with a very wide bandwidth in future

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applications.

This paper is organized as follows. The proposed DPA topology for back-off efficiency enhancement over a wide frequency band is analyzed and derived in Section II. Section III introduces the design approach for the proposed DPA. The implementation and measurement results are given in Section IV. The linearity improvement of the DPA when excited with a Long Term Evolution (LTE) modulated signal is also demonstrated. Conclusions are given in Section V.

II. NETWORK ANALYSIS AND BANDWIDTH EXTENSION

The DPA is usually composed of two amplifiers, namely the carrier and peaking amplifiers, and a combining network, as shown in Fig. 1. The combining network usually includes a common load and an impedance transformer that is often implemented by using a $\lambda_0/4$ transmission line to achieve anticipated load modulation [22]. For efficient amplification of modulated signals over a wide frequency range, ideally the effective load impedance of the carrier amplifier in the low-power region should be maintained close to the desired impedance, i.e., $2Z_0$, but in reality, it is not the case. In this section, we first analyze the frequency response of the DPA and then introduce a new matching network topology for bandwidth extension for DPA.

A. Analysis of the Combining Network

As shown in Fig. 1, if each transistor is considered to be an ideal current source, the effective load impedances of the two amplifiers can be expressed in terms of the $ABCD$ parameters of the impedance transformer, the common load Z_L , the current ratio between the peaking and carrier amplifiers δ , as well as the phase of the peaking amplifier φ . The detailed derivation is given in Appendix. In the low-power region (up to 6 dB back-off point), the effective load impedances of the carrier and peaking amplifiers are given by

$$Z_{C_low} = \frac{Z_L A + B}{Z_L C + D} \quad (1)$$

$$Z_{P_low} = \infty \quad (2)$$

where $ABCD$ is the transmission matrix of the impedance transformer at a given frequency. At saturation, the modulated load impedance seen by the two amplifiers can be expressed as follows:

$$Z_{C_sat} = \frac{\delta e^{j\varphi} Z_L (AD - BC) + Z_L A + B}{Z_L C + D} \quad (3)$$

$$Z_{P_sat} = \frac{e^{-j\varphi} Z_L + \delta Z_L D}{\delta Z_L C + \delta D} \quad (4)$$

where $\delta = |I_{P_sat}|/|I_{C_sat}|$ and φ is the phase of the output current of the peaking amplifier.

To demonstrate the frequency response of the network and simplify the analysis, a conventional Doherty structure using a $\lambda_0/4$ impedance transformer with a characteristic impedance of Z_T is used. The $ABCD$ matrix of the $\lambda_0/4$ impedance transformer can be written as

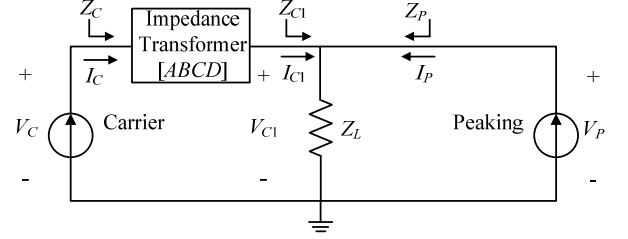


Fig. 1. The equivalent-circuit diagram of a DPA with the carrier and peaking amplifiers represented by current sources.

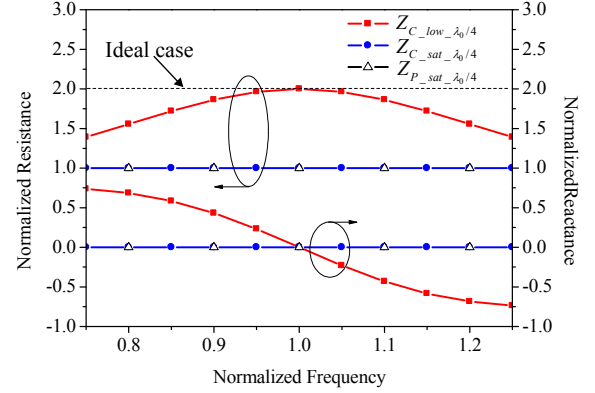


Fig. 2. Normalized load impedances at low-power region and saturation for a conventional DPA over normalized frequency band of 0.75 to 1.25.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\lambda_0/4} = \begin{bmatrix} \cos \theta & jZ_T \sin \theta \\ j \frac{\sin \theta}{Z_T} & \cos \theta \end{bmatrix} \quad (5)$$

where θ is the phase delay of the $\lambda_0/4$ impedance transformer at a given frequency, i.e., $\theta = \frac{\pi}{2} \cdot \frac{f}{f_0}$.

By replacing (5) in (1), (3) and (4), for a conventional DPA with a $\lambda_0/4$ impedance transformer, the effective carrier load impedance in low-power region and the load impedances of both two amplifiers at saturation can then be expressed by

$$Z_{C_low_lambda_0/4} = Z_T \frac{Z_L + jZ_T \tan \theta}{Z_T + jZ_L \tan \theta} \quad (6)$$

$$Z_{P_low_lambda_0/4} = \infty \quad (7)$$

$$Z_{C_sat_lambda_0/4} = \frac{\delta e^{j\varphi} Z_T Z_L + Z_T Z_L \cos \theta + jZ_T^2 \sin \theta}{Z_T \cos \theta + jZ_L \sin \theta} \quad (8)$$

$$Z_{P_sat_lambda_0/4} = \frac{Z_T Z_L e^{-j\varphi} + \delta Z_T Z_L \cos \theta}{\delta Z_T \cos \theta + j\delta Z_L \sin \theta} \quad (9)$$

In a general case, Z_L is $0.5Z_0$ and Z_T equals Z_0 , where Z_0 represents the optimum load impedance for both amplifiers and it usually is 50Ω in most DPA designs. Therefore, assuming both two amplifiers can achieve output current with the same amplitude over the whole frequency band (i.e., $\delta=1$) and the phase of the peaking amplifier φ equals $-\theta$, the normalized load impedances Z_{C_low} , Z_{C_sat} and Z_{P_sat} can be calculated according to (6), (8) and (9), and the results are illustrated in Fig. 2.

From the results, we can see that the effective resistance of the carrier load impedance in the low-power region, i.e.,

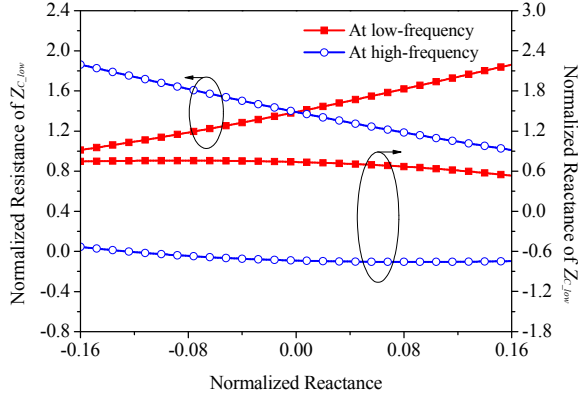


Fig. 3. Normalized load impedance $Z_{C,low}$ at low and high frequencies versus the reactance of the common load (normalized to Z_0).

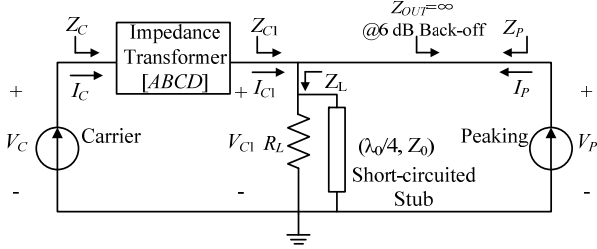


Fig. 4. The DPA with compensating reactance implemented by using a shunted short-circuited stub.

$\text{Re}\{Z_{C,low}\}$, has a maximum value of $2Z_0$ only at the center frequency f_0 and it decreases as the frequency deviates from f_0 . This leads to efficiency degradation when the DPA is operated over a wide bandwidth, as discussed in [7]. Moreover, the back-off efficiency will further degrade as the frequency deviation increases. To extend the operation frequency band of the DPA, the effective resistance of the load impedance of the carrier amplifier in the low-power region should be enlarged, at both low and high frequencies.

B. Proposed Network Compensation for Bandwidth Extension

The influence of complex impedance seen at the combining point on the back-off efficiency of the DPA at a specific frequency has been discussed in [23]. To analyze the effect of the reactance of the common load over a wide frequency range, assuming the common load $Z_L = R_L + jX_L$ and $R_L = 0.5Z_0$, the normalized carrier load impedance $Z_{C,low}$ at low and high frequencies ($0.75f_0$ and $1.25f_0$) as a function of the reactance of the common load (X_L) can be calculated according to (6) and the result is shown in Fig. 3. It can be observed that, at low frequency the effective resistance of $Z_{C,low}$ can be increased by increasing the reactance of the common load, while at high frequency the resistance can be enlarged by decreasing the reactance. This can be achieved by using suitable compensating reactance (CR) at the common load.

The resonance LC tank introduced in [17] is one of the possible solutions for reactance compensation, but the maximum operation frequency of this LC tank is limited. To increase the operation frequency, a $\lambda_0/4$ short-circuited stub with a characteristic impedance of Z_0 can be used, as shown in

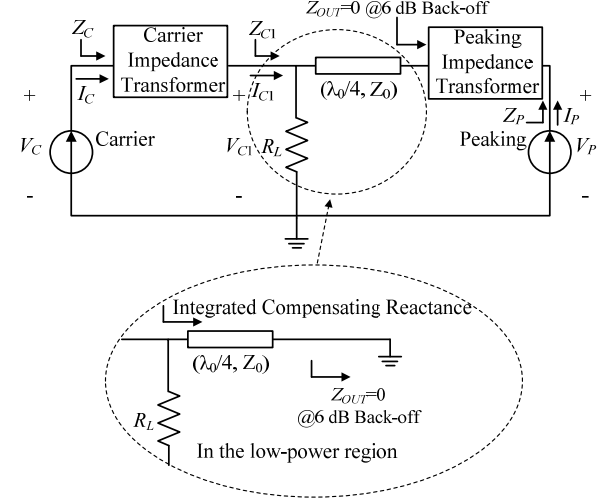


Fig. 5. The proposed DPA with an integrated compensating reactance in the output of the peaking amplifier.

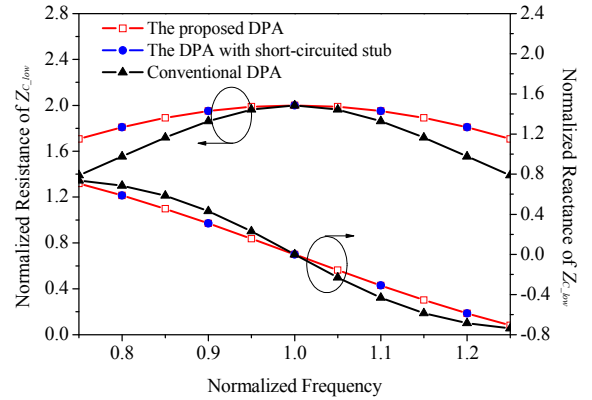


Fig. 6. Simulated carrier load impedance of a conventional DPA, the DPA with short-circuited stub and the proposed DPA in the low-power region.

Fig. 4. However, in Doherty operation, the shunted LC tank or the short-circuited stub will affect the load impedances of both the carrier and peaking amplifiers at saturation that can degrade the DPA performance.

In this paper, to maintain proper load modulation while conducting reactance compensation, an integrated reactance compensation approach is proposed. As shown in Fig. 5, instead of using a short-circuited stub, a $\lambda_0/4$ transmission line with a characteristic impedance of Z_0 is connected between the output of the peaking amplifier and the combining point firstly. The peaking impedance transformer is then designed to achieve short-circuit in the low-power region and a desired optimum load impedance, e.g., Z_0 , at saturation, respectively. In this configuration, when the peaking amplifier is off, i.e., in the low power region, the $\lambda_0/4$ compensating transmission line is acted as a short-circuited stub that can be used to compensate the carrier load impedance and thus enhance the back-off efficiency over a wide bandwidth. When the peaking amplifier is on, i.e., at the saturation region, the $\lambda_0/4$ line is simply acted as a delay line that does not affect the load modulation of the DPA since its characteristic impedance is Z_0 . This design overcomes the problem of using shunted reactive loads

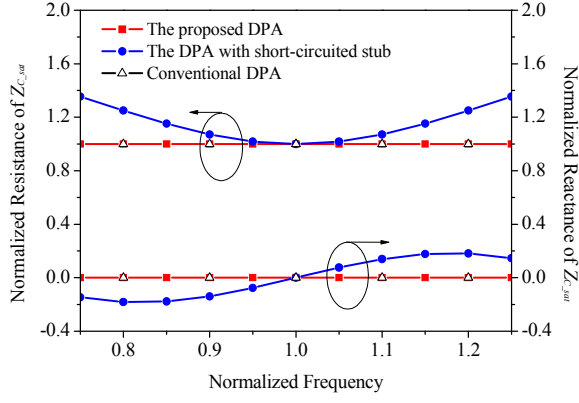


Fig. 7. Simulated carrier load impedance of a conventional DPA, the DPA with short-circuited stub and the proposed DPA at saturation.

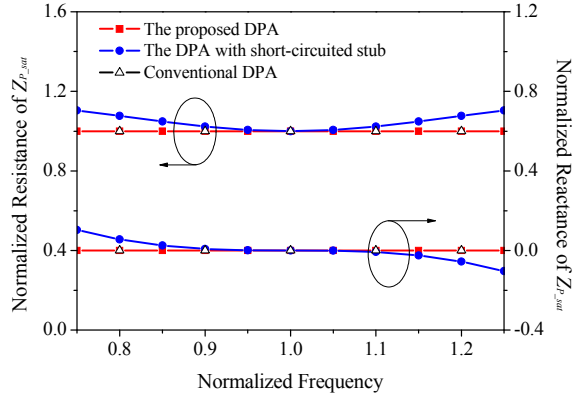


Fig. 8. Simulated peaking load impedance of a conventional DPA, the DPA with short-circuited stub and the proposed DPA at saturation.

mentioned earlier.

To verify the performance of the proposed DPA topology, further analyses can be conducted as follows. To facilitate derivation, a $\lambda_0/4$ transformer is used as the carrier impedance transformer. The normalized load impedances at low-power region and at saturated power at various frequencies can be calculated by using equations (6)-(9) for the two DPAs shown in Fig. 4 and Fig. 5, respectively. The results are shown in Fig. 6, 7 and 8. For reference, the result of the case of a conventional DPA is also depicted. It can be seen that, in the low-power region, the effective resistance of Z_{C_low} of both DPAs is enlarged at low and high frequencies because of the reactive load compensation, compared to that of the conventional DPA. These results show that an efficiency enhancement can be expected in wideband operation.

Regarding the results at saturation, for the DPA with a shunted short-circuited stub, the shunted $\lambda_0/4$ stub will affect the modulated load impedances of both amplifiers, as shown in Fig. 7 and 8, leading to improper load modulation and performance degradation at high power operation. On the contrary, for the proposed DPA, because the $\lambda_0/4$ line is integrated into the output of the peaking amplifier and the peaking impedance transformer can achieve the optimum load impedance at saturation as the same as that in the conventional design, the effect on the load impedances can be effectively

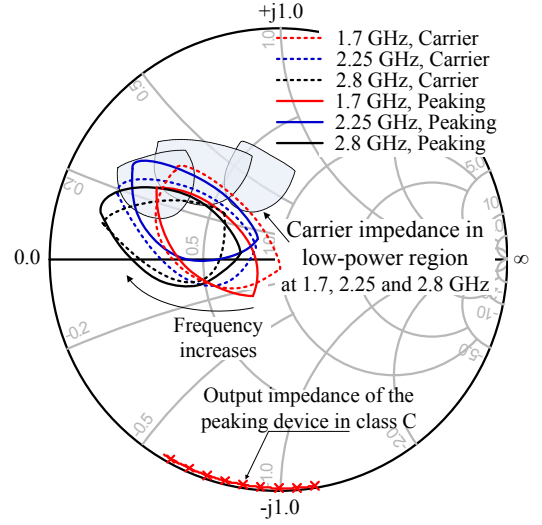


Fig. 9. Simulated output power and efficiency contours for 1.7, 2.25 and 2.8 GHz. For carrier device in class AB: >41 dBm output power and $>60\%$ efficiency, and for peaking device in class C: >41 dBm output power and $>55\%$ efficiency.

reduced and then proper load modulation can be achieved.

III. DESIGN AND SIMULATION

In this section, based on the idea of the integrated reactance compensation, a systematic design procedure is presented for the proposed DPA to obtain enhanced back-off efficiency over a wide frequency band and simultaneously achieve the desired load modulation at saturation.

A. OMN Design

In order to achieve the desired behavior in the proposed design, the OMNs of the carrier and peaking amplifiers must be properly designed. To describe the design procedure, we use Cree CGH40010F GaN HEMT device as an example. Firstly, the optimal load impedances at the device package plane of both amplifiers were obtained by using load-pull simulations. The Cree GaN HEMT circuit model was used in the simulations with bias conditions of a class AB mode and a predefined class C mode. To enlarge the current ratio (δ) and improve load modulation, the drain voltage was set to be 26 and 30 V for the carrier and peaking devices, respectively.

For the frequency band of 1.7–2.8 GHz, the results shown in Fig. 9 were generated by sweeping the fundamental load impedances while setting second and third harmonic terminations to predefined loads. For the carrier device, the inside region of the contour represents the area on the Smith chart for greater than 41 dBm output power and 60% efficiency. Meanwhile, the impedance region for the carrier amplifier to achieve high efficiency, greater than 70%, at back-off power is also given for the frequencies of 1.7, 2.25 and 2.8 GHz. To achieve similar output power with the carrier device for proper load modulation, the criterion of higher than 41 dBm output power and 55% efficiency was chosen for the peaking device, as illustrated in Fig. 9. In addition, the output impedance of the peaking device in class C operation is also depicted, which can

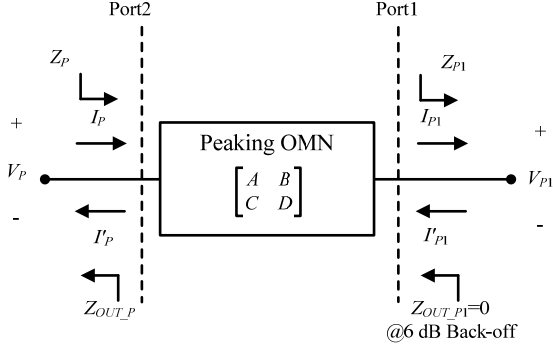


Fig. 10. The peaking OMN denoted by $ABCD$ matrix.

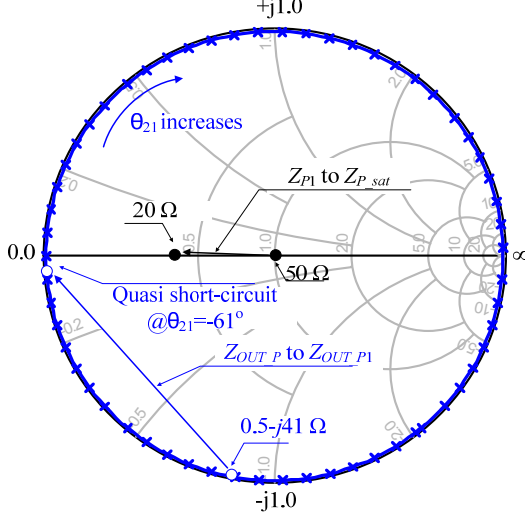


Fig. 11. Graphical illustration of the two-point matching technique for the peaking OMN design at the frequency of 2.25 GHz.

be used to design the peaking OMN in the proposed DPA.

As mentioned above, the peaking OMN should achieve quasi short-circuit in the low-power region and the desired optimum load impedance at saturation. To design such OMN, a two-point matching technique, deduced by using $ABCD$ matrix, is proposed, as discussed in detail below.

The peaking OMN is shown in Fig. 10. If the OMN is considered as a lossless reciprocal two-port network, the S parameter matrix of such network can be expressed as [8]

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} -S_{22}^* e^{j2\theta_{21}} & \sqrt{1-|S_{22}|^2} e^{j\theta_{21}} \\ \sqrt{1-|S_{22}|^2} e^{j\theta_{21}} & S_{22} \end{bmatrix} \quad (10)$$

where θ_{21} is the phase of S_{21} .

According to the network parameter conversion, the $ABCD$ parameters of the OMN can be written as

$$A = \frac{(1 - S_{22}^* e^{j2\theta_{21}})(1 - S_{22}) + (1 - |S_{22}|^2) e^{j2\theta_{21}}}{2\sqrt{1-|S_{22}|^2} e^{j\theta_{21}}} \quad (11)$$

$$B = Z_0 \frac{(1 - S_{22}^* e^{j2\theta_{21}})(1 + S_{22}) - (1 - |S_{22}|^2) e^{j2\theta_{21}}}{2\sqrt{1-|S_{22}|^2} e^{j\theta_{21}}} \quad (12)$$

TABLE I

DESIGN PARAMETERS OF THE PEAKING OMN					
Frequency (GHz)	Z_P	Z_{P1}	Z_{OUT_P}	Z_{OUT_P1}	θ_{21}
1.7	$28-j8 \Omega$	50Ω	$0.5-j57 \Omega$	$0.1-j12 \Omega$	-47°
2.25	20Ω	50Ω	$0.5-j41 \Omega$	Quasi short	-61°
2.8	$16+j8 \Omega$	50Ω	$0.5-j30 \Omega$	$0.5+j12 \Omega$	-75°

$$C = \frac{1}{Z_0} \frac{(1 + S_{22}^* e^{j2\theta_{21}})(1 - S_{22}) - (1 - |S_{22}|^2) e^{j2\theta_{21}}}{2\sqrt{1-|S_{22}|^2} e^{j\theta_{21}}} \quad (13)$$

$$D = \frac{(1 + S_{22}^* e^{j2\theta_{21}})(1 + S_{22}) + (1 - |S_{22}|^2) e^{j2\theta_{21}}}{2\sqrt{1-|S_{22}|^2} e^{j\theta_{21}}} \quad (14)$$

where Z_0 is the termination impedance (usually is 50Ω).

A set of linear equations of the voltages and currents at both side of the peaking OMN can then be expressed in terms of the $ABCD$ parameters as

$$\begin{bmatrix} V_{P1} \\ I'_{P1} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_P \\ -I_P \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_P \\ I'_P \end{bmatrix} \quad (15)$$

In the low-power region, the peaking device is in off-state and its output impedance is assumed to be Z_{OUT_P} . Since $V_P = I'_P Z_{OUT_P}$, the output impedances of the peaking amplifier becomes

$$Z_{OUT_P1} = \frac{V_{P1}}{I'_{P1}} = \frac{Z_{OUT_P} A + B}{Z_{OUT_P} C + D} \quad (16)$$

At saturation, the following relationship can be obtained:

$$Z_{P1}^* = \frac{Z_P^* A + B}{Z_P^* C + D} \quad (17)$$

In the low-power region, the peaking OMN should transform the impedance Z_{OUT_P} to the desired quasi short-circuited impedance Z_{OUT_P1} . On the other hand, the impedance Z_{P1} should also be transformed to the optimum load impedance Z_P when the amplifier is in saturation. When those four impedances have been determined, the design parameters of the OMN, i.e., S_{22} and θ_{21} , can be obtained according to (10)-(14), (16) and (17). An optimized OMN that can achieve two-point matching can then be designed accordingly.

Taking the peaking OMN for example, assuming the center frequency is 2.25 GHz, the optimum load impedance $Z_P = 20 \Omega$ can be obtained by using load-pull results in Fig. 9, while Z_{P1} is chosen to be 50Ω . The output impedance of the peaking device in class C operation is found to be $Z_{OUT_P} = 0.5-j41 \Omega$. Considering the phase of S_{21} (θ_{21}) as a degree of freedom, the parameter S_{22} can then be calculated by using (17) and a set of output impedances Z_{OUT_P1} can be plotted in the Smith chart, as shown in Fig. 11. When Z_{OUT_P1} is close to be quasi short-circuit, a series of $\theta_{21} = -61^\circ - n \times 180^\circ$ ($n=0, 1, 2, \dots$) can be obtained according to the periodicity of the exponential function, but only θ_{21} with the minimum value should be chosen in order to minimize the phase delay dispersion over the whole frequency band for wideband operation. By using a similar

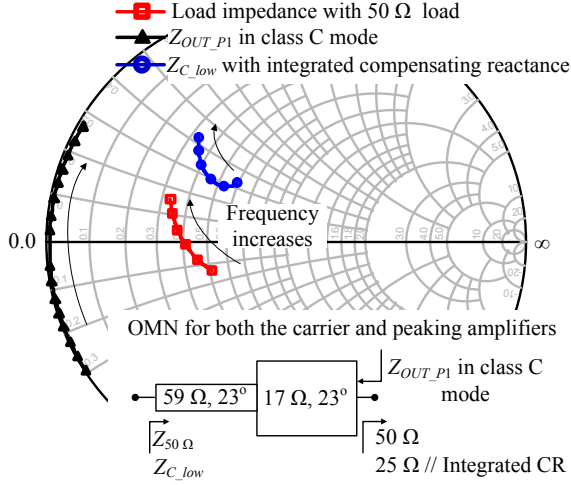


Fig. 12. Designed matching network for both amplifiers and the impedances on the Smith chart for the frequency band of 1.7–2.8 GHz.

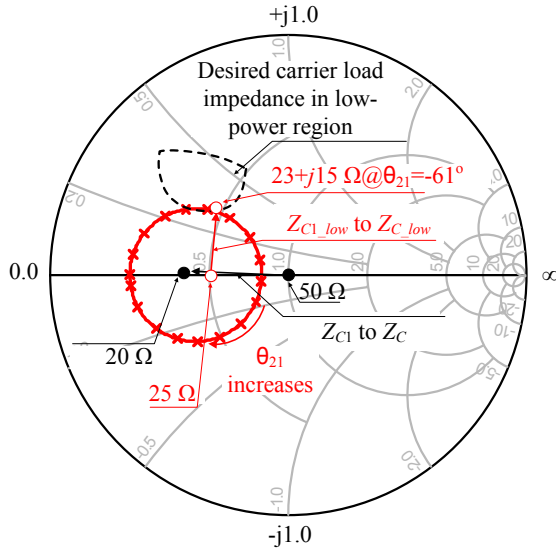


Fig. 13. Graphical illustration of the two-point matching technique for the carrier OMN design at the frequency of 2.25 GHz.

approach, the design parameters for the frequencies of 1.7 and 2.8 GHz can also be determined, as listed in Table I. Due to the frequency dispersion of the output impedance of the peaking device, it is difficult to achieve short-circuit over the whole frequency band. Low reactance value was used as the target of Z_{OUT_P1} for low and high frequencies.

Considering the obtained S parameters and θ_{21} , the OMN can then be designed by using network theory and tuned by optimization, as shown in Fig. 12. The load impedance at saturation power (with 50 Ω load) and the peaking output impedance in class C operation are also depicted. The results show that the OMN designed by using two-point matching technique can satisfy the requirement of the peaking amplifier.

Regarding the carrier amplifier, the carrier OMN should achieve the desired effective load impedance for high back-off efficiency in the low-power region and the optimum load impedance at saturation. For convenience, the same optimum

Frequency (GHz)	Z_C	Z_{C1}	Z_{C_low}	Z_{C1_low}	θ_{21}
1.7	$28-j8 \Omega$	50 Ω	$35+j17 \Omega$	$23+j8 \Omega$	-47°
2.25	20 Ω	50 Ω	$23+j15 \Omega$	25 Ω	-61°
2.8	$16+j8 \Omega$	50 Ω	$16+j21 \Omega$	$23-j8 \Omega$	-75°

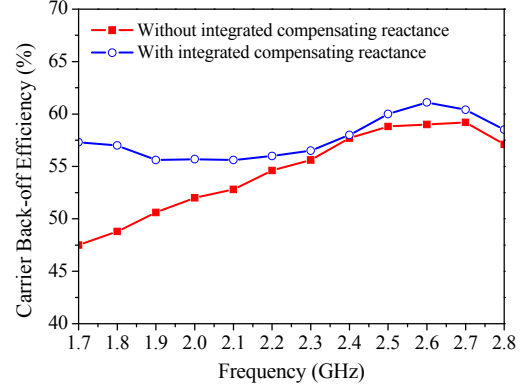


Fig. 14. The comparison of the back-off efficiency of the carrier amplifier (terminated with 25 Ω load) with and without integrated compensating reactance.

load impedance at saturation for 2.25 GHz (20 Ω) was chosen according to the inside region of the contours in Fig. 9. By using similar approach, the two-point matching for the carrier OMN design can also be achieved, as illustrated in Fig. 13. Considering the desired carrier back-off impedance region, the phase of S_{21} in the carrier OMN can be chosen to be -61° . After calculating the common load with the integrated compensating reactance, the design parameters of the carrier OMN for the frequencies of 1.7 and 2.8 GHz can be obtained, as shown in Table II. To alleviate the difference of the phase response between the carrier and peaking amplifiers over a wide frequency range, similar network topology, which can satisfy the requirements of both the two amplifiers mentioned above, was used to design the OMNs. The carrier load impedance in the low-power region with integrated compensating reactance is shown in Fig. 12. It is worth to mention that, in this design, the offset lines that usually are used in the conventional DPA are not needed in the proposed DPA.

B. IMN Design and System Simulation

After the OMNs are determined, the input matching networks (IMNs) can be designed by using the stepped-impedance matching network topology to cover the required bandwidth. To verify the efficiency and bandwidth enhancement of the proposed method, for the output power of about 38 dBm, the efficiencies of the carrier amplifier terminated with 25 Ω load, with and without the peaking amplifier connected to the combining point, were simulated and compared. In the simulation, the carrier amplifier was biased at $V_{GS} = -3$ V and $V_{DS} = 26$ V, while the peaking amplifier was in off-state with the bias condition of $V_{GS} = -5.6$ V and $V_{DS} = 30$ V.

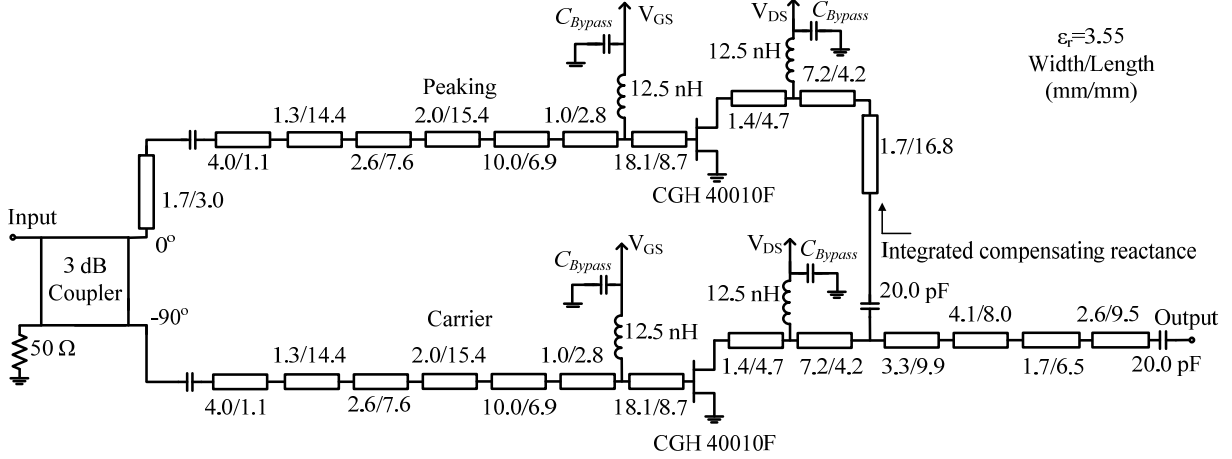


Fig. 15. The complete schematic of the proposed DPA.

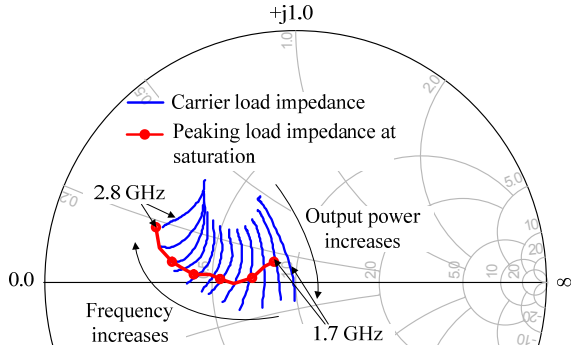


Fig. 16. Simulated load traces of the carrier device in the Doherty operation and the peaking device at saturation.

The results in Fig. 14 show that higher than 55% efficiency can be achieved over the whole frequency range with the proposed integrated compensating reactance generated by the peaking amplifier. Especially at the low-frequency, the efficiency is considerably higher compared to the conventional design without using compensating reactance.

The final circuit of the proposed DPA is shown in Fig. 15. To precisely convert 50 Ω to 25 Ω at the combining point over large frequency band, a four-order real-to-real matching network was used. Meanwhile, because the phase response of the carrier and peaking amplifiers are different over a wide frequency range, a 3 dB 90° hybrid coupler, instead of the Wilkinson power divider, is used as the input splitter to ensure suitable phase relationship between the output currents of the two amplifiers.

In Fig. 16, the simulated load impedance traces of the carrier device (in the Doherty region) and the peaking device (at saturation) are depicted. As discussed in Section II, using the integrated compensating reactance does not affect the Doherty load modulation. The load impedances of both carrier and peaking devices at saturation thus still satisfy the design criteria used in the load-pull simulations. More importantly, because of the integrated compensating reactance, the load impedances of the carrier amplifier at low output powers can match the desired load-pull results for the carrier amplifier and thus high

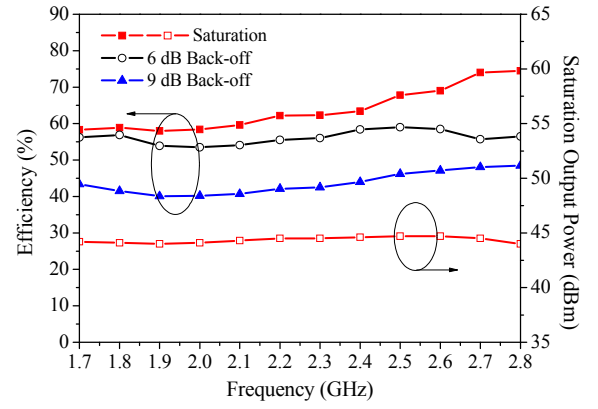


Fig. 17. Simulated efficiency and saturated output power of the proposed DPA at the frequency band of 1.7–2.8 GHz.

efficiency at back-off powers can be achieved.

Fig. 17 shows the simulated efficiency of the proposed DPA at different back-off powers versus frequency, as well as the saturated output power. With the saturated power around 44 dBm, the DPA can achieve the efficiency of higher than 54% and 40% at 6 and 9 dB back-off powers within the entire frequency band of 1.7–2.8 GHz.

IV. REALIZATION AND EXPERIMENTAL VERIFICATION

To validate the proposed method, a broadband DPA was fabricated by using Cree CGH40010F GaN HEMT and on a Taconic RF35 substrate with $\epsilon_r = 3.55$ and the thickness of 30 mil over the frequency range of 1.7–2.8 GHz, as shown in Fig.18. For design convenience, a 3 dB 90° hybrid coupler (Anaren X3C22E1-03S) was used as the input splitter. The carrier amplifier was biased in the class AB condition with 0.05 A quiescent current and $V_{DS} = 26$ V, while the peaking amplifier was biased in the class C mode to turn on at about 6 dB back off power and $V_{DS} = 30$ V.

A. Measurement Results with Continuous Wave Signals

Firstly, the DPA was measured under continuous wave (CW) signal stimulus from 1.7 to 2.8 GHz. Fig. 19 shows the measured efficiency and gain characteristics of the DPA as a function of output power under CW measurements. The

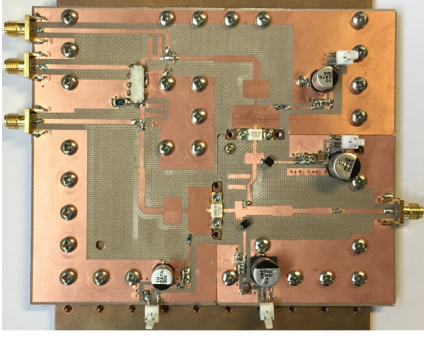


Fig. 18. Photograph of the fabricated DPA.

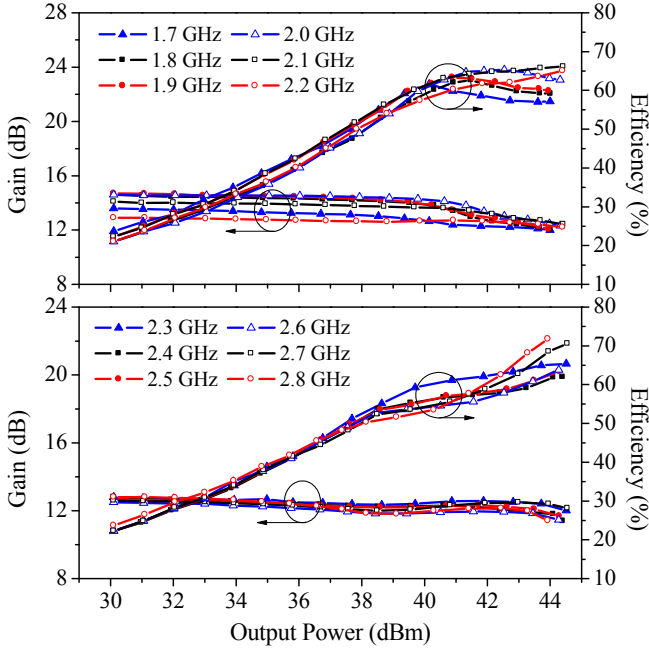


Fig. 19. Measured efficiency and gain of the DPA versus output power at different frequencies.

saturated power is greater than 44 dBm from 1.7 to 2.8 GHz with a peak of 44.5 dBm. The results show that the gain, output power and efficiency maintain consistent over the entire operation frequency band at back-off powers. Fig. 20 shows measured efficiency and gain at different back-off powers in the frequency band of 1.7–2.8 GHz (approximately 49% fractional bandwidth). For back-off operation, the efficiency is within 50%–55% and 37%–41% at 6 and 9 dB back-off power, while the maximum gain is about 14.5 dB with the gain fluctuation of less than 2.5 dB. Regarding the saturated operation, the efficiency is between 57%–71% with a gain of roughly 12 dB.

Comparison with reported wideband DPAs is outlined in Table III. For CW measurements, with good back-off efficiency and highly consistent saturated output power, the proposed DPA achieves wider operation bandwidth than most DPAs in Table III, except the DPA designed by using the bare-die device with slightly degraded 6 dB back-off efficiency [21].

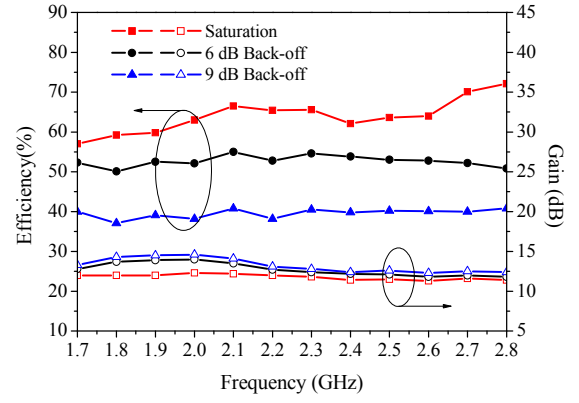


Fig. 20. Measured efficiency and gain of the DPA versus frequency at saturation, 6 dB and 9 dB back-off powers, respectively.

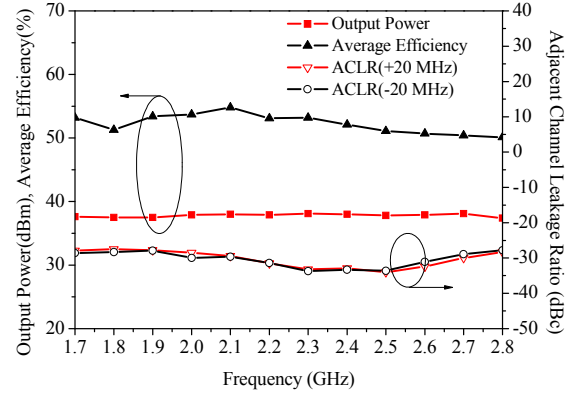


Fig. 21. Measured output powers, average efficiencies and ACLRs of the proposed DPA for modulated signal at 6.5 dB back-off power.

TABLE III
COMPARISON WITH REPORTED WIDEBAND DPAs

Reference	Frequency (GHz)	FBW (%)	Psat (dBm)	Efficiency@ Saturation (%)	Efficiency@ 6 dB Back-off (%)
[21] ²	1.05-2.55	83	40-42	45-83	35-58
[13] ²	1.5-2.4	46	~42	52-68	49-62
[19] ¹	1.6-2.4	40	42.7-43.3	72-77	55-63
[7] ¹	1.7-2.6	42	42.1-45.3	50-55	41-55
[18] ¹	1.8-2.2	20	41.8-42.3	69-73	58-67
[11] ¹	2.2-3.0	31	39.4-41.8	50-68	36-48
This work ¹	1.7-2.8	49	44-44.5	57-71	50-55

FBW: fractional bandwidth, Psat: Saturation output power

1 Packaged device

2 Bare-die device

B. Measurement Results with Modulated Signals

To evaluate the performance of the proposed DPA for modulated signal applications, a 20 MHz LTE signal with a PAPR of 6.5 dB was used to test the efficiency and linearity performances over the whole frequency band. As shown in Fig. 21, the proposed DPA can deliver an average efficiency of 50%–55% at 6.5 dB back-off power, while the adjacent channel leakage ratio (ACLR) is around –30 dBc for the most operational frequencies. To satisfy the linearity requirement of

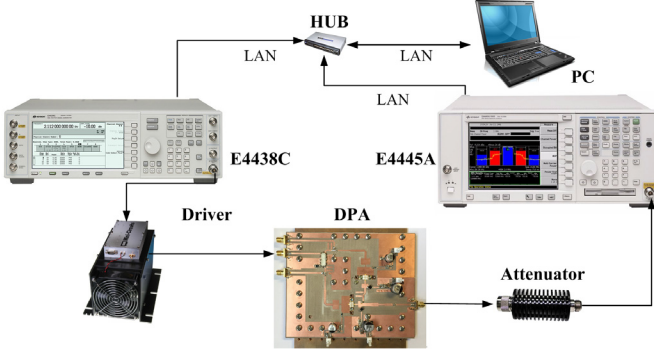


Fig. 22. The block diagram of the linearization test bench.

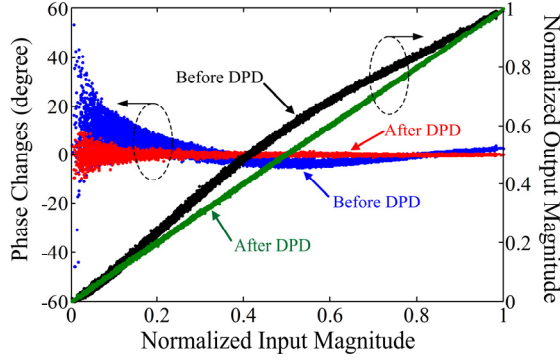


Fig. 23. AM/AM and AM/PM plots for 20 MHz LTE signal before and after DPD at 2.14 GHz.

common wireless systems (i.e. $\text{ACLR} < -45$ dBc), digital predistortion (DPD) technique has been widely used to improve the linearity of the DPAs when they are excited by wideband modulated signals [2], [4], [6], [12], [14]–[17], [21].

To validate the linearity improvement of the DPA, the DPD measurement was conducted at 1.96, 2.14, 2.355 and 2.655 GHz considering the frequency division duplex (FDD) LTE frequency band allocations. The block diagram of the experimental test bench is shown in Fig. 22. The baseband in-phase/quadrature (I/Q) signal was modulated and up-converted to RF signal in a vector signal generator (Keysight E4438C), and then amplified by the DPA. In the feedback loop, the output signal was down-converted and demodulated by a spectrum analyzer (Keysight E4445A) to baseband and then used for DPD inverse model extraction. The piecewise decomposition technique [24] together with the 2nd order dynamic derivation reduction (DDR) Volterra model [25] was employed in the DPD modeling. The magnitude threshold was set as {0.4 0.7} for the normalized data, while the nonlinearity order was selected as {7, 7, 7} and the memory length was set to {3, 3, 3}. After the inverse model was obtained, the pre-distorted signal can be generated. It then can be modulated and up-converted by the vector signal generator again as the input signal of the DPA for DPD linearization.

To evaluate the linearization performance, taking the frequency of 2.14 GHz for example, the time-domain AM/AM and AM/PM characterizations at the average power of 38 dBm are depicted in Fig. 23, where it can be seen that both the static nonlinearities and memory effects can be effectively removed

TABLE IV
COMPARISONS OF THE DPD PERFORMANCES AT DIFFERENT FREQUENCIES

Frequency (GHz)	1.96	2.14	2.355	2.655	
Output Power (dBm)	37.9	38	38	38.1	
Average Efficiency (%)	52.1	53.5	51.7	50.8	
ACLR (dBc)	Before DPD	-28.8/-28.5	-29.6/-29.8	-33.3/-32.9	-31.5/-32.8
	After DPD	-47.8/-48.3	-48.9/-48.9	-50.1/-50.3	-49/49.7

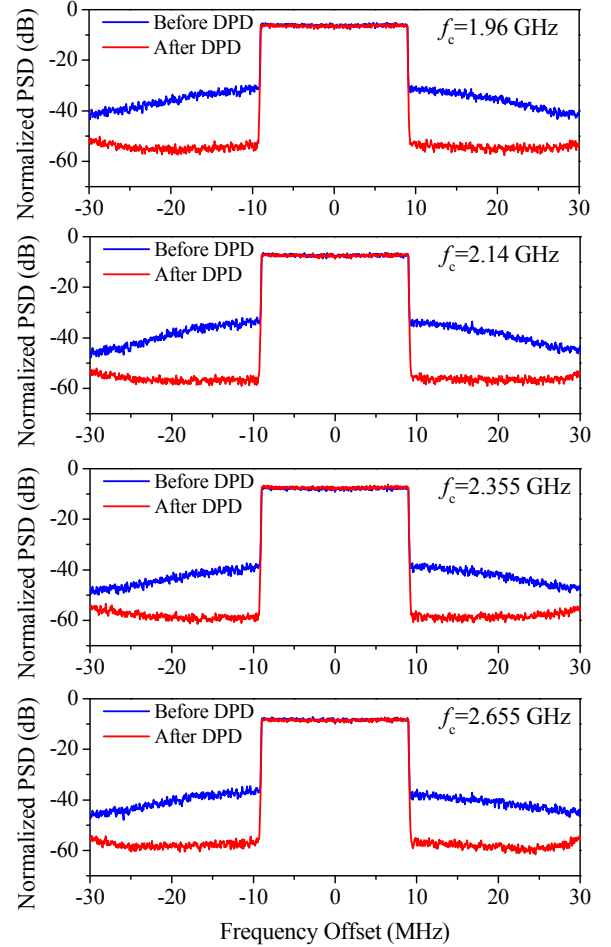


Fig. 24. Measured signal spectra before and after linearization for 20 MHz LTE modulated signal at 1.96, 2.14, 2.355 and 2.655 GHz.

after DPD linearization. The linearization results at different frequencies are summarized in Table IV. The proposed DPA can achieve an average efficiency of higher than 50% and an ACLR of better than -47 dBc at 6.5 dB back-off power (about 38 dBm) when using DPD linearization. Fig. 24 shows the measured signal spectra of normalized outputs before and after DPD. The results show that the distortion caused by the DPA can be removed effectively. For modulated signal measurements at about 6.5 dB back-off power, the proposed DPA can simultaneously achieve good efficiency and high linearity over the entire design frequency band.

V. CONCLUSION

In this paper, a broadband high-efficiency GaN DPA with 49% fractional bandwidth and its linearization results have been reported. The frequency response of the combining network for bandwidth extension of the DPA was analyzed, and a broadband DPA with integrated compensating reactance was proposed to extend the bandwidth in the back-off power region. A two-point matching technique using $ABCD$ matrix was employed to design the OMNs in the DPA. Experiment results showed that the proposed DPA achieves very good average efficiency and with high linearity performance after linearization over a wide frequency band when driven with modern modulated signals.

APPENDIX

Considering the DPA topology in Fig.1, the equations of the voltages and currents at both side of the impedance transformer can be expressed in terms of the $ABCD$ parameters as

$$\begin{bmatrix} V_C \\ I_C \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{C1} \\ I_{C1} \end{bmatrix} \quad (\text{A.1})$$

In the low-power region, the impedance seen to the right of the impedance transformer turns to be Z_L . Considering $V_{C1} = I_{C1}Z_L$, the carrier load impedance is given by

$$Z_{C_low} = \frac{V_C}{I_C} = \frac{Z_L A + B}{Z_L C + D} \quad (\text{A.2})$$

For the Doherty region, the fundamental voltage and current at the output of the carrier amplifier is written by using (A.1) as

$$V_C = AV_P + BI_{C1} \quad (\text{A.3})$$

$$I_C = CV_P + DI_{C1} \quad (\text{A.4})$$

From Fig.1, the fundamental voltage at the output of the peaking amplifier becomes

$$V_P = V_{C1} = I_{C1}Z_{C1} \quad (\text{A.5})$$

By means of (A.3) and (A.5), the following expression is obtained.

$$I_{C1} = \frac{V_P}{Z_{C1}} = \frac{V_C}{AZ_{C1} + B} \quad (\text{A.6})$$

According to the active load modulation, the following relationship arises:

$$Z_{C1} = Z_L \left(1 + \frac{I_P}{I_{C1}}\right) \quad (\text{A.7})$$

Substituting (A.6) into (A.7), the impedance Z_{C1} is expressed as

$$Z_{C1} = \frac{Z_L V_C + Z_L I_P B}{V_C - Z_L I_P A} \quad (\text{A.8})$$

According to the impedance transformation, the impedance Z_C can be expressed as

$$Z_C = \frac{Z_{C1} A + B}{Z_{C1} C + D} \quad (\text{A.9})$$

Thus, the output voltage of the carrier amplifier becomes

$$V_C = I_C Z_C = I_C \frac{Z_{C1} A + B}{Z_{C1} C + D} \quad (\text{A.10})$$

Substituting (A.8) into (A.10) and rearranging the terms results

in

$$V_C = \frac{I_P Z_L (AD - BC) + I_C (Z_L A + B)}{Z_L C + D} \quad (\text{A.11})$$

For further derivation, the following relationship is assumed:

$$\frac{I_P}{I_C} = \delta e^{j\varphi} \quad (\text{A.12})$$

where $\delta = |I_{P_sat}|/|I_{C_sat}|$ and φ is the phase of the output current of the peaking amplifier.

Taking into account (A.11) and (A.12), the carrier load impedance at saturation power can be given as follows:

$$Z_{C_sat} = \frac{V_C}{I_C} = \frac{\delta e^{j\varphi} Z_L (AD - BC) + Z_L A + B}{Z_L C + D} \quad (\text{A.13})$$

By means of (A.3) and (A.5), the following expression can be obtained:

$$V_P = \frac{V_C Z_{C1}}{AZ_{C1} + B} \quad (\text{A.14})$$

Considering (A.8), (A.11) and (A.14), the peaking load impedance at saturation is written as

$$Z_{P_sat} = \frac{V_P}{I_P} = \frac{e^{-j\varphi} Z_L + \delta Z_L D}{\delta Z_L C + \delta D} \quad (\text{A.15})$$

According to (A.2), (A.13) and (A.15), the frequency response of the DPA, including the load impedance of the carrier amplifier in low-power region, the load impedances of both two amplifiers at saturation, can be analyzed by using the $ABCD$ parameters of the impedance transformer at given frequencies.

REFERENCES

- [1] J. Moon, J. Kim, J. Kim, I. Kim, and B. Kim, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 1, pp. 143–152, Jan. 2011.
- [2] J. Kim, B. Fehri, S. Boumaiza, and J. Wood, "Power efficiency and linearity enhancement using optimized asymmetrical Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 425–434, Feb. 2011.
- [3] P. Colantonio, F. Ciannini, R. Giofre, and L. Piazzon, "Increasing Doherty amplifier average efficiency exploiting device knee voltage behavior," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp. 2295–2305, Sep. 2011.
- [4] R. Darraji and F. M. Ghannouchi, "Digital Doherty amplifier with enhanced efficiency and extended range," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 11, pp. 2898–2909, Nov. 2011.
- [5] S. Chen and Q. Xue, "Optimized load modulation network for Doherty power amplifier performance enhancement," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3474–3481, Nov. 2012.
- [6] J. Xia, X. Zhu, L. Zhang, J. Zhai, and Y. Sun, "High-efficiency GaN Doherty power amplifier for 100 MHz LTE-advanced application based on modified load modulation network," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2911–2921, Aug. 2013.
- [7] K. Bathich, A. Z. Markos, and G. Boeck, "Frequency response analysis and bandwidth extension of the Doherty amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 934–944, Apr. 2011.
- [8] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, "A transformerless load-modulated (TLLM) architecture for efficient wideband power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2863–2874, Sep. 2012.
- [9] D. Kang, D. Kim, Y. Cho, B. Park, J. Kim, and B. Kim, "Design of bandwidth-enhanced Doherty power amplifiers for handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3474–3483, Dec. 2011.

- [10] J. M. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, "A 3–3.6-GHz wideband GaN Doherty power amplifier exploiting output compensation stages," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2543–2548, Aug. 2012.
- [11] G. Sun and R. H. Jansen, "Broadband Doherty power amplifier via real frequency technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 99–111, Jan. 2012.
- [12] D. Y.-T. Wu and S. Boumaiza, "A modified Doherty configuration for broadband amplification using symmetrical devices," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3201–3213, Oct. 2012.
- [13] D. Gustafsson, C. Andersson, and C. Fager, "A modified Doherty power amplifier with extended bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 533–542, Jan. 2013.
- [14] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "A Doherty architecture with high feasibility and defined bandwidth behavior," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3308–3317, Sep. 2013.
- [15] L. Piazzon, R. Giofrè, P. Colantonio, and F. Giannini, "A wideband Doherty architecture with 36% of fractional bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 11, pp. 626–628, Nov. 2013.
- [16] C. M. Andersson, D. Gustafsson, J. C. Cahuana, R. Hellberg, and C. Fager, "A 1–3-GHz digitally controlled dual-RF input power-amplifier design based on a Doherty-outphasing continuum analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3743–3752, Oct. 2013.
- [17] M. N. A. Abadi, H. Golestaneh, H. Sarbishaei, and S. Boumaiza, "An extended bandwidth Doherty power amplifier using a novel output combining," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014.
- [18] X. Fang and K. M. Cheng, "Broadband, wide efficiency range, Doherty amplifier design using frequency-varying complex combining load," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Phoenix, AZ, USA, May. 2015.
- [19] X. Fang and K. M. Cheng, "Improving power utilization factor of broadband Doherty amplifier by using bandpass auxiliary transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2811–2820, Sep. 2015.
- [20] S. Watanabe, Y. Takayama, R. Ishikawa, and K. Honjo, "A miniature broadband Doherty power amplifier with a series-connected load," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 572–579, Feb. 2015.
- [21] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "A close-form design technique for ultra-wideband Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3414–3224, Dec. 2014.
- [22] S. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA, USA: Artech House, 2006.
- [23] X. Fang and K. M. Cheng, "Extension of high-efficiency range of Doherty amplifier by using complex combining load," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2038–2047, Sep. 2014.
- [24] A. Zhu, P. J. Draxler, C. Hsia, T. J. Brazil, D. F. Kimball, and P. M. Asbeck, "Digital predistortion for envelope-tracking power amplifiers using decomposed piecewise Volterra series," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 10, pp. 2237–2247, Oct. 2008.
- [25] L. Guan and A. Zhu, "Simplified dynamic deviation reduction-based Volterra model for Doherty power amplifiers," in *Proc. IEEE Int. Integer. Nonlinear Microw. Millimeter-Wave Circuits Workshop*, Vienna, Austria, Apr. 2011.



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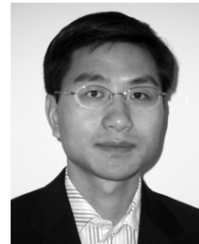
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