A 2.0-2.5 GHz Frequency-Selectable Oscillator for Digital Predistortion Model Identification of RF Power Amplifiers

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***Abstract*—This paper presents the design of a frequency selectable oscillator used as part of a new data acquisition architecture for digital predistortion (DPD) of RF power amplifiers (PAs). The proposed architecture aims to alleviate the requirement of high sampling rate analog-to-digital-converters (ADCs) in the data acquisition loop. The oscillator utilizes switchable capacitors with a digital control scheme and is capable of operating between 2.0 GHz and 2.5 GHz with an approximate frequency step size of 512 kHz.**

***Index terms* — Digital predistortion, frequency selectable oscillator, model extraction, power amplifier, switchable capacitors**

I. Introduction

The radio frequency (RF) power amplifier (PA) is a device that converts DC power into added RF signal power in wireless transmitters. It is well known that the PA is most efficient when operating in saturation but it is highly nonlinear in this region. Digital predistortion (DPD) is a digital signal processing technique that extracts the model of the PA and uses its inverse to predistort the input signal. The cascade of DPD-PA results in a linearized output signal allowing higher input power levels to be used, increasing the efficiency of the PA [1].

Before applying DPD, an accurate behavioral model must be extracted. To do so, the output of the PA is down-converted to baseband and sampled by analog-to-digital-converters (ADCs) before further digital signal processing. It is normal to characterise at least five times the input bandwidth to include the spectral regrowth introduced by the PA nonlinearities. LTE Advanced signals have 100 MHz bandwidth, and the signal bandwidth will increase further in forthcoming 5G systems, requiring ADCs to operate at multi-gigasample per second sampling rates with high resolution, typically 14 bits. Current ADCs are difficult to use at these high data rates, and so, alternate architectures are required which can perform the PA output data acquisition at a much lower ADC rate.

II. DPD Model Extraction

A. Time Domain Data Acquisition

Fig. 1 depicts the conventional data acquisition architecture used in DPD. The output of the PA is down-converted from RF to baseband, and sampled by ADCs in the time domain. The parameter extraction block then compares this data with the input signal to build a model of the DPD. Sampling the full output spectrum in the time domain requires very high sampling rate ADCs.

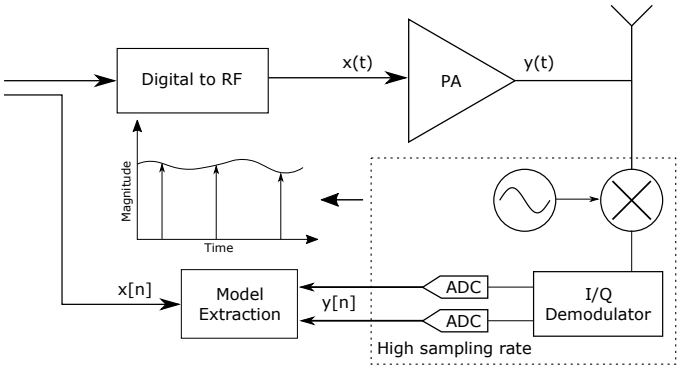

Fig. 1: Time domain data acquisition

B. Frequency Domain Data Acquisition

An alternative model extraction architecture was recently proposed [2] which performs the output signal characterisation in the frequency domain. It splits the output spectrum of the PA into segments and sequentially demodulates each segment, obtaining their Fourier coefficients.

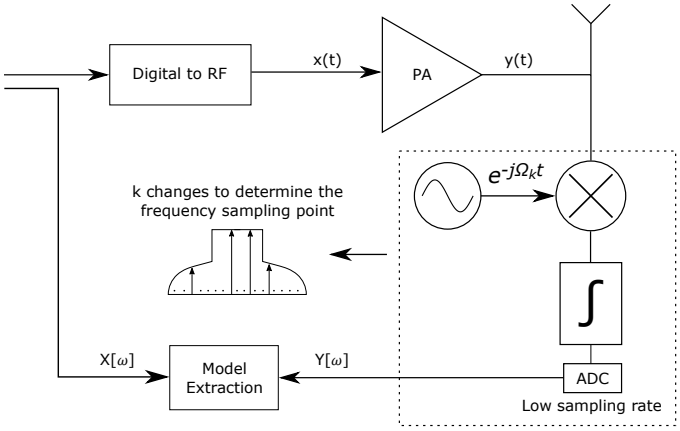

Fig. 2: Frequency domain data acquisition

The architecture for the proposed solution is demonstrated in Fig. 2. The output of the PA is first mixed with the complex signal $e^{-j\Omega_k t}$ where Ω_k is the characterisation frequency. The output of the mixer is integrated for a period of T_0 and passed through a low rate ADC. With this operation, the sample captured at the ADC output is equivalent to the frequency domain value calculated from the Fourier transform. The local

oscillator sweeps across the band, namely, by sequentially changing k, allowing the frequency domain value of the signal at different frequencies to be captured. In this approach, the ADC sampling rate is independent from the signal bandwidth which provides great advantages for future wideband applications. This paper outlines a design for the oscillator in this application.

III. Frequency-Selectable Oscillator Design

The oscillator was designed using a 28 nm CMOS process in Cadence Virtuoso. A complementary LC oscillator topology with tail current biasing was chosen due to its suitability to RF oscillation frequencies and its lower phase noise compared to ring oscillators. To allow for digitally controlled discrete frequency selection, a network of switchable capacitors was incorporated into the design. This network consists of two banks for coarse and fine tuning [3].

The coarse tuning bank uses a binary control coding scheme. Careful choice of capacitances, with parasitic elements associated with the active devices compensated for, results in equal step sizes for every coarse bank unit combination. The coarse bank consists of four different units resulting in 2^4 different frequency steps.

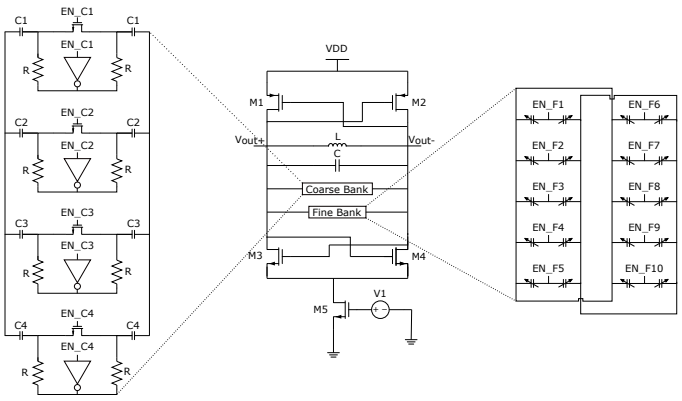

Fig. 3: Oscillator core and tuning banks

A different approach was taken for the fine tuning bank. The capacitance needed to change the frequency by 500 kHz was on the same scale as the parasitic capacitances of the CMOS switches used to turn on and off the coarse tuning units. It was therefore not feasible to continue using that approach. Instead, low capacitance varactors were used with discretized control voltages. A thermometer coding scheme was used to ensure consistency of frequency step sizes. There is both an on and off capacitance associated with the units used in the coarse bank. This makes it very difficult to choose capacitance values which will result in constant frequency steps over the full tuning range. A thermometer coding scheme, linearly turning on each unit one by one, guaranteed a constant step size. 10 units were used in the fine bank.

The oscillator and its coarse and fine tuning banks are shown in Fig. 3. The 4-bit binary coded coarse tuning bank is shown which uses resistor biasing to define a voltage between the capacitors and NMOS device while the unit is turned off. This voltage is set by the inverter and resistors R which are controlled with the same signal as the respective units. Setting the tuning range of the above described switchable capacitor networks over approximately 100 MHz provided the most consistent frequency step size. It was then decided to use five similar designs in parallel, each covering 100 MHz of the full 500 MHz tuning range. The five sub ranges are controlled by connecting or disconnecting the V_{DD} of each oscillator via an inverter. The differential outputs are connected to transmission gates which only allow the active oscillator to output a signal, minimizing interference from other circuit elements.

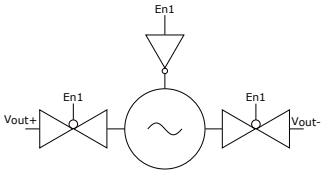

Fig. 4: One of five oscillator sub-bands

Simulation results revealed maximum and minimum oscillation frequencies of 2.498 GHz and 2.008 GHz, respectively, resulting in a frequency range of 490 MHz and a mean frequency step size of 512 kHz. A V_{DD} of 2.5 V was used and the active oscillator draws 1.18 mA from the supply. Phase noise was simulated at -124.5 dBc/Hz @ 1 MHz offset and -121.7 dBc/Hz @ 1 MHz offset for the minimum and maximum frequencies, respectively. Temperature and V_{DD} corners were analysed to investigate the variation in the oscillator's phase noise and frequency stability as shown in Fig. 6.

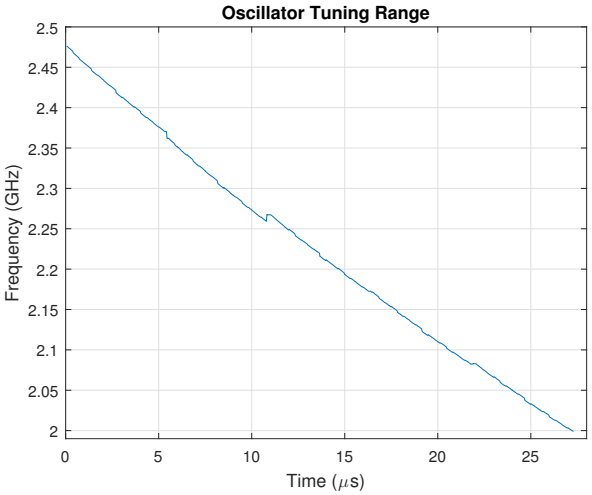

Fig. 5: Full oscillator tuning range

IV. System Simulation

The designed oscillator's efficacy in the proposed data acquisition architecture was investigated by emulating the real system in Keysight SystemVue design software. Fig. 7 shows the test bench used in SystemVue for the system simulation of the proposed sequential demodulation architecture. The input signal's in-phase and quadrature (I and Q) components are modulated on to a carrier and passed through a nonlinear PA. The output of the PA is mixed with two signals at 0° and

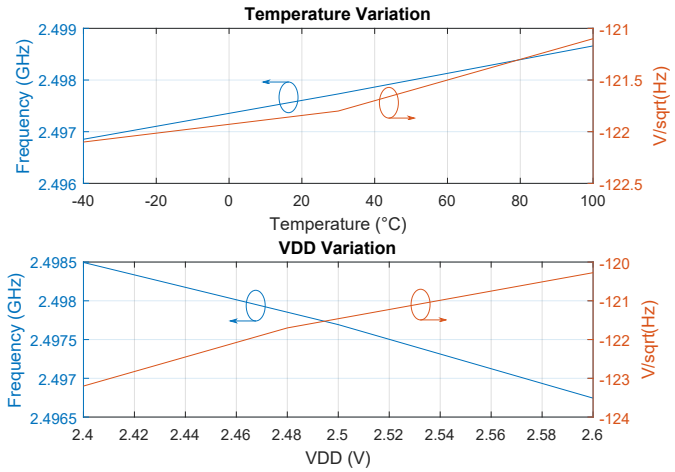

Fig. 6: Temperature and V_{DD} corners

$-90°$ which are then integrated over the number of samples equalling the input signal length. The real and imaginary parts of the Fourier Coefficient for the signal is the resultant value at the in-phase and quadrature integrator output, respectively. The oscillators then switch to a new frequency and repeat the process until the full output spectrum is characterised. These data sets are then imported to MATLAB to perform the DPD model extraction.

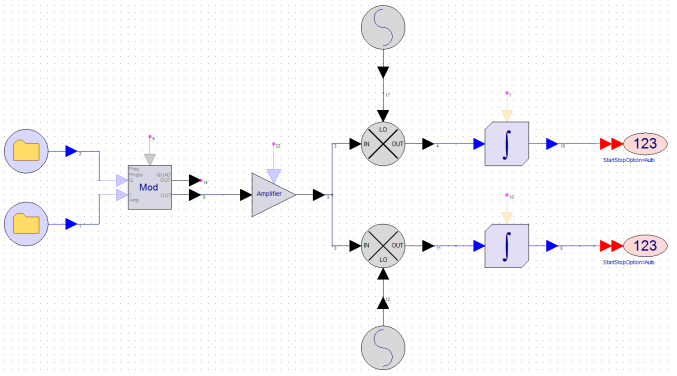

Fig. 7: SystemVue sequential demodulation test bench

There are a number of steps involved in generating the predistorted input signal using sequential demodulation which are listed below:

1) Obtain $Y[\omega]$ from sequential demodulation;
2) Build input matrix using behavioral model and apply modified DFT to every column to get $X[\omega]$ only at frequencies corresponding to those used in the sequential demodulation;
3) Solve $Y[\omega] = C_p X[\omega]$ to find C_p, the PA model;
4) Multiply the PA model coefficients by $x[n]$ to get $y[n]$;
5) Use $y[n]$ as the input and $x[n]$ as the expected output to build the inverse PA model;
6) Multiply $x[n]$ by the inverse PA model to generate the predistorted output.

Step 1 was completed in SystemVue while the rest of the steps were conducted in MATLAB. For proof of concept, the behavioral model used for step 2 was a 7$^{\text{th}}$-order memoryless polynomial model [4]. Memory models will be tested later. A modified DFT is applied to the input data to obtain Fourier coefficients only at the same frequencies as those characterised in the sequential demodulation. (1) depicts this modified DFT where X_k is the Fourier coefficient, x_n is the signal, N is the length of the signal, f is the characterisation frequency and f_s is the sampling frequency.

$$X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi n \frac{f}{f_s}} \tag{1}$$

The output of the PA with and without DPD can be seen in Fig. 8. The output with DPD has most of the distortion removed and has a normalized mean square error (NMSE) of -47.82 dB compared to the output without DPD which has an NMSE of -22.25 dB.

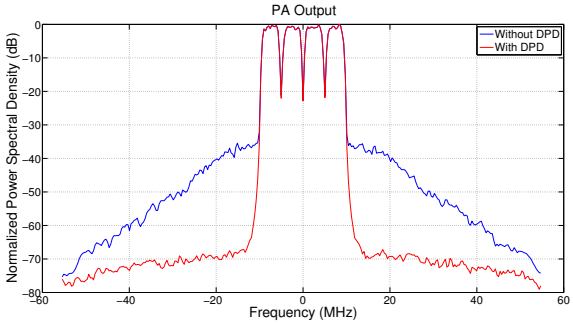

Fig. 8: PA output spectrum with and without DPD

V. Conclusion

A frequency selectable oscillator was designed with a tuning range of 490 MHz and frequency step size of 512 kHz. This oscillator is a proposed solution for one circuit block as part of a new PA data acquisition architecture which aims to characterise the output spectrum of the PA in the frequency domain to alleviate the high data rate requirements for the ADC in the feedback path.

Acknowledgment

This publication has emanated from research supported in part by a research grant from Science Foundation Ireland (SFI) and is co-funded under the European Regional Development Fund under Grant Number 13/RC/2077.

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