Low Power Real-Time Seizure Detection for Ambulatory EEG

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***Abstract*—Ambulatory Electroencephalograph (AEEG) technology is becoming popular because it facilitates the continuous monitoring of epilepsy patients without interrupting their routine life. As long term monitoring requires low power processing on the device, a low power real time seizure detection algorithm suitable for AEEG devices is proposed herein. The performance of various classifiers was tested and the most effective was found to be the Linear Discriminant Analysis classifier (LDA). The algorithm presented in this paper provides 87.7 (100–70.2)% accuracy with 94.2 (100–78)% sensitivity and 77.9 (100–52.1)% specificity in patient dependent experiments. It provides 76.5 (79.0–73.3)% accuracy with 90.9 (96.2–85.8)% sensitivity and 59.5 (70.9–52.6)% specificity in patient independent experiments. We also suggest how power can be saved at the lost of a small amount of accuracy by applying different techniques. The algorithm was simulated on a DSP processor and on an ASIC and the power estimation results for both implementations are presented. Seizure detection using the presented algorithm is approximately 100% more power efficient than other AEEG processing methods. The implementation using an ASIC can reduce power consumption by 25% relative to the implementation on a DSP processor with reduction of only 1% of accuracy.**

***Index Terms*—AEEG, ASIC, discriminant analysis, real time, low power, seizure**

I. Introduction

Epilepsy is a neurological condition characterised by a recurring tendency of the brain to produce sudden bursts of abnormal electrical activity that disrupt other brain functions [1]. Such episodes are called seizures, they occur randomly and may occur several times daily. Clinical manifestations include loss of awareness or consciousness, and disturbances of movement and sensation [2]. Epilepsy is highly prevalent, at least 8.2 per 1,000 of the general population suffer from the condition according to World Health Organisation estimates, and can have profound social, physical and psychological consequences [2].

Electroencephalogram (EEG) has been used for clinical diagnosis of epilepsy for many decades [3]. Compared to other methods such as Electrocorticogram (ECoG), EEG is a safe and clean method for detecting the activity of the brain. Clinical analysis of EEG traces for identification of seizures is well established. However, the performance of automated EEG based methods is dependant on the types of features analyzed and how they are used to classify the signal [4].

Reliable long-term, ambulatory EEG monitoring is of significant clinical value in epilepsy. It enables long-term monitoring at significantly lower cost than in-patient monitoring [1]. The ability to automatically detect seizures in real-time would further enhance its clinical value. For example, automated analysis would significantly reduce the workload of clinicians, and would help to increase the capacity of epilepsy units. In addition, a quarter of those who suffer from epilepsy unfortunately do not respond to standard therapy [5]. Automated, real time seizure detection would enable long term management of chronic epilepsy by allowing warnings to be sent and appropriate responses to be made by the subject for remote clinicians. More importantly, new 'closed loop' therapeutic interventions seek to predict and stop seizures. The ability to reliably detect seizures in real time is a pre-requisite for such interventions [5].

One key practical consideration in realizing long-term real-time AEEG based seizure detection is extending battery life such that the monitoring device can be used for several days between battery charges. Current AEEG systems focus on EEG data acquisition [6] and either wireless EEG data transmission or storage for offline processing and analysis [7]. However, power can be saved by increasing the amount of signal processing in the system. Increased signal processing in AEEG devices allows for reduced storage requirements, less transmission of data and enables real-time seizure detection. Several seizure detection algorithms have been proposed previously, but the more accurate ones tend to be computationally complex, which leads to high power consumption. There is, therefore, a clear need for high accuracy low-power seizure detection algorithms.

In this paper a low-power algorithm for real time seizure detection is presented. The algorithm was tested using data from 13 subjects, and achieved high sensitivity and reasonable specificity. We quantify the algorithm's power consumption by simulating its operation on a DSP processor and on an ASIC. Optimizations for low power, including downsampling and reduced bitwidth, are assessed both in terms of power saving and in terms of their impact on the accuracy of the algorithm. The paper compares the power consumption of processing with that of storage and transmission. To the authors' knowledge this is the first paper which has presented a low power seizure

detection algorithm and a DSP processor and an ASIC power optimized implementation.

The paper is structured as follows. After illustrating the related work in Section 2, a detailed description of the method with algorithm implementation using a DSP processor and an ASIC is presented in Section 3. Various power reduction techniques are also presented in section 3. In Section 4 the experimental results are presented. Different design options and a detailed discussion on results is presented in Section 5. The last two sections describe conclusion and future work respectively.

II. Related Work

Seizure detection using EEG has received much interest in recent years because of the availability of powerful processors. Most algorithms for detecting seizure can be categorized into one of three classes: time domain, frequency domain or wavelets, based on the type of features extracted.

One of the earliest attempts at automated seizure detection was in [8]. In this work, classification was into definite or probable events based on EEG analysis. The approach was simple and low complexity but considering the definite detections, then, overall, 58% of events were detected as definite events. Higher accuracy algorithms, which extract frequency domain features, were proposed in [9] and recently in [10]. Ref. [9] used an Artificial Neural Network (ANN) for classification and a genetic algorithm to select the best training data set. The number of iterations in the genetic algorithm was limited to 2000 and so the selected data set may not be the best. The method including pre and post processing was computationally complex. For patient specific data 91.29% sensitivity and 99.19% specificity was reported, but with patient independent data sensitivity dropped to 3% because the ANN classifier used was patient dependent and needed to be trained separately for different patients. The algorithm proposed in [10] required wavelet and Fast Fourier Transform (FFT) calculations. The authors reported 80 to 98% sensitivity but the method was patient-specific. It used Support Vector Machine (SVM) for classification. Ref. [11] proposed a slightly different two-stage approach for seizure detection. Features were extracted using wavelet decomposition. Ref. [12] proposed a simple method to detect seizures using the line length of the EEG signal. The method tunes the line length threshold for each patient and a very low false rate of less than 1 false signal per hour was reported. However, the results may vary significantly with variations in the threshold. Ref. [13] studied linear and non-linear methods for automatic seizure detection in scalp EEG recordings. They used both time and frequency domain features. The proposed method, multi dimensional probability evolution (MDPE), showed 100% accuracy in seizure detection but the experiments were performed on a very small database. The authors used 8 seizures each of at least 40 seconds.

The general trend in automated seizure detection has focused on high accuracy without considering its implementation, which is a crucial part of designing an EEG-based automated seizure detection device. The computational complexity and power consumption of the algorithm play important roles in system design and should be considered carefully. Exploration and comparison of different design options have not been considered in previous work. Implementation of these options allows the designer to trade power for accuracy.

III. Method

A. EEG Data

The EEG data used were obtained from the Freiburg EEG database [14] (Table III-A). 13 epilepsy patients aged 10 to 50 provided around 1 hour each of continuous 6-channel EEG. The data were originally acquired using a Neurofile NT digital video EEG system with 128 channels and sampled at 256 Hz using a 16 bit analog-to-digital converter.

The data were separated into sets of seizure and nonseizure data based on information provided in [14]. Both seizure and nonseizure data were further divided into continuous 32-second epochs with no overlap. We maintained the proportion of seizure and nonseizure EEG data in the training set for each patient to avoid patient specific training of the classifier. To check the robustness of the algorithm we used the Matlab random function to divide the EEG data into training sets and testing sets. Each training and testing set might have data in different proportions from different patients but this is a common case in real life. We used a 10-fold cross validation to check classifier performance to avoid bias.

B. Algorithm

We propose a simple and computationally inexpensive approach based on the algorithm presented in [15]. A schematic of the approach is shown in Figure 1. There are three main stages of the algorithm:

1) Preprocessing
2) Feature Extraction
3) Classification

These are described in more detail below.

1) Preprocessing: Generally, preprocessing is required to remove artifacts from the EEG data. Artifacts are one of the major problems in EEG processing. EEG signals are prone to impairment by other signals such as electromyograph (EMG) and electrocardiograph (ECG) [16]. To reduce complexity, we bandpass filtered the EEG data according to the standards published in [17] and [18]. EEG data were bandpass filtered using an FIR Kaiser window filter of order 25 in the range 0.3-80 Hz.

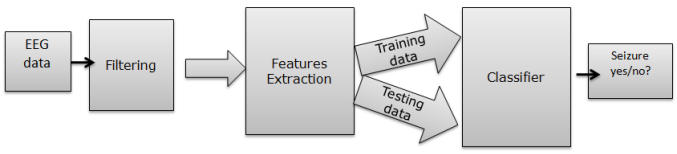

Fig. 1. A Brief Overview of the Algorithm

TABLE I
EEG DATA DETAILS

Patient no	Gender	Age	Seizure type	Origin	Nonseizure data analysed (minutes)	Seizure data analysed (minutes)
1	M	14	SP,CP	Frontal	35.2	44.8
2	F	26	SP,CP, GTC	Temporal	32	41.6
3	F	16	SP,CP, GTC	Frontal	12.8	22.4
4	M	44	CP,GTC	Temporo/ Occipital	48	54.4
5	M	47	SP,CP, GTC	Temporal	25.6	35.2
6	F	10	SP,CP, GTC	Parietal	57.6	57.6
7	F	42	SP,CP, GTC	Temporal	12.8	12.8
8	F	41	CP,GTC	Fronto/ Temporal	80	80
9	M	31	SP,CP, GTC	Temporal	48	57.6
10	F	50	SP,CP, GTC	Temporal	51.2	57.6
11	M	28	SP,CP, GTC	Temporal	22.4	22.4
12	M	33	SP,CP, GTC	Tempo/ Parietal	35.2	41.6
13	M	13	SP,CP	Temporal	35.2	38.4
Total (for all 6 channels)					**496**	**566.4**

SP = simple partial, CP = complex partial, GTC = generalized tonic-clonic

2) Feature Extraction: It is important to select the features carefully otherwise it may reduce the performance of the classifier [19]. The results reported in [15] showed that some frequency domain features are useful for distinguishing between seizure and nonseizure data. However, obtaining frequency domain features requires conversion of the signal to the frequency domain which consumes significant power and requires considerable processing time in embedded systems. So, to keep the complexity of the algorithm at the possible lowest level we selected five time domain features based on our observations and the results presented in [15]. All the features were extracted for each 32 seconds of epoch. The five selected features are:

- **RMS (Root Mean Square):** RMS is a good signal strength estimator [20]. The RMS (γ) for an epoch of *N* samples was calculated using:

$$\gamma = \sqrt{(\sum_{i=1}^{N}[x(i)]^2)/N} \quad (1)$$

- **Number of Maxima and Minima:** The number of maxima and minima are useful to test the rate of change of the signal. The maxima/minima can be global or local. We calculated the number of local minima and maxima for each EEG epoch.

- **Line Length:** Line length was proposed in [12] as a promising feature for differentiating between seizure and nonseizure data [12]. We used the following equation for calculating line length (ℓ) over *N* samples:

$$\ell = \sum_{i=1}^{N} abs[x(i-1) - x(i)] \quad (2)$$

- **Nonlinear Energy:** Nonlinear energy emphasizes the artifacts [21] and has been used both as a feature and for artifact removal [15] [22]. Nonlinear energy (η), for an epoch of *N* samples, was calculated using

$$\eta = (\sum_{i=1}^{N}[x^2(i) - x(i+1)x(i-1)])/N \quad (3)$$

3) Classification: We compared Linear Discriminant Analysis (LDA), Quadratic Discriminant Analysis (QDA), Mahalanobis Discriminant Analysis (MDA) and Support Vector Machine (SVM) classifiers. The performance of different classifiers for the same features in terms of sensitivity, specificity and accuracy were compared. For this work, all epochs were successfully classified, i.e. a 100% classification rate was obtained. The following definitions were used:

- Sensitivity: Correctly Classified Positive Epochs
- Specificity: Correctly Classified Negative Epochs
- Accuracy: Correctly Classified Epochs
- Error rate: Incorrectly Classified Epochs

LDA is popular because its linearity makes its estimated posterior probability of group membership and the implicit regions of allocation very easy to determine [23]. LDA can be used to classify multiple classes, in this case as we have only two, its classification frontier is a straight line or hyperplane. We define the group prior probabilities relative to the group frequencies in training LDA. The classifier was trained independently of the number and types of channel. When the data were divided into training and testing data sets, the data from all the channels were blended and the number and types of channel were not mentioned to obtain channel independent results. As a random function was used to divide the data into training and testing data sets, training data sets might or might not contain the data from the patient for which the performance evaluation of the classifier was going to be carried out.

To allow comparison with the performance of the algorithms presented in [9] and [10], patient dependent results using LDA for all 13 patients are also presented. The patient dependent results were obtained by using the data for testing and training from the same patient. The same validation method is used here as described in the next section.

C. Validation

k-fold cross validation was applied to test the algorithm in all cases. In this method, the extracted features were divided into *k* sets randomly. The classifier model was trained using *k*-1 sets and tested using the remaining data set. This process was repeated *k* times. Here 10-fold cross validation was used. However, in SVM classification 5-fold cross validation was used because it was highly computationally complex

and required considerable time for convergence. The Matlab R2007, the statistics toolbox was used for discriminant analysis and the bioinformatics toolbox was used for SVM analysis. In SVM classification, a linear kernel (dot product) was used. To compare the performance of different classifiers, a Matlab classifier performance object (CP) was used which accumulated the results of classifier and classperf interface to keep track of performance during validation of the classifiers [24].

D. Power Reduction Techniques

A number of power reduction techniques were applied to the algorithm. They are described below.

1) Downsampling: One of the most popular and simple power saving techniques is downsampling. In the EEG signal most of the information is concentrated in the 0.5-70 Hz range [19] [25]. Therefore downsampling from 256 Hz to a minimum of 32 Hz was evaluated. For each frequency the bandpass filtering range was adjusted to meet the Nyquist criteria.

2) Reduction in bitwidth: It is possible to save energy by reducing bitwidth if the algorithm is implemented on an ASIC. We used (4) to reduce the original bitwidth w of the input data X to bitwidth w'.

$$X' = \lfloor (X/(2^w - 1)) \times ((2^{w'}) - 1) \rfloor \tag{4}$$

3) Hardware Approximation: It is also possible to reduce the power required by an operation by simplifying (1) and (3). One of the most common techniques for reducing the power consumption at the processing level is to replace the multiplication operations by add and shift operations [26]. The following simplified equations were used to reduce the number of multiplications in the algorithm.

1) RMS: Equation (1) can be replaced by

$$\gamma' = (\sum_{i=1}^{N} |x(i)|)/N \tag{5}$$

2) Nonlinear Energy: Equation (3) can be replaced by (6). In addition, the value of (5) can be reused in (6) which can save further operations at the expense of memory.

$$\eta' = (\sum_{i=1}^{N} |x(i)|)/N - (\sum_{i=1}^{N} |x(i+1) - x(i-1)|) \tag{6}$$

E. DSP Processor Implementation

TI's C5510 DSP processor, TI Code Composer Studio (CCS) 5.9 and Power Composer 1.0 [27] were used to measure the power consumption of a processor based implementation. The TI C5510 is a fixed point low power and low cost DSP processor [28]. All the floating point variables were converted to fixed point variables [29]. By taking into consideration the accumulator wordlength (A), data wordlength (L) and filter coefficient quantization error, the floating point numbers were scaled using (7) and normalized after processing.

$$\xi = min(\lfloor log_2((2^{M-1} - 1)/max(|b_i|)) \rfloor, A - L - \lceil log_2 \alpha \rceil) \tag{7}$$

where $\alpha = \sum_{i=0}^{N-1} |b_i|$, M is the maximum filter coefficient word length and b_i is the filter coefficients.

Power Composer is a software tool which plugs into CCS. It measures cycle-by-cycle power consumption by analyzing assembly instructions. It has an accuracy of 97% and measurements were taken at 1.6 V, 24 MHz [27].

F. ASIC Implementation

As the microprocessor's fixed bitwidth and architecture do not allow certain power reduction techniques to be reflected, the algorithm was implemented in Verilog Hardware Description Language (HDL). The code was simulated using the Modelsim Verilog simulator for a single channel and then scaled for 6 channels. The code was synthesized using the Synopsys Design Compiler (DC) for TSMC 0.13μm CMOS technology. The area, power and timing results were also analyzed using the Synopsys DC and PrimeTime tool suite. The operating voltage was 1.2 V.

IV. Results

A. Performance Comparison of Various Classifiers

Table II shows a comparison of the performance of various patient independent classifiers.

TABLE II
CLASSIFIER PERFORMANCE COMPARISON (PATIENT INDEPENDENT)

	LDA	**QDA**	**MDA**	**SVM**
Sensitivity (%)	91.8	97.8	33.7	89.3
Specificity (%)	59.0	41.2	81.0	59.3
Accuracy (%)	76.5	71.6	60.2	75.3

Based on these results, LDA was chosen because of it has the least computational complexity and any increase in accuracy by using more complex classifiers such as Support Vector Machine (SVM) was not found to be significant.

B. Patient Dependent LDA Results

Table III shows patient dependent LDA performance for 13 patients. When the classifier was trained and used for the same patient an increase in accuracy of more than 10% increase was achieved.

C. Effect of Change in Epoch Size

The epoch size was varied and the results are shown in Table IV. It is apparent from the results that the larger the epoch size, the greater the accuracy because more information is available to analyze the seizure activity.

D. Effect of Downsampling

As most of the information of EEG data in the range 0.5–70 Hz, a dramatic reduction in the correct rate after a downsampling factor of 4 (from 256 Hz) can be seen (Table V).

TABLE III
PATIENT DEPENDENT LDA RESULTS

Patient No	Sensitivity (%)	Specificity (%)	Accuracy (%)
1	100	77.2	90
2	100	75	89.1
3	100	79.2	92.4
4	100	100	100
5	83.3	52.1	70.2
6	100	86.1	93.1
7	91.7	70.8	81.2
8	78	82	80
9	98.1	78.9	89.4
10	97.2	77.1	87.7
11	100	100	100
12	96.1	71.2	84.7
13	84.7	80.3	82.6
Average	**94.2**	**77.9**	**87.7**

TABLE IV
EFFECT OF CHANGE IN EPOCH SIZE USING LDA CLASSIFIER

Epoch size (sec)	Sensitivity (%)	Specificity (%)	Accuracy (%)
32	91.8	59.0	76.5
28	88.2	59.6	74.2
24	89.1	57.6	74.0
20	88.1	56.2	72.6
16	87.1	58.1	72.8
12	88.3	57.1	72.7
8	86.1	57.8	71.9
4	84.9	57.6	71.1

TABLE V
EFFECT OF DOWNSAMPLING USING LDA CLASSIFIER

Downsampling factor	Sampling Frequency (Hz)	Sensitivity (%)	Specificity (%)	Accuracy (%)
1	256	91.8	59	76.5
2	128	92.4	57.4	76.1
4	64	90.4	55.4	74.1
8	32	77.2	53	65.9

E. Effect of Change in Bitwidth of Input Data

Table VI shows the effect on the performance of the algorithm when bitwidth was reduced.

TABLE VI
EFFECT OF CHANGE IN BITWIDTH OF INPUT DATA USING LDA CLASSIFIER

Change in Bitwidth	Sensitivity (%)	Specificity (%)	Accuracy (%)
0	91.8	59	76.5
2	87.9	60.3	75.0
4	87.5	60.8	75.1
6	84.1	61.4	73.5
8	79.1	61.2	70.8

After a reduction in bitwidth of more than 6 bits, the number of maxima and minima became zero and so they were removed from the list of features and after a reduction in bitwidth of more than 16 bits, it was not possible to train QDA and MDA classifiers because most of the terms became 0 or negative.

F. Effect of Hardware Approximations

Table VII shows the effect of hardware approximation on our algorithm.

TABLE VII
EFFECT OF HARDWARE APPROXIMATION USING LDA CLASSIFIER

	Sensitivity (%)	Specificity (%)	Accuracy (%)
Before	91.8	59	76.5
After	81.0	61.6	72.0

G. Power Consumption in DSP processor

We measured the power consumption of processing on TI's C5510 DSP processor. The average current consumption was 12.83 mA with an average cycles count of 777 for processing of a single sample and total processing time of 218 ms. So, the processor can be operated at around 200 kHz which is far less than the minimum operating frequency of most DSP processors. Because of the low operating frequency the algorithm can be run on a modern micro-controller with a MAC unit as most of them have a clock frequency of at least 5 MHz [30] [31]. The power consumption was calculated using the information in [32], giving 80.8 μW per channel. In this work, we assume 6 channels, giving total power consumption of 484.8 μW.

H. Power Consumption in ASIC

The power consumption of the ASIC for different design options is shown in Table VIII. Hardware approximation reduced power consumption by more than 15% while bitwidth reduction by 6 bits reduced power consumption by more than 60% because of reduced switching activity and cell leakage power. When different design options are discussed in this and following sections, bitwidth of input data was reduced by 6 bits, the EEG data were downsampled by factor of 4 and all the hardware approximations were applied.

TABLE VIII
POWER CONSUMPTION OF DIFFERENT ASIC DESIGNS FOR SINGLE CHANNEL EEG DATA PROCESSING

Implementation Option	Power Consumption (μW)
Without any Power Reduction Technique	29.8
With Downsampling (by factor 4)	7.4
With Hardware Approximations	25
With Reduction in Bitwidth (by 6 bits)	12.5
With Hardware Approximations & Reduced Bitwidth	10.8

V. DISCUSSION

Based on the results in the previous section, different EEG data processing options were selected and compared in terms of sensitivity, specificity, accuracy and power consumption and the findings are summarized in Table IX. The power consumption results are for a single channel EEG data processing. The sensitivity, specificity and accuracy results are for patient independent scenario. The first two options, A and B, are for

the implementation using a DSP processor while rest of the design options are for implementation using an ASIC. It can be observed in Table IX that the power consumption of presented seizure detection algorithm consumes up to 6 times less power in implementation using an ASIC than the implementation using a DSP processor.

Using the results from the previous section a rough estimation of the life span of a battery operated seizure detection device was obtained as shown in Table X. A single LCC class battery having 250 mAh capacity was used for lifetime calculation of different design options [25]. Here, power consumption of 6-channel 16 bits Analog to Digital Converter (ADC), 6-channel EEG signal acquisition system, Phase-Locked Loop (PLL) and 32-kHz crystal oscillator was taken into account as 84 μW [33], 225 μW [34], 40 μW [28] and 7 μW [35] respectively. The power consumption of Toshiba 16MB NAND flash, 52 μW [36], was used for storing EEG data from 6 channels at 256 Hz sampling rate. In EEG data transmission, the power consumption of transceiver was considered as 500 μW [37]. In EEG data compression 150 μW of power consumption was taken into account for 0.25 compression ratio [25]. The considered EEG data processing option from Table IX is also mentioned in Table X.

TABLE X
POWER CONSUMPTION AND LIFETIME OF DIFFERENT DESIGNS

System	**Total Power (μW)**	**Lifetime (weeks)**
Store EEG data in flash	407	5.2
Transmit all EEG data	856	2.5
Transmit compressed EEG data	756	2.6
Store compressed EEG data	456	4.2
Detect seizure in real-time, store EEG data and transmit alarm signals (Option B)	539	4
Detect seizure in real-time, store EEG data and transmit alarm signals (Option G)	436	5

The storage of EEG data in flash is the least power consuming but does not allow real-time seizure detection. However, flash is useful for storing EEG data for clinical inspection. It is clear from the results that a system with real-time seizure detection can increase the life time of a system by 37% using a microprocessor implementation and 100% using an ASIC implementation, with 2% and 3% of reduction in accuracy respectively, when compared with a wireless EEG device transmitting all of the EEG data. It can be also observed from Table IX that the power consumption of the presented seizure detection algorithm using ASIC implementation is 6 times less than the implementation using a DSP processor. When power consumption of all the components of a typical AEEG device was considered [25] the implementation of the system using an ASIC can increase lifetime by 25% when compared to the implementation using a DSP processor. As the complexity of algorithm increases, the ASIC design requirement becomes more essential to increase the battery lifetime. However, the high design cost of ASIC development necessitates a domain specific approach, targeting a wide range of biomedical applications. As the proposed algorithm does not have high accuracy, it could also be used as a screening algorithm in a two stage seizure detection method, as proposed in [11]. A device can use the proposed algorithm most of the time and switch to a higher accuracy, higher complexity, algorithm when suspicious events are detected. This would reduce power consumption overall while increasing the accuracy.

VI. CONCLUSION

In this paper, a low power real time seizure detection algorithm for AEEG was proposed. The performance of various classifiers was compared and LDA was found to be the best choice for implementation. The proposed algorithm achieved 94.2% sensitivity and 77.9% specificity with an overall accuracy of 87.7% in patient dependent experiments and 91.8% sensitivity and 59.0% specificity with an overall accuracy of 76.5% in patient independent experiments. Simulation of the algorithm was performed for a DSP processor and for an ASIC. The lifetime of the whole system with different optimization options was calculated. The algorithm was tested with different power saving techniques. The techniques provided up to 5 times saving in power with only 3% reduction in accuracy (Option G) relative to design without any power reduction technique (Option C). The ASIC implementation of the algorithm was 25% less power consuming than the implementation using a DSP processor.

VII. FUTURE WORK

More accurate features are required for seizure detection. The latency in seizure detection can be an issue and hence an algorithm should be able to detect the seizure as soon as possible. Most epilepsy patients have seizures during 2-5% of their lifetime [3]. So, it is necessary to deploy an algorithm with a lower false alarm rate. Although different classifiers are compared in this paper, the performance of the algorithm could perhaps be improved by using another classifier or other features. The significant saving in power consumption using an ASIC implementation suggests the need for careful and thorough research on a biomedical domain specific ASIC.

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TABLE IX
DIFFERENT EEG DATA PROCESSING OPTIONS COMPARISON FOR A SINGLE CHANNEL PATIENT INDEPENDENT SCENARIO

Device	Option	Down-sampling (factor 4)	Bitwidth Reduction (6 bits)	Hardware Approximations	Sensitivity (%)	Specificity (%)	Accuracy (%)	Power Consumption (μW)
DSP processor	A				91.8	59	76.5	80.8
DSP processor	B	$\surd$			90.4	55.4	74.1	20.2
ASIC	C				91.8	59	76.5	29.8
ASIC	D	$\surd$			90.4	55.4	74.1	7.4
ASIC	E	$\surd$		$\surd$	91	49.7	71.8	6.2
ASIC	F		$\surd$	$\surd$	74.9	63.4	69.5	10.8
ASIC	G	$\surd$	$\surd$		90.5	54.7	73.8	3.1
ASIC	H	$\surd$	$\surd$	$\surd$	91.5	50.5	72.4	2.7

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