Fractional Spur Suppression in All-Digital Phase-Locked Loops

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***Abstract*—In this paper, fractional spur suppression techniques for all-digital PLLs (ADPLLs) are summarized. The attention is paid to the recently proposed digital-to-time converter (DTC)-based ADPLL architecture. DTC's nonlinearity dominates the fractional spurs contribution. Its influence is modeled with a pseudo phase-domain ADPLL and its relationship with the spur level is quantitatively described. An LMS algorithm is adopted to calibrate the DTC gain. Furthermore, an improved adaptive algorithm is proposed to suppress the fractional spurs.**

I. Introduction

CMOS technology scaling favors the utilization of all-digital phase-locked loops (ADPLLs) for frequency synthesis [1]. One practical limitation of ADPLLs is fractional spurs, which occur when the PLL is in a fractional-N frequency relationship during which the frequency command word FCW = f_V/f_R is very close to an integer (i.e., so-called an "integer-N" channel) [2]. f_V is the generated variable frequency output; f_R is the input reference frequency. The fractional spurs are fundamentally due to the finite quantization of the phase detection mechanism [e.g., time-to-digital converter (TDC) resolution] and were first studied in [3]. Furthermore, TDC imperfections, such as wrong estimation of its gain as well as its non-linearities can worsen the fractional spurs. Frequency locations of these fractional spurs vary with FCW, but only for very small fractional values of FCW (when interpreted as in a signed format) they are close enough to dc, thus not being filtered out by the loop filter and causing undesired modulation of the oscillator.

Numerous techniques have been proposed to suppress the fractional spurs. In the traditional divider-based ADPLL, $\Sigma\Delta$ modulator is adopted to dither the divider value. However, the large quantization noise of the oscillator cycle period and TDC nonlinearity can severely affect the performance, especially for higher-order $\Sigma\Delta$ modulators producing large clock edge excursions. In the counter-based ADPLL, the TDC gain must be calibrated for process, voltage and temperature (PVT) variations, otherwise large fractional spurs could result. However, such calibration is quite straightforward and could be done entirely in the digital domain. Recent ADPLL architectural improvements replace the TDC with a digital-to-time converter (DTC) [4] and a combination of DTC and TDC [5] [6] [7] .

II. Fractional Spurs

In [8], two techniques were proposed to reduce the level of fractional spurs: A gated-ring oscillator (GRO) TDC is used to first-order shape the TDC quantization noise and mismatches; and a digital correlation loop is applied to improve the phase noise performance. The key to algorithmic fractional spur minimization is "correlation" and an LMS algorithm should be formostly considered. Furthermore, in [4], a sign-error LMS algorithm is used to adjust the DTC gain. Moreover, Goertzel DTFT algorithm is included in the noise cancellation technique, which complicates the design. For the divider-based ADPLL, an excellent work is done in [9]. A TDC produces a multi-bit output and the DTC nonlinearity correction correlates the accumulated FCW_f (fractional part of FCW) and the detected phase error. This correction method is applied on the phase error before the digital loop filter, rather than the DTC gain. When PVT changes, TDC still has to cover a large range. TDC element scrambling is adopted to linearize the TDC performance at the price of increasing the in-band noise floor. When only the correlation loop to compensate the DTC gain error is enabled, the largest spur level drops from -24 dBc to -44 dBc. When the DTC nonlinearity correlation part is also enabled, the largest spur level drops to -57 dBc.

In another ADPLL [7], a single-bit TDC and two-stages of DTCs are chosen. A coarse stage and a fine stage DTC follow the integer divider of the oscillator clock. Now, the multipath correlation scheme is applied on the coarse DTC, which can cancel its nonlinearity. As for the fine DTC, correlation is used only to calibrate its gain. The largest in-band fractional spur achieved is lower than -52 dBc, keeping the same in-band noise floor level. Then, a multipath correlation scheme is applied on the fine DTC, achieving -67 dBc in-band fractional spur level. The whole background calibration is termed there a pre-distortion. In [10], the spur cancellation is also based on correlation, but it is gradient-based and can reduce the spur level by more than 20 dB. Even for an analog PLL [11], correlation can still be used to adjust the DTC gain.

III. DTC Nonlinearity's Effect on Fractional Spurs

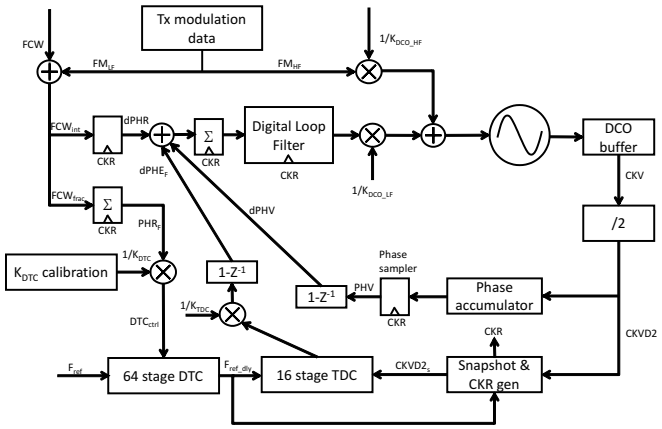

Fig. 1: DTC-based ADPLL architecture.

In the following, spurs in the DTC-based ADPLL will be described. This ADPLL architecture is shown in Figure 1, which derives from the traditional counter-based ADPLL [1]. The reference signal is first delayed by DTC before it is fed into the TDC. Thus, the rising edge of the delayed reference signal is almost aligned with the rising edge of the DCO output signal, thus shortening the TDC measurement range [6]. This principle is called phase prediction, which takes the advantage of DTC over TDC due to the fact that DTC makes it easier to achieve lower power and better linearity.

The linearity requirements in this DTC-based ADPLL are shifted from TDC to DTC, so the fractional spurs mainly originate from DTC. In this section, DTC's influence on the fractional spurs is discussed. There are two ways to quantify the DTC nonlinearity's influence on the fractional spur level. One is the traditional method, starting from the frequency modulation equation. Another is the proposed pseudo-phase-domain method, which is derived with the help of z-transform. In the traditional method, the DCO output jitter is assumed to be equal to the DTC nonlinearity, provided other parts are ideal. While the new method gives a direct relationship between DTC nonlinearity and the DCO output jitter, after we get the jitter's transient information, the following calculation can be done in the regular way as the traditional method.

A. Traditional Method

The traditional method takes the DCO output clock as a starting point. The information needed is the deviation of the normalized tuning word (NTW) value. Due to the periodic operation of DTC, NTW has a frequency component at FCW$_f \cdot f_R$. The ADPLL is thus frequency modulated. Generally, the DCO output signal can be written as $V_0 = A\sin(\omega_0 t + \theta(t))$, where A is defined as the signal's amplitude, $\omega_0 = 2\pi f_0$ is the carrier frequency, $\theta(t)$ takes account of the initial phase and its subsequent variations. Ideally, there would be only one tone at V_0 frequency spectrum, the amplitude would be a constant A, and the phase would be a constant $\theta(t)$. However, as thermal and flicker noise exist inside DCO, there is phase noise, making $\theta(t)$ fluctuating over time.

Let us consider a special case: a single sinusoidal tone modulates the phase: $\theta(t) = \theta_p \cdot sin(\omega_m t)$, where $\omega_m(t)$ is the modulating frequency. When the peak phase deviation, θ_p, is much smaller than 1, the single sided spectral density can be approximated as

$$S_{V_0}(\omega) = \frac{A^2}{2}\delta(\omega-\omega_0) + \frac{A^2}{2}[\frac{\theta_p^2}{4}\delta(\omega-\omega_0-\omega_m) + \frac{\theta_p^2}{4}\delta(\omega-\omega_0+\omega_m)] \quad (1)$$

It is evident that the phase modulating tone is translated by the carrier frequency ω_0 to appear on both sides of ω_0. As an example, if the DCO frequency is 4 GHz and the DCO jitter is $\sigma_{\Delta\tau}$ = 2.6857 ps, then $\theta_p = 2\pi\frac{\sigma_{\Delta\tau}}{T_0} = 2\pi\frac{2.6857\,ps}{250\,ps} = 0.0675$ rad where $T_0 = 2\pi/\omega_0$. Because the in-band phase error transfer function is flat at unity, DTC's INL can be assumed to be the DCO's jitter. The fractional spur level can be written as

$$\begin{aligned}\mathcal{L}_{\Delta\omega_m} &= 10\log_{10}(\frac{\theta_p^2}{4}) \\ &= -29.43\,dBc\end{aligned} \quad (2)$$

In the traditional method, there is one important assumption: DTC nonlinearity is equivalent to the DCO output signal's jitter. It is acceptable in-band. Furthermore, in the above derivation, θ_p is small. When it grows larger, the Bessel function of first kind should be used to calculate the fractional spur level. Generally, formula (2) is useful when the fractional spur level is below -20 dBc.

B. Pseudo-Phase Domain Method

We now study the fractional spurs from a different perspective. A pseudo phase-domain ADPLL is set up in Figure 2. It is termed "pseudo-phase" because the phase is in the units of 2π rad rather than 1 rad. One period of T_V corresponds to a phase of 2π rad.

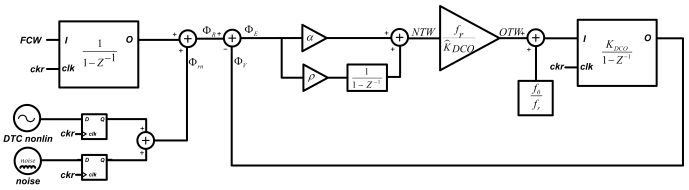

Fig. 2: Pseudo phase domain ADPLL.

Φ_{rn} disturbance consists of the reference noise and DTC nonlinearity, $\Phi_{DTC,n}$. The working principle of the DTC-counter-based ADPLL reveals that the DTC nonlinearity directly phase-modulates the reference signal. $R_R[k] = \sum_{l=1}^{k} FCW + \Phi_{DTC,n}$. In the following analysis we assume that the TDC has sufficiently fine resolution to neglect the quantization noise while the DCO quantization noise and thermal noise are vanishingly small. Only two non-ideal effects are taken into consideration: reference noise and DTC nonlinearity. Assume DTC has a sinusoidal INL curve when the digital control word sweeps one cycle. INL$_{pp} = 0.2LSB$. DTC unit delay is 25 ps. In the ADPLL, the reference frequency is 50 MHz and FCW equals 80. $T_V = 250\,ps$. The variance of timing uncertainty is $\sigma_t^2 = (\frac{\text{INL}_{pp}\cdot T_{DTC}}{2\sqrt{2}})^2$. Normalized to the unit interval and multiplying by 2π radians: $\sigma_\phi = 2\pi\frac{\sigma_t}{T_V}$. That value has to be divided by 2, to transfer the single-sided spectrum into double-sided spectrum. Thus the fractional spur level can be written as

$$\begin{aligned}\mathcal{L} &= \frac{\pi^2}{4}(\frac{\text{INL}_{pp}T_{DTC}}{T_V})^2 \\ &= -30.06\ dBc/Hz\end{aligned}$$

Up to this point, this formula is actually the same as formula (2), just obtained through a different derivation method. This is because they directly link NTW to the DTC nonlinearity.

To validate the effectiveness of the formulas above, a simulation result is given in Figure 3. The reference noise is $-114\,dBc/Hz$. $\alpha = 0.156$.

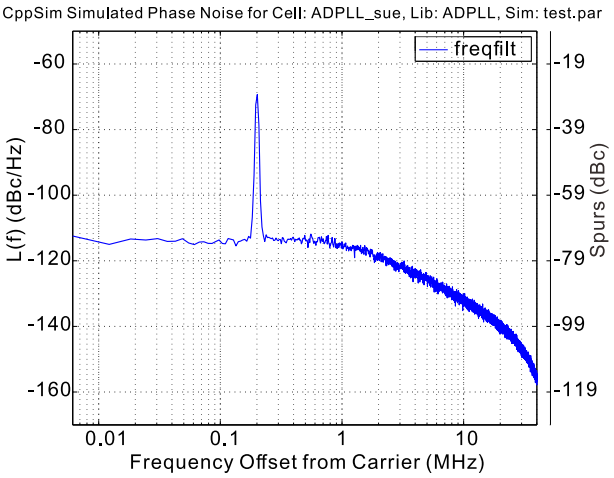

Fig. 3: Simulated fractional spur level.

The fractional spur level is simulated to be $-28.80\,dBc/Hz$. The estimation error of the fractional spur level is only 1.26 dB, which is small enough to be accepted. It proves that formula (3) is very helpful to determine the in-band spur level.

To close the gap between the simulation result and the theoretical value, further derivation is done to give a precise relationship between NTW and DTC nonlinearity. In Figure 2, following equations are valid.

$$\Phi_E[k] = \Phi_R[k] - \Phi_V[k] \quad (3)$$

$$\Phi_R[k] = k \cdot FCW + \Phi_{rn}[k] \quad (4)$$

$$\Phi_V[k] = k \cdot \frac{f_0}{f_r} + \sum_{n=1}^{k} NTW[n] \quad (5)$$

$$NTW[k] = \alpha\Phi_E[k] + \rho \sum_{n=1}^{k} \Phi_E[n] \quad (6)$$

$$\bar{\Phi}_E = 0 \quad (7)$$

What interests us is how Φ_E and NTW change as Φ_{rn}. Formula 6 can be written as $NTW[k] = k_c + \alpha\Phi_E[k] + \rho\sum_{n=m}^{k}\Phi_E[n]$. k_c is a constant, given by $\rho\sum_{n=1}^{m-1}\Phi_E[n]$, which approximates FCW $-\frac{f_0}{f_r}$. Formula 3, formula 4 and formula 5 give

$$\begin{aligned}\Phi_E[k] &= k \cdot FCW + \Phi_{rn}[k] - k \cdot \frac{f_0}{f_r} - \sum_{n=1}^{k} NTW[n] \\ &= k \cdot (FCW - \frac{f_0}{f_r} - k_c) + \Phi_{rn}[k] - \\ &\quad \sum_{l=2}^{k}(\alpha\Phi_E[l] - \rho \sum_{n=m}^{l} \Phi_E[n]) \end{aligned} \quad (8)$$

The formula above can be simplified by taking $k_c = \text{FCW} - \frac{f_0}{f_r}$. It is based on the fact that in type-II system, the phase error approaches zero. As the above equation shows, the first term should be zero, independent of k. Then the remained terms also equal zero. By z-transform, we can get

$$\Phi_E = \frac{1 - 2z^{-1} + z^{-2}}{(1 + \alpha + \rho) - (\alpha + 2)z^{-1} + z^{-2}}\Phi_{rn} \quad (9)$$

$z = e^{sT_r} \approx 1 + sT_r = 1 + 2j\pi f_{rn}T_r$. If we only consider DTC nonlinearity, then f_{rn} is the fractional spur's frequency, which is 200 kHz in the simulation. Then

$$\begin{aligned}|\theta_p| &= \frac{f_r}{f_{rn}}|\alpha + \frac{\rho}{1 - z^{-1}}||\frac{1 - 2z^{-1} + z^{-2}}{(1 + \alpha + \rho) - (\alpha + 2)z^{-1} + z^{-2}}|A_{\Phi_{rn}} \\ &= \frac{50MHz}{200kHz} \cdot 0.1976 \cdot 0.1367 \cdot 0.01 \\ &= 0.0675\end{aligned}$$

With formula (2), the fractional spur level is -29.43 dBc/Hz. The Bessel function also yields the same value. In addition, the observed value of θ_p is 0.068 in the simulation. It can be concluded that $-29.43\ dBc$ is the theoretical fractional spur level. It is closer to the simulation result -28.80 dBc. The 0.63 dB gap is due to the computational error of the spectrum calculation code. As a summary, the key difference between the two methods is how they get the relationship between DCO output jitter and DTC nonlinearity.

IV. DTC Gain Calibration

An LMS algorithm is chosen here to calibrate the DTC gain, K_{DTC}. It works by iteratively diminishing the correlation between an error signal (here: the phase error) and a forcing signal (here: PHR$_f$ being the accumulated FCW$_f$). When PVT changes, the DTC gain is no longer correct and so the phase error increases linearly in one cycle of the sweeping DTC control codes. Fig. 4 shows the scheme of the proposed DTC gain calibration. $(1 - \text{PHR}_f)$ is approximately linearly correlated with the noise n. $1/K_{DTC}$ is the coefficient needed to be updated. At its optimum point, $\hat{e}$ do not have the part correlated with $1 - PHR_F$. It is around zero at last. LMS algorithm makes DTC tracks the current transfer function by adjusting DTC gain.

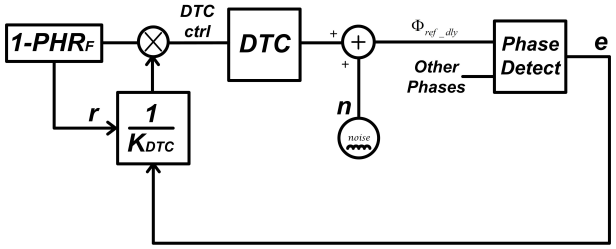

Fig. 4: Block diagram of DTC gain calibration.

As shown in Figure 5, the blue transfer function will at last tracks the black transfer function. The DTC gain has only one value to suppress the PVT variation, but not DTC nonlinearity, INL for example. The analysis proves that when DTC gain is tuned manually, the first spur can be suppressed while other spurs' level may go to even higher values.

For illustration simplicity, assume INL has a sinusoidal wave and is applied in Figure 5. LMS algorithm has to be improved. Divide the DTC control words into 4 equal parts. Each contains 8 control numbers. In each part, the correlation between the detected phase error and $1 - PHR_F$ still exists. What's more, there is another correlation relationship in each piece of the PHR_F, as described in [7]. That makes it practical to calibrate DTC gain with four segments. In Figure 5, 4 gain values are adaptively updated. As a result four lines tracks the sinusoidal curve, greatly reducing the phase error amplitude.

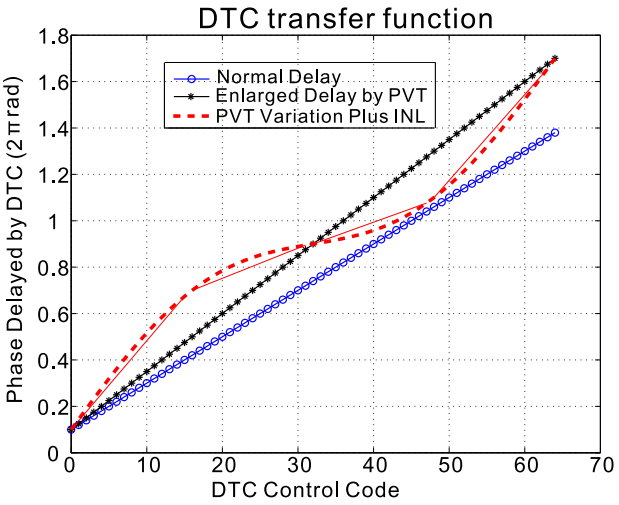

Fig. 5: DTC transfer function.

To illustrate the effectiveness of 3-points nonlinearity cancellation algorithm, Figure 7 is shown. The peak value of the nonlinearity applied is $0.1\,T_V$. It is so large that the spur level can be -16.86 dBc if one-value DTC gain calibration algorithm is used. When 3-points nonlinearity cancellation is used, the highest spur level is reduced to -42.03 dBc. 3 points means only when phrf=0.25, phrf=0.5, phrf=0.75 (along with phrf=0.0), the phase error is fed into the LMS algorithm. With more points, even lower spur level can be achieved. That means, with multiple gain values, the LMS can cancel the nonlinearity.

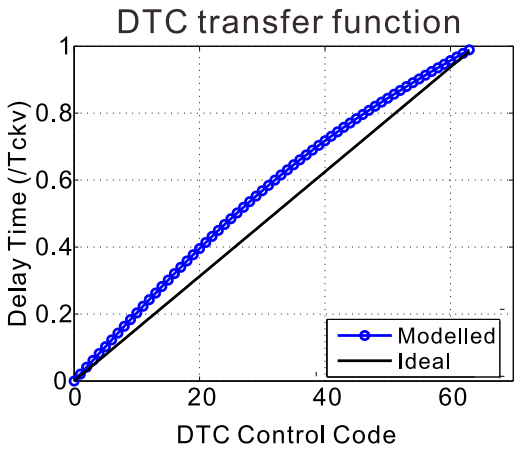

Fig. 6: DTC transfer function.

V. Conclusion

A pseudo phase-domain method is proposed to accurately estimate the level of fractional spurs that are due to the DTC nonlinearity. Being a scalar value, a wrong value of the DTC gain produces fractional spurs located at $min(f_R/FCW_f, f_R/(1-FCW_f))$ and its harmonic frequencies, even though the DTC might be perfectly linear. The induced phase error behaves like a sawtooth wave in the time domain. From the analysis, it can be concluded that to keep the fractional spur level below -38 dBc, DTC gain should be

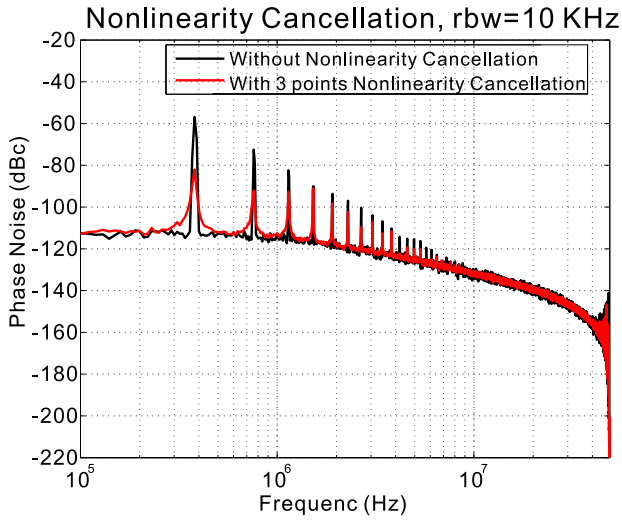

Fig. 7: Phase noise comparison with the 3-point nonlinearity cancellation.

calibrated within 1% error. To leave a margin, even smaller error is required. That highly sensitive characteristic drives the need to use multiple DTC gains. In this way, DTC nonlinearity is not a limitation of the DTC-counter-based ADPLL, because it can be digitally calibrated. With multiple values of DTC gain adopted in the adaptive algorithm, such as 3-point nonlinearity cancellation, fractional spurs can be suppressed by more than 20 dB without sacrificing the in-band noise floor level.

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