

A 60 GHz 25% Tuning Range Frequency Generator with Implicit Divider Based on Third Harmonic Extraction with 182 dBc/Hz FoM

Zhirui Zong¹, Masoud Babaie¹, and Robert Bogdan Staszewski^{1,2}

¹ Delft University of Technology, The Netherlands.

² University College Dublin, Ireland.

Abstract—A 60 GHz frequency generator with implicit $\div 3$ divider is proposed in this work to improve the system-level efficiency and phase noise. A third-harmonic boosting technique is utilized to simultaneously generate 20 GHz and sufficiently strong 60 GHz signals in order to avoid any divider operating at 60 GHz. The prototype is fabricated in 40 nm CMOS and exhibits a phase noise of -100 dBc/Hz at 1 MHz offset from 60 GHz carrier and 25% tuning range. The phase noise and FoM_T (figure-of-merit with tuning range) are improved by 5 dB and 4.6 dB, respectively, compared to state-of-the-art.

Index Terms—60 GHz, mm-wave, oscillator, harmonic boost, harmonic extraction, divider.

I. INTRODUCTION

High data-rate wireless communications at 60 GHz set stringent phase noise (PN) requirements on local oscillators (LOs). Furthermore, LOs require a wide tuning range (TR) to cover the specified frequency bands (e.g., 57–66 GHz) with margin for process, voltage and temperature (PVT) variations. Meanwhile, long battery lifetime calls for high power efficiency thus, ultimately, high figure-of-merit (FoM). Unfortunately, CMOS implementations of such 60 GHz LOs suffer from poor PN, limited TR and high power consumption.

Oscillators and high-frequency dividers are the key challenges in the 60 GHz PLL design. The traditional PLL architecture employs a 60 GHz oscillator, which feeds both a 60 GHz frequency divider back for a phase detection with a frequency reference clock, and a power amplifier (PA) to drive an antenna [1]. The oscillator PN is severely affected by a poor Q -factor of the resonant tank. The dividers are typically power hungry and occupy large silicon area, yet suffer from limited locking range. The frequency tripling PLL [2] relieves the aforementioned design challenges but shifts them to the injection locked frequency tripler (ILFT), so the solution-level issues remain. The common mode (CM) extraction PLL [3] traps the existing second harmonic at the CM node of the 30 GHz differential oscillator, and gets rid of the problematic frequency multipliers. Nevertheless, the required large CM swing dramatically increases the $1/f$ noise up-conversion. Also the conversion of single-ended CM signal to a differential output may introduce large phase error.

To alleviate the above design challenges of mm-wave oscillators and dividers with minimum impact on other

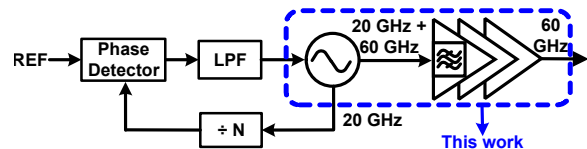


Fig. 1. A new PLL architecture with the proposed 60 GHz frequency generator.

circuitry, a 60 GHz LO with an implicit $\div 3$ divider is proposed in this work. Fig. 1 introduces a new PLL architecture that employs the proposed LO.

II. PROPOSED PLL ARCHITECTURE

The basic concept of the proposed idea is that the oscillator simultaneously generates the fundamental at 20 GHz and its 3rd harmonic at 60 GHz. The 60 GHz signal is feed forward to the buffer/PA, while the 20 GHz signal is fed back to the phase detector after further frequency division, as shown in Fig. 1. Consequently, the $\div 3$ functionality is inherent with the 60 GHz LO thus avoiding any physical divider operating at the 60 GHz carrier. This leads to a dramatic increase of the system-level efficiency.

However, the ~ 20 GHz fundamental harmonic must be suppressed at the PA output, hence a filtering function is needed on the feedforward path. Fortunately, mm-wave buffers and PAs are usually loaded by LC tanks, which are natural band-pass filters (BPF). Therefore, their natural BPF filtering is exploited here to reject the ~ 20 GHz fundamental frequency component.

III. THIRD HARMONIC BOOSTING TECHNIQUES

Third-harmonic techniques have been exploited in the past to lower the phase sensitivity to circuit noise in a class-F oscillator [4]. However, the 3rd harmonic of the generated voltage is relatively weak ($\sim 15\%$). Also, thick-oxide devices were used due to reliability concerns, but they limit the frequency TR so they should be avoided. In order to reduce the required gain of the following buffer, a much stronger 3rd harmonic is desired. This work proposes a harmonic-boosting technique for a transformer based dual-tank oscillator to significantly increase the voltage level of the 3rd harmonic.

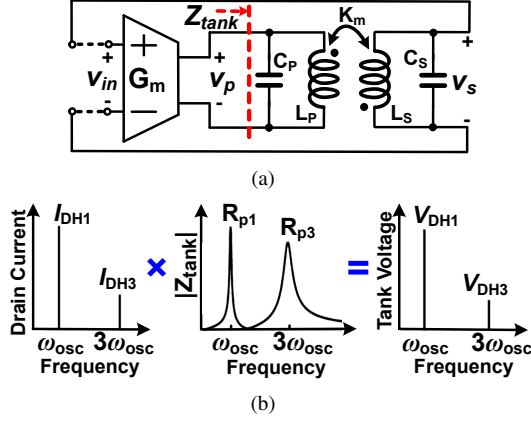


Fig. 2. (a): Simplified diagram and (b): operational principle of the proposed oscillator.

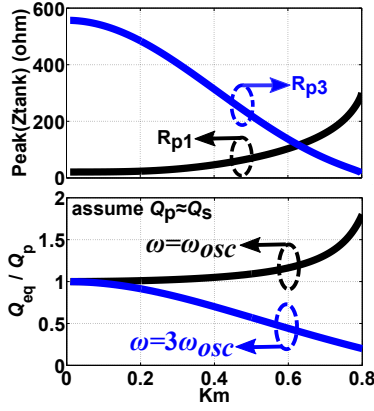


Fig. 3. Dependency of tank impedance and Q_{eq} on k_m .

A. Method and Trade-off in Increasing Third Harmonic

Fig. 2 shows the simplified diagram of the 3rd-harmonic tuned oscillator and explains its operational principle in frequency domain. To generate a stronger 3rd harmonic voltage, there are two possible options: increasing either I_{DH3}/I_{DH1} current or R_{p3}/R_{p1} impedance ratios. The I_{DH3}/I_{DH1} is typically fixed for a certain type of oscillator. Consequently, larger R_{p3}/R_{p1} is desired. On the other hand, high Q -factor at ω_{osc} is necessary for good PN performance, while low Q at $3\omega_{osc}$ is appreciated for tolerance to frequency misalignment between the second ($\sim 3\omega_{osc}$) and first resonances (ω_{osc}). Since it is a two-port dual-tank oscillator, its Q -factor is not so straightforward to estimate as in the traditional one-port LC resonators. The equivalent Q -factor (Q_{eq}) is derived from the phase response of the open-loop transfer function V_s/V_{in} .

Magnetic coupling coefficient, k_m , affects the tank impedance Z_{tank} and Q_{eq} . That relationship is shown in Fig. 3. R_{p1} decreases with smaller k_m , while R_{p3}

behaves opposite. Therefore, smaller k_m is desired for larger R_{p3}/R_{p1} , while larger k_m is required for the optimal Q_{eq} at ω_{osc} and $3\omega_{osc}$. As a trade-off, $k_m=0.61$ is chosen for $R_{p3}/R_{p1} > 1$ with the sufficient Q -factor.

B. Oscillation Mode Stability Analysis

Start-up conditions are examined to ensure that the oscillation can only happen at ~ 20 GHz, even if $R_{p3} > R_{p1}$. Barkhausen's phase and gain criteria should be satisfied for a stable oscillation. Analysis and simulations reveal that the open-loop phase response $\angle V_s/V_{in}=0^\circ$ at $\omega=\omega_{osc}$, while $\angle V_s/V_{in}=-180^\circ$ at $\omega=3\omega_{osc}$. Hence, the phase criterion can be satisfied only at the first resonant frequency (~ 20 GHz).

Moreover, the open-loop magnitude response of V_s/V_p is investigated. At ~ 20 GHz, the transformer tank exhibits a transfer gain of 2.2 (6.85 dB) from primary to secondary, while at ~ 60 GHz, it has a transfer attenuation of 0.24 (-12.40 dB). This property effectively cleans up the 3rd-harmonic component in the secondary winding.

IV. CIRCUIT IMPLEMENTATIONS

A. Third Harmonic Boosting Oscillator

Fig. 4 shows a schematic of the proposed 3rd-harmonic boosting oscillator. To mitigate the breakdown stress on the core transistors and avoid thick-oxide devices, a lower supply voltage ($V_{DD}=0.7$ V) is used. A 1:2 transformer of $k_m=0.61$ together with switched MOM-capacitor banks in the primary and secondary windings comprise the resonant tank. C_s provides coarse tuning, while C_p adjusts the second resonance close to $3\omega_{osc}$.

The simulated waveform reveals that the 3rd-harmonic, V_{DH3} , to fundamental, V_{DH1} , voltage ratio is $\sim 40\%$ at the drain nodes, while a clean waveform at fundamental frequency is restored at the gate nodes (see Fig. 5).

B. Output Buffer/Fundamental Harmonic Rejection Stage

A common-source amplifier with transformer loading is designed as the oscillator buffer stage, as highlighted in Fig. 6. Simulations show that the buffer stage can

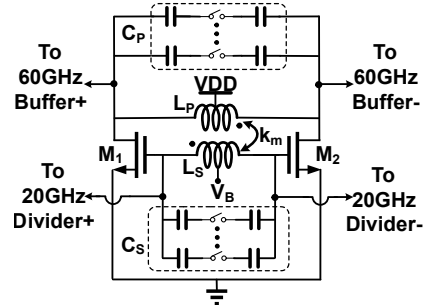


Fig. 4. Schematic of the 3rd-harmonic boosting oscillator.

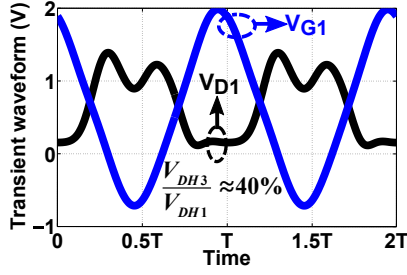


Fig. 5. Simulated oscillation waveforms at drain and gate nodes.

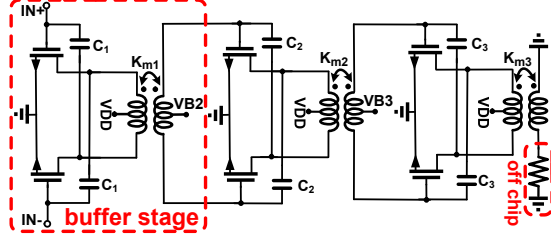


Fig. 6. Schematic of the 3-stage power amplifier.

provide fundamental-harmonic rejection ratio (HRR) of 14–25 dB across the frequency range of 50–66 GHz, while consuming 10.5 mA from 1 V supply. Over the 55–63 GHz range, the fundamental HRR is >19 dB, which is better than that of many ILFTs.

It is worthy to note that the good fundamental HRR is just a by-product of the buffer stage in this work. No extra cost (e.g., the gain) is paid to obtain such HRR.

Two extra amplifier stages are designed and added after the buffer stage to form a PA (see Fig. 6) for measuring purpose (to overcome the large loss in 60 GHz cables and probe, and conversion loss in the external test mixers). Neutralization capacitors (C_1 , C_2 and C_3) are added to improve the differential-mode stability factor. Similar to the buffer stage, each of the amplifier stages can provide a good HRR to further suppress the undesired fundamental tone at ~ 20 GHz at no extra cost.

V. EXPERIMENTAL RESULTS

A prototype of the proposed 60 GHz LO with the implicit $\div 3$ divider is fabricated in TSMC 1P7M 40-nm CMOS. The chip micrograph is shown in Fig. 7. An R&S FSUP50 signal source analyzer is used with an external mixer for PN measurements. Fig. 8 shows the measured PN at 57.8 GHz, while drawing 13.5 mW from a 0.7 V supply. At 1 MHz offset, the PN is -100.1 dBc/Hz, which is the best ever-reported.

To verify the suppression of the fundamental tone at ~ 20 GHz, the frequency spectrum is measured around the output carrier and also within 0–50 GHz, as shown in Fig. 9. The measured leakage of the ~ 20 GHz fundamental

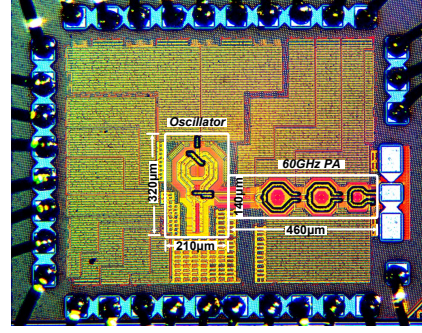


Fig. 7. Chip micrograph; the core area is 0.13 mm².

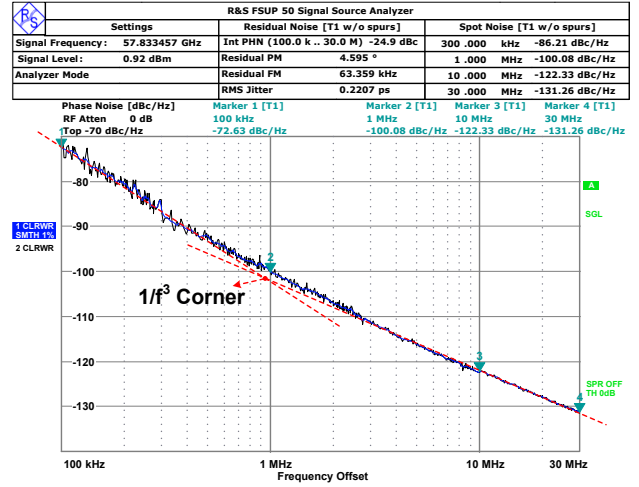


Fig. 8. Measured phase noise at 57.8 GHz.

is -55 dBm or -60.3 dBc. Due to the common-mode leakage from the oscillator and nonlinearity of the PA, the second harmonic at ~ 40 GHz is visible at -47 dBm or -52.3 dBc.

The TR is 25% from 48.4 to 62.5 GHz. Fig. 10 shows the PN at 1 MHz offset and the corresponding FoM across the TR. Note that the power consumption of the buffer stage (10.5 mW) is included in the FoM and FoM_T calculations. The PN varies between -98.8 and -100.1 dBc/Hz. The FoM has the worst value of 179 dBc/Hz at the lowest frequencies, and best value of 181.9 dBc/Hz at the highest frequencies. Since the switched capacitors have lower Q -factor in on-state, the FoM at lower frequencies decreases.

The 60 GHz PA delivers a maximum of +6 dBm power (after de-embedding the losses) to an external 50 Ω load, while consuming 58 mA from a 1 V supply.

The performance of the proposed LO is summarized and compared to state-of-the-art 60 GHz oscillators in Table I. The PN and FoM_T are the best, and advance the start-of-art by 5 dB and 4.6 dB at 1 MHz offset, respectively. The best FoM was reported in [5], but no power consumption

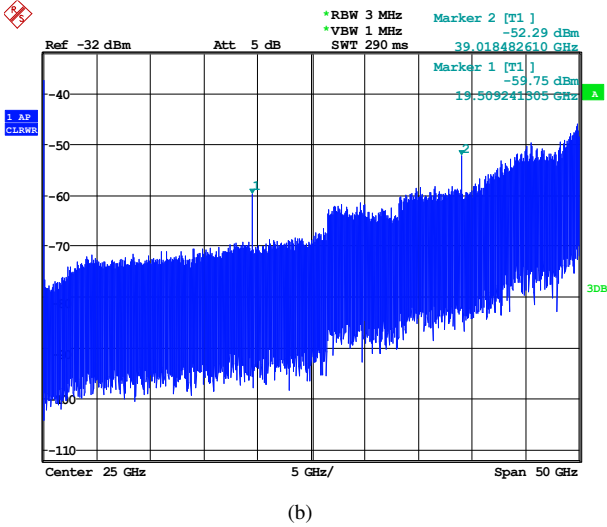
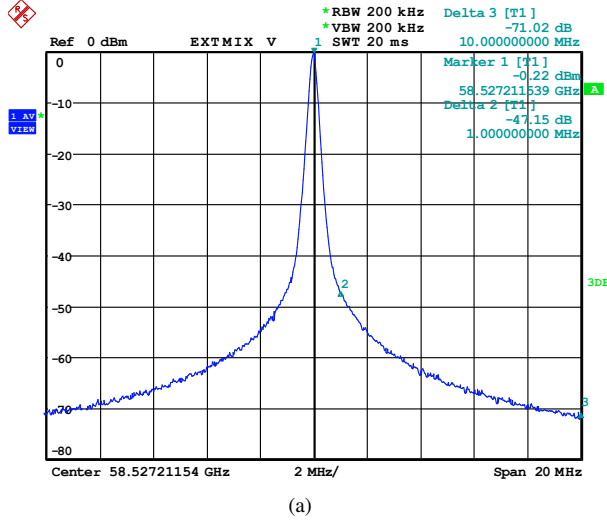


Fig. 9. Measured spectrum (a): at 57.8 GHz and (b): 0–50 GHz.

from the oscillator buffer stage was included in that FoM calculation.

VI. CONCLUSION

A novel 60 GHz frequency generator based on a 3rd harmonic extraction was proposed in this paper to improve the system-level efficiency and performance. A 3rd harmonic boosting technique is described to increase the 3rd harmonic at the oscillator output. The oscillator generates both ~ 20 GHz fundamental and a significant amount of the 3rd harmonic at ~ 60 GHz. Undesired fundamental harmonic at ~ 20 GHz is rejected by the good fundamental HRR inherent with the oscillator buffer stage, and ~ 60 GHz component was amplified to the output. Prototyped in 40 nm CMOS, the frequency generator advances the state-of-the-art phase noise performance and FoM_T by 5 dB and 4.6 dB, respectively. It is worthy to note

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-ART

	This work	[1]	[5]	[2]	[3]
CMOS (nm)	40	65	130	65	32 SOI
Type	HM extract	funda mental	funda mental	freq. tripling	CM extract
P _{DC} (mW)	Osc. 13.5 buffer 10.5	13.2	3.9	10.6+14*	42
V _{DD} (V)	0.7/1	1.2	1	1.2	1
TR (%)	25.4	11.6	10	11.5	22.4
PN dBc/Hz	1 MHz -100.1 10 MHz -122.3	-92	-95/-91	NA	-89
FoM dBc/Hz	1 MHz 181.5 10 MHz 183.7	176.4	185/181	NA	167.7
FoM _T dBc/Hz	1 MHz 189.6 10 MHz 191.8	177.7	185/181	NA	174.7

*:including the power consumption of the frequency tripler

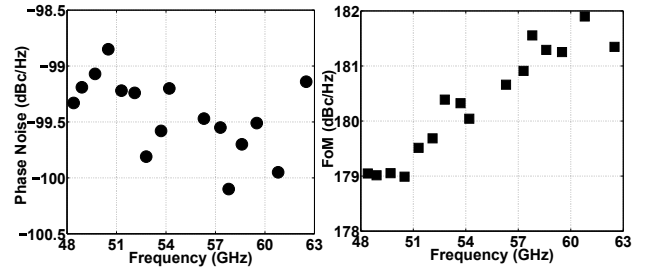


Fig. 10. Phase noise and FoM variation across the tuning range.

that the embedded $\div 3$ functionality will further improve the efficiency when used in the system.

ACKNOWLEDGMENT

We acknowledge TSMC university shuttle program for chip fabrication, Integrand Software for EMX license, and European ERC Grant 307624 for financial support.

REFERENCES

- [1] W. Wu, et al., "A 56.4–63.4 GHz spurious free all-digital fractional-N PLL in 65 nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 352–353, Feb. 2013.
- [2] T. Siriburanon, et al., "A 60-GHz Sub-Sampling Frequency Synthesizer Using Sub-harmonic Injection-Locked Quadrature Oscillators," *IEEE RFIC Symp.*, pp. 105–108, June 2014.
- [3] B. Sadhu, M. Ferriss, A. Valdes-Garcia, "A 46.4–58.1 GHz Frequency Synthesizer Featuring a 2nd Harmonic Extraction Technique that Preserve VCO Performance," *IEEE RFIC Symp.*, pp. 173–176, June 2014.
- [4] M. Babaie, R.B. Staszewski, "Third-harmonic Injection Technique Applied to a 5.87-to-7.56 GHz 65 nm CMOS Class-F Oscillator with 192 dBc/Hz FOM," *IEEE ISSCC Dig. Tech. Papers*, pp. 348–349, Feb. 2013.
- [5] J. Borremans, et al., "VCO design for 60 GHz using differential shielded inductors in 0.13 μ m CMOS," *IEEE RFIC Symp.*, pp. 135–138, 2008.