

# Design and Built-In Characterization of Digital-to-Time Converters for Ultra-Low Power ADPLLs

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**Abstract**—The newly proposed phase-prediction counter-based ADPLL has achieved a wireless standard-compliant performance at ultra-low power consumption. The digital-to-time converter (DTC) is the key enabler but its nonlinearity can easily create fractional spurs. This paper analyzes the effect of the DTC nonlinearity on in-band fractional spurs and proposes a method to characterize it in a built-in fashion by means of a fine-resolution  $\Delta\Sigma$  TDC that forms an outer loop with the DTC. The TDC is realized in 40nm CMOS and exhibits only 1.8ps rms of random jitter.

**Index Terms**—Fractional spurs, TDC, DTC, ADPLL.

## I. INTRODUCTION

As the CMOS technology scales, all digital PLLs (ADPLLs) become more and more popular due to their reconfigurability, lower area and power consumption. The first ADPLL for wireless applications [1] was counter-based, whose time-to-digital converter (TDC) had to cover merely one period of the variable DCO clock (CKV) rather than the full cycle of the frequency reference (FREF) clock, which is two orders-of-magnitude wider, as required by the conventional divider-based ADPLL topologies. To be able to further reduce power consumption of the TDC, which is the second most power hungry circuit after the DCO, the required TDC linear range was shortened in [2] by introducing a digital-to-time converter (DTC), whose purpose was to maximally align FREF with CKV. This way, the required TDC measurement range is greatly reduced to only a few inverter delays, which relaxes the TDC linearity specifications and significantly lowers its power.

This DTC-assisted ADPLL architecture [2], shown in Fig. 1, has broken through the critical 1mW barrier of a PLL for standard-compliant wireless applications, with DTC/TDC combination consuming merely 40 $\mu$ W. To put it into perspective: Previously, the TDC alone would consume several mW.

The resulting side effect, however, is that now the strict linearity requirements of the TDC have shifted to the DTC. It is well known that the phase detector nonlinearity (whether due to TDC or DTC) has a direct

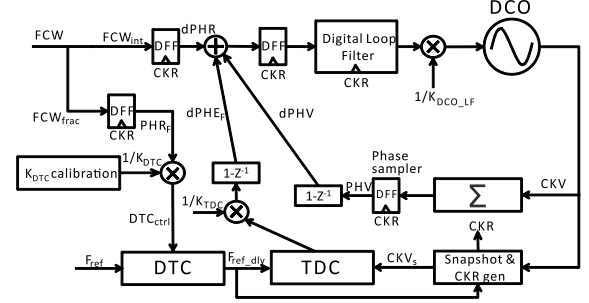


Fig. 1. DTC-counter-based ADPLL architecture.

impact on in-band fractional spurs. Also, the nonlinearity is inversely proportional to the device sizes, and smaller power consumption pushes designers to reduce the device size. Consequently, in the quest towards ultra-low power (ULP) radios, the DTC nonlinearity is now controlling the critical balance between the power consumption and in-band fractional spurs. The size of the DTC devices cannot be too large as that would unnecessarily increase the power consumption and it cannot be too small as that would produce excessively larger spurs.

It is therefore imperative to be able to design and characterize a DTC with optimized linearity and power consumption. Unfortunately, measuring the DTC transfer function with a sub-ps accuracy is utmost difficult. In this paper, we propose such characterization method with a built-in structure in 40nm CMOS forming a  $\Delta\Sigma$  TDC and verify it on two DTC designs.

## II. DTC NONLINEARITY INDUCED SPURS

Influence of the DTC nonlinearity on the counter-based ADPLL has not been much studied before. For the divider-based ADPLL, this kind of work was carried out in [3]. However, that TDC is made up of a bang-bang phase detector (BB-PD), which is a one-bit TDC. The BB-PD makes the loop bandwidth dependent on the thermal noise of the FREF path [4]. For the multi-bit TDC, which is the interest of this paper, the TDC transfer function gain is determined by the resolution of the TDC. This architecture

results in a more linear TDC transfer function than in the BB-PD.

In the DTC-counter-based ADPLL with multi-bit TDC, the DTC nonlinearity will modulate the phase error,  $\Phi_e$ , directly. This is different from the traditional counter-based ADPLL, where the TDC nonlinearity will affect the  $\Phi_e$  in a less direct way due to the random thermal noise that participates in the TDC detection process.

To quantize the influence of the DTC nonlinearity on fractional spurs, a special case of a sine-shaped nonlinearity can be assumed first. Its INL peak-to-peak value is denoted as  $INL_{pp}$ . The in-band spur level can be calculated from the following formula:

$$L = \frac{\pi^2}{4} \left( \frac{INL_{pp}}{T_{ckv}} \right)^2 \quad (1)$$

where,  $T_{ckv}$  denotes the period of the variable DCO clock, CKV. The spurs beyond the loop bandwidth will be attenuated by the ADPLL closed-loop transfer function. For practical INL curves, the suggested approach is to carry out the Fourier decomposition first and then calculate the spurs for all major harmonics.

The derivation of the above formula is explained as follows: The variance of timing uncertainty is  $\sigma_t^2 = \left( \frac{INL_{pp} \cdot T_{DTC}}{2\sqrt{2}} \right)^2$ . It is then normalized to the unit interval and multiplied by  $2\pi$  radians:  $\sigma_\phi = 2\pi \frac{\sigma_t}{T_V}$ . Then, it is divided by 2, to transfer the single-sided spectrum into double-sided. The fractional spur level is thus obtained. Since the practical DTC must be longer than  $T_{ckv}$ , only the active DTC units should be used to calculate the INL curve.

### III. FIRST-ORDER SIGMA-DELTA TDC DESIGN

Measurement of the DTC nonlinearity is extremely difficult due to the general unavailability of time-measurement equipment of sub-ps accuracy. Furthermore, bringing the internal signals, such as  $FREF_{dly}$ , to the outside of the IC chip will deteriorate their internal rail-to-rail transition times of  $\sim 20$  ps by at least one or two orders of magnitude. Since the information sought is in the transition timestamps, slowing down the signal edges will proportionately increase jitter, especially given noisy off-chip environment. Consequently, a built-in characterization circuitry must be employed for accurate measurements of the DTC nonlinearity.

In an analogy to characterizing a DAC using a fine-precision ADC, to be able to measure the DTC nonlinearity, a TDC of much higher resolution is required. Inspired by a  $\Delta\Sigma$  pulse-width digitizer architecture [5], a first-order  $\Delta\Sigma$  architecture is proposed in this paper to realize a fine-resolution TDC that would precisely measure the DTC's transfer function. The TDC, shown in Fig. 2, encompasses the two DTCs under test, and further consists

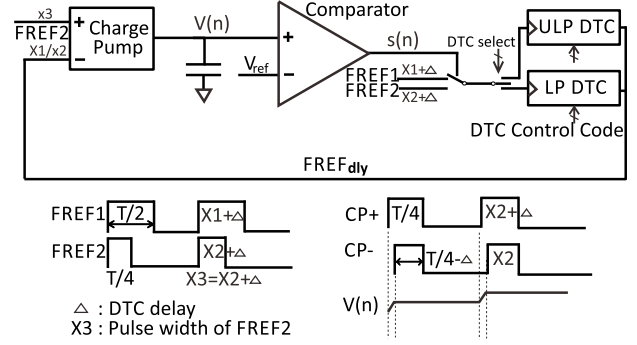


Fig. 2. Sigma-delta TDC architecture.

of a charge pump, integrating capacitor, comparator and digital logic.

The charge pump is controlled by two signals. The first signal,  $FREF2$ , has a duty cycle of 25% and constantly charges the capacitor. The second signal discharges the capacitor with a variable duty cycle from 0 to 50%, and comes from an output of the selected DTCs under test. Due to the existence of a pole, when the loop is stable, the average current of the charge pump integrating on the capacitor must be zero. Hence, the capacitor voltage must hover above and below a certain fixed voltage level, which is established by the reference voltage  $V_{ref}$  of the following comparator. That above/below 1-bit information stream  $s(n)$  provided by the comparator is fed into a moving-average (MA) decimation filter. Such an MA filter appears sufficient and keeps the hardware complexity low.

The Fig.2 structure is somewhat similar to the traditional  $\Delta\Sigma$  ADC where the integrating capacitor voltage is quantized by the comparator (one-bit ADC). Selector and DTC here act as a one-bit DAC. The DTC output is subtracted in the charge pump. Hence, an alternating pattern of 0's and 1's will appear at the comparator output.  $FREF1$  and  $FREF2$  are generated by a common high-frequency signal of  $4\times$  frequency.

Even though this architecture is used to obtain the transfer function of an embedded DTC, it should be noted that it can be adapted as a fine-resolution TDC to measure time delay between  $FREF1$  and  $FREF2$ .

#### A. DTC Circuit Design

The DTC adopts an identical ULP topology as in [2] and comprises a string of 64 units of bypass/delay. The schematic of a single unit is shown in Fig. 3. The input from the previous unit is  $D_{in}$  and the output is  $D_{out}$ . The  $FREF$  clock is simultaneously distributed to all 64 units. Each unit comprises two parts: the selection set to establish the starting point of the  $FREF$  propagation path and an output-enabled buffer to produce delay equivalent to two inverters.

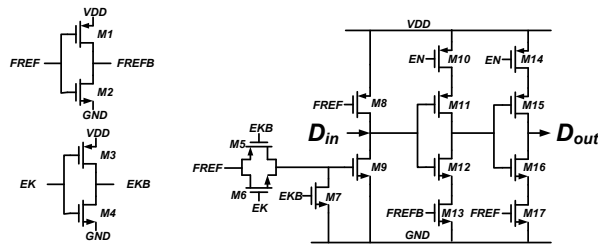


Fig. 3. Schematic of a single DTC unit. 64 of such units are connected in a string.

Transistors M5, M6 and M7 form a transmission-gate based logic AND gate, which consumes less power than the conventional topology. M8 and M9 act as an inverter when this stage's selection set is chosen. Otherwise,  $D_{in}$  sees high impedance. This inverter and the logic AND form the selection set. M10 and M14 of the output-enabled buffer are enabled by the digital input code EN. When EN=0, the input signal propagates through this buffer. M13 and M17 are controlled by the input signal to save power. After the first inverter in the selection set, the signal's rising edge becomes a falling edge. For those buffers, it is the falling edge that matters. Therefore M10, M11, M16 and M17 are oversized to decrease the delay time of the falling edge.

### B. Charge Pump Design

The charge pump acts as a phase-to-current converter, which converts the phase difference between FREF1 and FREF2 to the output current, which is then accumulated on the load capacitor, whose voltage is to be fed into the 1-bit quantizer. The information at the input of the charge pump is in the phase domain. Then it converts into the current domain during the  $\Delta$  action. By integrating the current, the information shifts from current domain to voltage domain during the  $\Sigma$  action.

Figure 4 is the schematic of a single-ended charge pump. Bias current flows into M1, while M2–M5 act as current mirrors. M6/M7 and M8/M9 are input ports of the charging and discharging clocks, respectively. When the charge pump is charging, M7 and M8 are enabled and M6 and M9 are disabled. Current from M5 flows through M7 and then go to the load. M11 and M12 serve as dummy loads to bias both output branches of the charge pump to a similar voltage. This current steering topology features a better supply rejection than the current switching topology. M13–M16 provide controllable offset currents for characterization purposes.

The charging and discharging mismatch dominates the accuracy of the measured DTC delay by adding a systematic error. However, it can be de-embedded as demonstrated in Sec. IV.

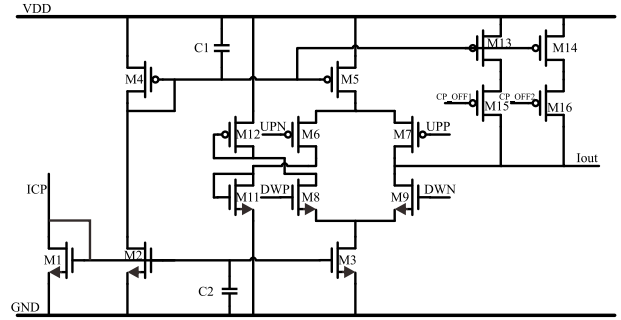


Fig. 4. Charge pump schematic.

### C. Comparator Design

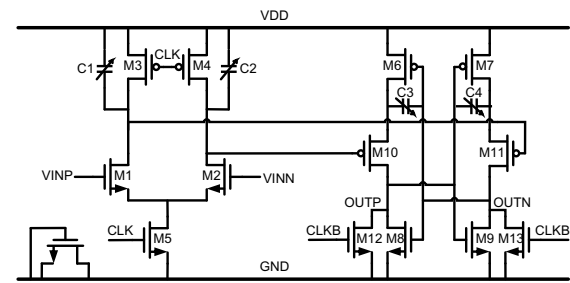


Fig. 5. Comparator schematic.

Figure 5 shows the comparator circuit, which is a typical two-stage architecture. The first stage is a pre-amplifier, consisting of M1–M5. The second stage is a latch. To get a better isolation of the noise from the previous component, the comparator acts an extra delay. C1–C4 are used to enhance its phase noise performance.

The input-referred noise is  $\sim 1$  LSB in a 12-bit mode, which is around 0.25 mV when the supply voltage is 1 V. This value is consistent with simulations, 0.28 mV. By simulation, it is found that with the charge pump output voltage swing around 30 mV, the input-referred noise contributes to about 2 ps measurement error of the DTC delay, which is the chief thermal noise contributor later verified through measurements.

## IV. MEASUREMENT RESULTS

The chip micrograph of the two DTCs and the surrounding TDC circuitry for built-in self characterization (BISC) is shown in Fig. 6. The core TDC circuitry occupies only 0.08 mm<sup>2</sup>. The measured DTC nonlinearity is shown in Fig. 7. The micrograph and plots clearly reveal that the DTC optimized for linearity (“LP-DTC”) is larger than the DTC optimized for power consumption (“ULP-DTC”). Consequently, the LP-DTC exhibits much better DNL than does the ULP-DTC. However, the raw data indicates that the INL improves by a much smaller amount. This

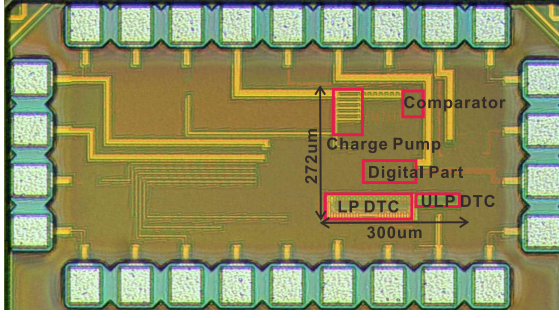


Fig. 6. Die micrograph (TSMC 40 nm,  $980 \times 530 \mu\text{m}^2$ ).

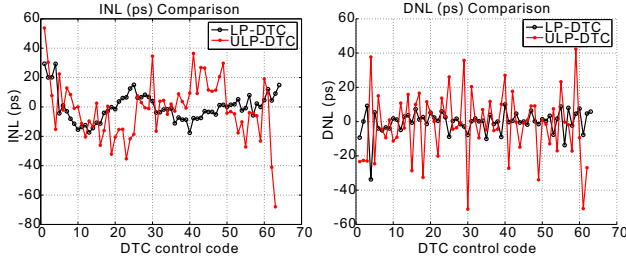


Fig. 7. Measured linearity of two DTCs: (a) INL; and (b) DNL.

could be explained by a systematic error in the TDC circuitry, which is common to both DTCs. To investigate it further, we first recognize that the x-axis in Fig. 7(a) (i.e., INL-vs-DTC-code) needs to be normalized to the physical time, which is shown in Fig. 8(a) (i.e., INL-vs-DTC-delay). Now, both the INL curves reveal the same “low-frequency” pattern of the systematic error, which is fit into a 3<sup>rd</sup>-order Fourier series, and then subtracted from both DTCs and plotted in Fig. 8(b) to confirm better INL linearity of the LP-DTC.

The next set of measurements deal with random noise, which mainly comes from input-referred noise of the comparator, jitter of the generated input clocks (FREF1, FREF2), supply noise coupled to the charge pump and voltage divider. The LP-DTC INL data is taken multiple times, boxplot of which is shown in Fig. 9(a). It can be seen that most data are covered within a 5 ps box. The

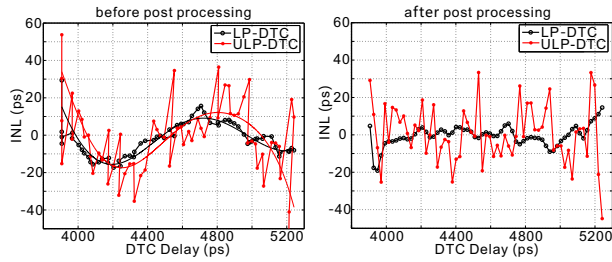


Fig. 8. Measured INL of two DTCs in which x-axis is DTC delay: (a) before post-processing; and (b) after post-processing.

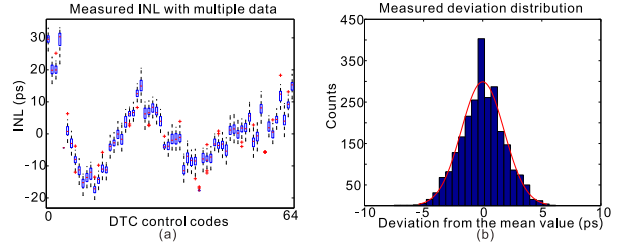


Fig. 9. Measured deviation caused by random noise: (a) box plot; (b) histogram with normalized distribution.

histogram of the INL deviation data is shown in Fig. 9(b). It is normal distributed with a standard deviation of 1.8 ps. Similar results are obtained for the ULP-DTC, which indicate that the noise is mainly due to sources outside of the DTCs. This single-shot data can be further reduced by averaging. Excluding the systematic error which could be easily subtracted, the  $\Delta\Sigma$  TDC achieves a very high resolution.

## V. CONCLUSIONS

To be able to characterize a linearity improvement of an ultra-low power (ULP) digital-to-time converter (DTC), a  $\Delta\Sigma$  time-to-digital converter (TDC) outer loop is created on top of two DTCs to their perform built-in self characterization (BISC). The entire circuitry is fully integrated in 40 nm CMOS die thus avoiding any issues with off-chip noise and transition time degradation. The resulting  $\Delta\Sigma$  TDC achieves fine resolution limited only by the 1.8 ps rms random jitter.

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