A Fully Integrated 28nm Bluetooth Low-Energy Transmitter with 36% System Efficiency at 3dBm

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***Abstract*—We propose a new transmitter (TX) architecture for ultra-low power radios. An all-digital PLL employs a digitally controlled oscillator with switching current sources to reduce supply voltage and power without sacrificing its phase noise and startup margins. It also reduces 1/f noise allowing the ADPLL, after settling, to reduce its sampling rate or shut it off entirely during direct DCO data modulation. The switching power amplifier integrates its matching network while operating in class-E/F_2 to maximally enhance its efficiency. The transmitter is realized in 28nm CMOS and satisfies all metal density and other manufacturing rules. It consumes 3.6 mW/5.5 mW while delivering 0 dBm/3 dBm RF power in Bluetooth Low-Energy.**

I. Introduction

Ultra-low power (ULP) transmitters are key subsystems for wireless sensor networks and internet-of-things (IoT). However, the system lifetime is severely limited by their power consumption and available battery technology. Energy harvesting can enable further applications but provides lower supply voltages (on-chip solar cells: 0.2–0.8V) than deep-nanoscale CMOS supply of 1 V. Although dc-dc converters can boost the voltage, their poor efficiency ($\leq$80%) introduces significant power penalty. Hence, the following new techniques are exploited in this work to enhance the ULP transmitter (TX) efficiency: First, the most power-hungry circuitry, such as digitally controlled oscillator (DCO) and output stage of power amplifier (PA), can operate directly at low voltage of harvesters. Second, a new switching current source oscillator optimized for 28 nm CMOS reduces power and supply voltage without compromising the robustness of the oscillator start-up or loading its tank quality factor. Third, thanks to the low wander (i.e, low flicker noise) of the DCO, digital power consumption of the rest of all-digital PLL (ADPLL) is saved by scaling the rate of sampling clock to the point of its complete shut-down. Last, a fully integrated differential class-E/F_2 switching PA is utilized to optimize high power added efficiency (PAE) at low output power of 0–3 dBm.

II. Switching Current Source Oscillator

The phase noise (PN) specifications are quite trivial for IoT applications and can be easily met by LC oscillators as long as the Barkhausen start-up criterion is satisfied over process, voltage and temperature (PVT) variations. Consequently, reducing DCO's power consumption (P_{DCO}) is the ultimate goal of IoT applications. The P_{DCO} can be calculated by [1]

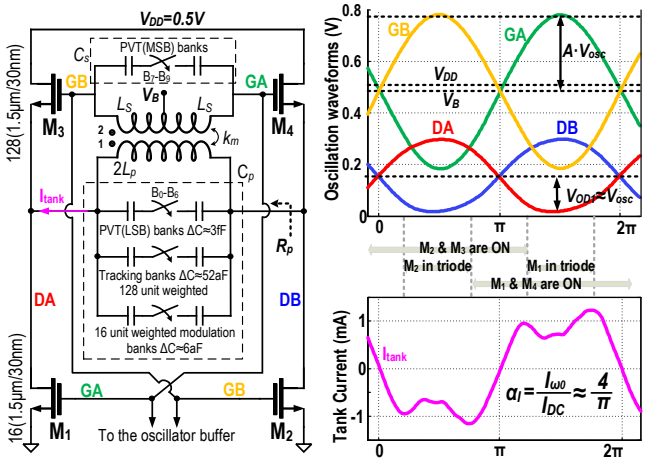

Fig. 1. Schematic and waveforms of the proposed oscillator.

$$P_{DCO} = V_{DD}^2 \cdot \frac{\alpha_V}{\alpha_I} \cdot \frac{1}{R_p}. \quad (1)$$

where, R_p is an equivalent input parallel resistance of the tank modeling its losses; α_I is the current efficiency, defined as ratio of the fundamental component of tank's current I_{ω_0} over the oscillator DC current I_{DC}; and α_V is the voltage efficiency, defined as ratio of the drain oscillation amplitude V_{osc} (single-ended) over the supply voltage V_{DD}.

Lower P_{DCO} is typically addressed by scaling up R_p=$L_p\omega_0 Q_t$ simply via a large multi-turn inductor [2]. However, (1) indicates that topology parameters such as oscillator's α_I and minimum supply voltage (V_{DDmin}) can also play an important role in the minimum achievable P_{DC}. Fig. 1 illustrates the proposed oscillator that combines best features of the traditional cross-coupled NMOS oscillator (i.e., low V_{DD}) and the complementary push-pull oscillator (i.e., high α_I) from the ULP standpoint. As can be gathered from Fig. 1, oscillation voltage at G_B is high within the first half-period. Hence, only M_2 and M_3 transistors are on and the current flows from left to right side of the tank's primary inductor $2L_p$. However, M_1 and M_4 are turned on for the second half-period and tank's current direction is reversed. Consequently, like in the push-pull structure, the tank current flow is reversed every half-period thus doubling the oscillator's α_I to 4/π.

The minimum V_{DD} is determined by the bias voltage V_B= V_{OD1} + V_{gs3}. Hence, $M_{3,4}$ should work in weak-inversion keeping $V_{gs3} < V_t$ to achieve lower V_{DDmin}. Since M_{1-4}

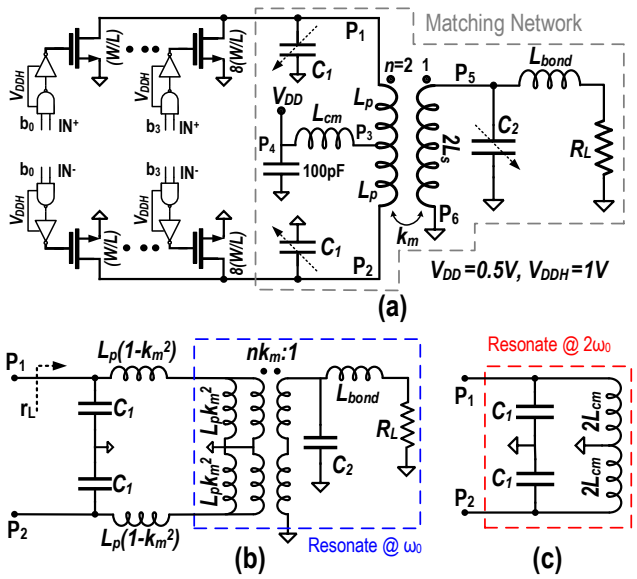

Fig. 2. (a) Class-E/F$_2$ switching PA. PA's matching network equivalent circuit for (b) differential, and (c) common-mode excitations.

TABLE I
$F_C{\cdot}F_I^2$ FOR DIFFERENT FLAVORS OF CLASS-E/F PA

	E	E/F$_2$	E/F$_3$	E/F$_{2,3}$	E/F$_4$	E/F$_{2,4}$	E/F$_{3,4}$	E/F$_5$
$F_C{\cdot}F_I^2$	7.44	2.47	7.25	4.99	5.88	2.06	5.06	7.35

have the same DC gate voltage, M$_{3,4}$ sub-threshold operation also provides enough V_{OD} overdrive for the switching current source devices M$_{1,2}$ to operate in the saturation region at the DC operating point. Hence, unlike traditional oscillators, the dimension of M$_{3,4}$ devices must be a few times (i.e., 8×) larger than current source devices to guarantee their weak-inversion operation. Furthermore, the oscillation swing cannot go further than $V_{OD1,2}$ at DA/DB nodes, which is chosen ~150 mV to satisfy the system's phase noise spec by a few dB margin. Consequently, as with cross-coupled NMOS oscillator, the proposed structure can operate at V_{DD} as low as 0.5 V.

The transformer voltage gain (A) enhances the oscillation swing at M$_{1-4}$ gates to even $>V_{DD}$ and guarantees the start-up over PVT variations. Furthermore, the combination of A and the effective trans-conductance gain of M$_{1-4}$ must compensate the tank losses. Hence, the contribution of M$_{1-4}$ to the oscillator PN reduces by A, which compensates the effect of lower voltage efficiency (α_V) of this structure on the oscillator PN and FoM.

Larger tank input impedance, R_p is also beneficial to reduce the oscillator's power consumption. R_p reaches its maximum when L_sC_s/L_pC_p=1 for $Q_p \approx Q_s$. Hence, the PVT tuning capacitors are divided in the transformer's primary and secondary to roughly satisfy this criterion.

Switching the bias of M$_{1-4}$ devices reduces both their 1/f noise and also the DC component of their effective ISF function. Consequently, a much lower 1/f^3 PN corner is expected than in the traditional oscillators [1].

III. Class-E/F$_2$ Power Amplifier

Designing a fully integrated PA optimized for low output power (P_{out} < 3 dBm) with PAE > 40% is very challenging, especially when differential structure is needed to satisfy

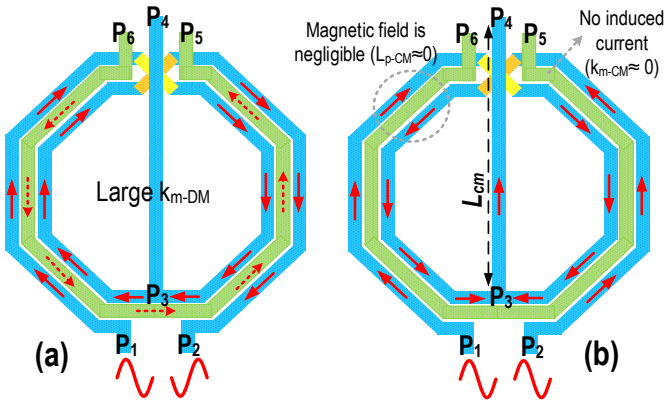

Fig. 3. Behavior of 2:1 step-down transformer in (a) differential-mode, and (b) common-mode excitations.

the stringent 2$^{\text{nd}}$ harmonic emissions. To realize such a low P_{out}, one needs to employ a matching network with a large impedance transformation ratio (ITR) to *increase* the load resistance, r_L, seen by the PA transistor drains of Fig. 2.

$$\text{ITR} = r_L/R_L = 0.5 \cdot n^2 \cdot k_m^2 \tag{2}$$

Unfortunately, the differential structure and imperfect magnetic coupling factor k_m of the matching network's transformer exhibit reverse effect of *reducing* r_L and thus ITR. Hence, the transformer turns ratio (n:1) should be large n>4 to compensate for them. However, Q-factor of transformer windings, and thus its efficiency, drops dramatically with n>2. Consequently, the PAE of published integrated PAs is relatively low (< 30%) or off-chip components are used in their matching networks [2]-[6].

The drain efficiency η_D of class-E/F switch-mode PA can be calculated by [7]

$$\eta_D = \frac{(C_{out}/C_1)}{(C_{out}/C_1) + F_C F_I^2 R_{on} C_{out}\,\omega_0}. \tag{3}$$

where, C_1 is PA's required shunt capacitance to satisfy class-E/F zero-voltage and zero-slope (ZVS) switching [8]. R_{on} and C_{out} are, respectively, on-state channel resistance and output capacitance of M$_1$ transistor. Note that $R_{on}\times C_{out}$ is a constant at a given technology and invariant to changes of M$_1$'s width. F_I is defined as ratio of RMS over DC values of M$_1$ drain current. F_C is the PA waveform factor. Both F_I and F_C are merely a function of matching network strategy and do not change over technology or PVT variations [8].

A smaller P_{out} can also be realized by using a lower V_{DD} for the PA's drains (e.g., 0.5 V) without any degradation of η_D, as gathered from (3). As a consequence, the required ITR will be smaller, which results in better efficiency of PA's output matching network. Furthermore, the drain voltage of the switching transistor is also limited to ≤1.5 V, alleviating reliability issues due to gate-oxide breakdown [9]. Eq. (3) also indicates that the switching amplifiers with smaller $F_C{\cdot}F_I^2$ (see Table I) inherently demonstrate higher efficiency. For example, class-E PA efficiency can be improved by realizing an additional open circuit as the PA switches' effective load at 2$^{\text{nd}}$ harmonic $2\omega_0$ (i.e., class-E/F$_2$ operation). Furthermore, class-E/F$_2$ shows a better tolerance to C_{out} variations [7] due to the role of 2$^{\text{nd}}$ harmonic tuning in smoothing the drain voltage waveform [8]. These benefits come at the expense of

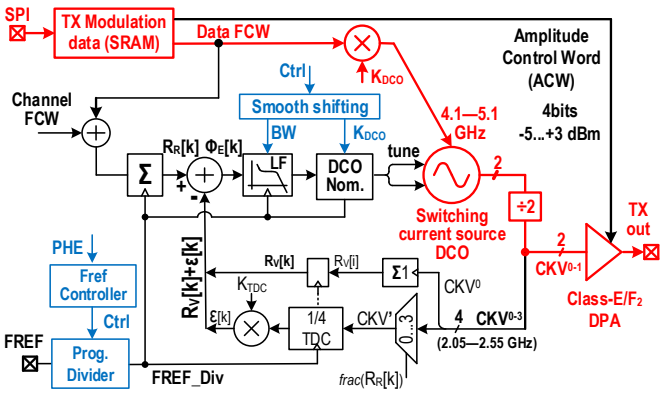

Fig. 4. Block diagram of the 2.4 GHz ULP Bluetooth low-energy transmitter.

$\sim 3\times$ lower power gain for PA transistors compared to that in the conventional class-E setup. However, the power gain of 28 nm NMOS devices is high enough at relatively low frequency of 2.4 GHz such that a 4.5 dB power gain penalty has a negligible effect on the total system efficiency.

Fig. 2(b) shows the equivalent circuit of the PA matching network in the differential mode. The transformer's secondary inductance $2L_s$ and capacitor C_2 resonate at ω_0 to optimize the matching network efficiency. Furthermore, the transformer's leakage inductance $L_p(1-k_m^2)$ and primary capacitor C_1 respectively realize the required series inductance and shunt capacitance of a class-E/F PA to satisfy its ZVS switching criteria.

As illustrated in Fig. 3, the step-down 2:1 transformer acts differently to the common-mode (CM) and differential-mode (DM) input signals. When the transformer's primary is excited by a CM signal at $2\omega_0$ [Fig. 3(b)], the magnetic flux excited within two turns of the primary winding cancels itself out. Consequently, the transformer's primary inductance is negligible and no current is induced at the transformer's secondary ($k_{m-CM} \approx 0$). Hence, R_L, L_s and C_2 cannot be seen by the $2\omega_0$ component of drain current. Furthermore, CM inductance seen by PA transistors is mainly determined by the dimension of the trace between the transformer center-tap and decoupling capacitors at the V_{DD} node, which roughly must resonate with C_1 at $2\omega_0$ to realize the class-E/F$_2$ operation (see Fig. 2 (c)).

IV. All-Digital Phase-Locked Loop Architecture

Fig. 4 shows a block diagram of the proposed ultra-low power (ULP) all-digital PLL (ADPLL) adapted from a high-performance cellular 4G ADPLL [10]. The $\sim$2.45 GHz $\div 2$ divider output of 4 phases, CKV$^{0-3}$, oversamples the frequency reference (FREF: 1–50MHz) generating CKR$^{0-3}$ vector clock to sample the variable DCO phase Rv[k] to calculate the phase error, $\phi_E[k]$. To avoid metastability in FREF retiming, FREF is simultaneously oversampled by different phases of CKV and an edge selection signal chooses the path farther away from metastability. The $\phi_E[k]$ is fed to the type-II loop filter (LF) with 4th order IIR. The LF is dynamically switched during frequency acquisition to minimize the settling time while keeping the phase noise (PN) at optimum. The built-in DCO gain, K_{DCO}, and TDC gain, K_{TDC}, calibrations are autonomously performed to ensure the wideband FM response.

The long string of 417 ps/7 ps >60 inverters is shortened 4x by running the DCO at 2x the carrier frequency and dividing its output by 2 to create a CKV clock vector, CKV$^{0\ldots3}$. A phase predictor ensures the TDC input CKV' is $< T_V/4$ by selecting a CKV phase that is closest to FREF. The TDC output, after decoding, is normalized to T_V by the Δ_{TDC}/T_V multiplier and the octal estimation, normalized to $T_V/4$, is added to produce the phase error ϕ_E. The DCO tuning word is updated based on ϕ_E.

The following architectural innovations allow the ADPLL to support ULP operation (highlighted in blue): The effective sampling rate of the phase detector and its related DCO update is dynamically controlled by scaling-down the frequency reference (FREF) clock and simultaneously adjusting the loop gain. During ADPLL settling, the full FREF rate is used, but afterwards its rate could get substantially reduced (e.g., 8x), thus saving power consumption of the digital circuitry. The resulting in-band PN degradation is tolerable due to low PN of the DCO. In fact, freezing FREF would incur sufficiently low frequency drift during Bluetooth 625μs packets, while keeping in operation the bare minimum of circuitry highlighted in red.

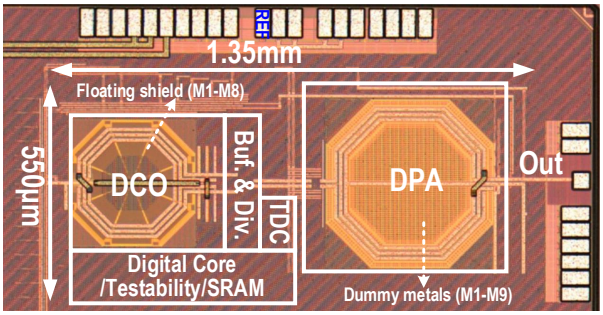

Fig. 5. Die micrograph of the proposed ULP transmitter.

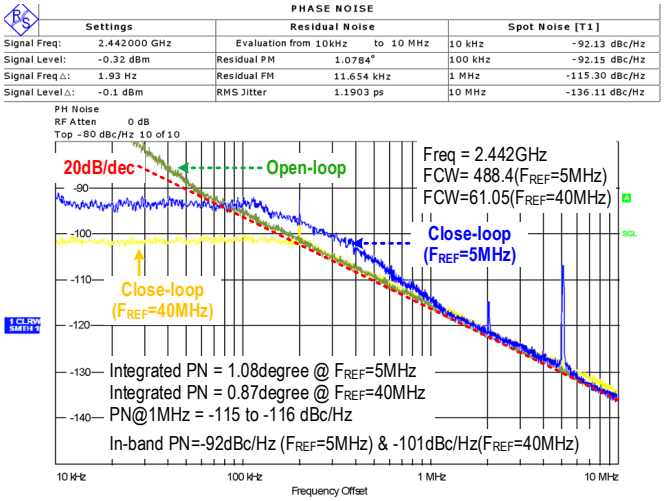

Fig. 6. Transmitter phase noise in open-loop and different close-loop configurations.

V. Measurement Results

Fig. 5 shows the die photo of the 0.75mm^2 ULP TX in TSMC 1P9M 28nm CMOS. Both DCO and PA transformer's windings are realized with top ultra-thick metal. However, they include a lot of dummy metal pieces on *all* metal layers (M1–M9) to satisfy very strict minimum metal density manufacturing rule of advanced ($\leq$28 nm) technology nodes.

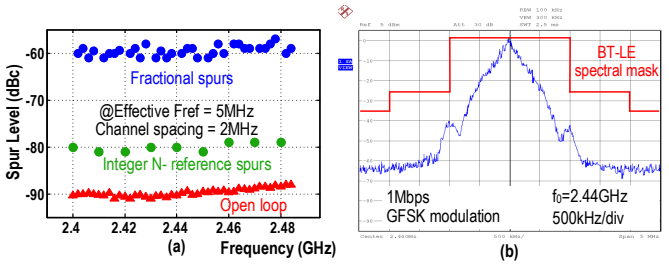

Fig. 7. (a) ADPLL fractional, reference and open-loop spurs; (b) Bluetooth GFSK modulation spectrum.

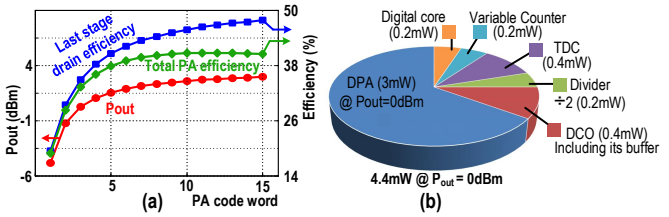

Fig. 8. (a) PA characteristics; (b) TX power breakdown at P_{out}=0 dBm.

Fig. 6 displays the phase noise plot of the proposed transmitter at different configurations. The measured DCO PN is -116 dBc/Hz at 1 MHz offset from 2.442 GHz carrier (green line in Fig. 6) while consuming 0.4 mW from 0.5 V power supply. Thanks to the switching current source technique, $1/f^3$ PN corner of the oscillator is extremely low (i.e.$\leq$100 kHz) across the tuning range (TR). The oscillator has a 22% TR, from 4.1-to-5.1 GHz. its average FoM is 188 dBc and varies $\sim$1 dB across the TR. As expected, the DCO also shows very low supply frequency pushing of 10-12 MHz/V, thus making it suitable for direct connection to solar cells and integration with PA.

When used as LO at *undivided* 40 MHz FREF, the ADPLL consumes 1.4 mW. It settles in 20 μs, and exhibits in-band PN of -101 dBc/Hz with integrated PN of 0.87°, as shown by yellow line in Fig. 6. Thanks to the low wander of the DCO, digital power consumption of the rest of ADPLL can be saved by scaling the rate of sampling clock to 5 MHz. However, the in-band PN increases to -92 dBc/Hz with integrated PN of 1.08^o (blue line in Fig. 6). The reference spur is -80 dBc and the worst-case fractional spur is -60 dBc at BT-LE channels as shown in Fig. 7 (a). Fig. 7 (b) shows Bluetooth-LE 1 Mb/s GFSK modulation provided by the ADPLL, while fulfilling all spectrum mask requirements with sufficient margin.

PA output level is adjustable between -5 to +3 dBm and reaches excellent peak PAE of 41% (see Fig. 8 (a)). The proposed TX consumes 3.6/5.5 mW during the open-loop 1 Mb/s GFSK BT-LE modulation at 0/3 dBm output, resulting in η_{TX}=28/36% total TX efficiency. The power consumption would increase by 0.8 mW with TDC, variable counter and digital circuitry turned on when the ADPLL is clocked at 40 MHz FREF. Thus, even in closed loop, with η_{TX}=23/32% at 0/3dBm it is still 1.5x better than the prior record. The TX power breakdown is also illustrated in Fig. 8 (b).

Table II summarizes the performance and compares it with leading ULP transmitters. The proposed ULP TX achieves the lowest power consumption and PN.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART.

	This work			ISSCC'13 IMEC [2]	ISSCC'12 Toumaz[3]	ESSCIRC'14 Frontier[4]	ISSCC'15 Dialog[5]	ISSCC'15 Renesas[6]
CMOS technology	28nm			90nm	130nm	65nm	55nm	40nm
OSC PN @1MHz (dBc/Hz)	-116			-111	-107	-108.2	N/A	N/A
OSC FoM (dB)	188			183	N/A	N/A	N/A	N/A
PLL in-band PN (dBc/Hz)	-92 @ FREF=5MHz			-85	-87	-87.5	N/A	N/A
	-101@ FREF=40MHz							
Integrated PN (degree)	1.08 @ FREF=5MHz			2.3	N/A	N/A	N/A	N/A
	0.87 @ FREF=40MHz							
Output power (dBm)	-5 to +3			-23 to -1	-30 to +5	-10 to -3	-20 to 0	0
Maximum PA PAE	41%			25%	N/A	<25%	<25%	<25%
On-chip matching network	Yes			No	No	No	Yes	Yes
Supply voltage (V)	0.5 / 1			1.2	1	1.1	0.9-3.3	1.1
Power consumption (mW)	@P_{OUT}	0dBm	3dBm	-1dBm	0dBm	-3dBm	0dBm	0dBm
	open-loop	3.6	5.5	5.4	8.9	5.1	10.1	7.7
	close-loop	4.4	6.3					
TX efficiency (P_{OUT}/P_{DC})	open-loop	28%	36%	15%	12%	10%	10%	13%
	close-loop	23%	32%					

VI. Conclusion

We have proposed an ultra-low power Bluetooth LE transmitter that demonstrates the best ever reported power efficiency and phase purity, while abiding by the strict 28 nm CMOS technology manufacturing rules. A new switching current source oscillator combines advantages of low supply voltage of the conventional NMOS cross-coupled oscillator with high current efficiency of the complementary push-pull oscillator to reduce the oscillator supply voltage and dissipated power further than practically possible in the traditional oscillators. Furthermore, due to the low wander of DCO, digital power consumption of ADPLL was saved by scaling the rate of sampling clock to the point of its complete shut-down. A fully integrated differential class-E/F_2 switching PA is utilized to improve system efficiency at low output power of 0–3 dBm. Its required matching network was realized by exploiting different behaviors of a 2:1 step-down transformer in differential and common-mode excitations.

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