Analytical Approach to Statistical Logic Cell Delay Analysis and its Extension to a Timing Graph

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***Abstract*—In this paper we propose a new methodology to determine the delay of combinational circuits within the framework of statistical static timing analysis (SSTA). The methodology is based on exact analytical solutions for the probability density functions of logic gate delays. Assuming initial delays of the input arrival times and operation time of gates to be normally distributed, the non-Gaussian distribution of the resulting delay of a gate is obtained, as well as its first two moments. This allowed us to propose a novel closed-loop algorithm for the calculation of delay propagation in combinational circuits. Possible extensions and future steps are discussed.**

I. Introduction

The continuous reduction of feature size is creating new challenges for the timing analysis of digital integrated circuits (ICs) as process-related uncertainties begin to dominate behavior. A digital IC design must operate safely at the specified frequency of the clocks without any timing violations, which is typically checked by timing analysis tools [1]–[5].

In general, there are two methods for performing the timing analysis of an IC, dynamic and static. Dynamic timing analysis, or dynamic timing verification, requires the creation of a vector of all possible input transitions and input arrival times for each gate. The number of such input vectors grows exponentially with the number of possible gate pins, which makes dynamic timing analysis ineffective for modern ICs with millions of multi-input gates.

Another method which has less computation cost is a static timing analysis that approximates the maximum and minimum delays of an IC [4]. Static timing analysis (STA) does not depend on the data values being applied at the input pins. Traditionally, STA is deterministic, so that the circuit delay is computed for specific process conditions: i.e., process parameters, supply voltage and temperature are all assumed to be fixed and uniformly applied to all devices. Then, a so-called corner file is created to determine the delay of the gates.

As technology continues to scale down, the impact of process variations (such as process-voltage-temperature variations) on timing grows (see eg. [6], [7]). Also variations arise from the manufacturing process (e.g. transistor length is difficult to control exactly). Moreover, with decreasing size of transistors and interconnect width, the variations of electrical characteristics can be of the same order as nominal values. Therefore, the use of approaches known as statistical static timing analysis (SSTA) is increasing [8], [9].

Within the SSTA all delays are treated as random variables with corresponding probability density functions (PDFs) [10]–[20]. Three main challenges of SSTA that have been addressed with different

degrees of success: (i) impact of spatial correlations, (ii) non-analytical operations such as $\max$, and (iii) non-Gaussian distributions of variations. The correlations for both Gaussian and non-Gaussian cases were considered in [10], [11], [21]. A block-based incremental timing analysis framework was proposed and analysed in [12], [17], [18]. The approximation for the maximum operation applied to random variables was considered, e.g. in [18], [22]–[26]. We address the interested reader to the review articles [27]–[30].

Recent papers show an increasing interest in SSTA [31]–[36], and the need for fast algorithms for stochastic analysis has increased [37]. For this reason, the aim of this study is to initiate a new statistical approach that relies on an analytical treatment of one gate. We propose a closed form expression for the "maximum" operation ($\max$) with consequent convolution with a delay representing a gate and/or interconnect delay. In this study, for the purposes of simplicity we approximate obtained exact non-Gaussian distribution of gate delay then by a Gaussian in a manner described in [38] by matching two first moments. This allows us to investigate the degree of deviation of the exact distribution from Gaussian one. While the approach appears to be standard, it allows one to see the 'mechanism' of the skewness and kurtosis formation. In principle, the proposed algorithm can be extended to a number of practically important cases such as correlated variables and non-Gaussian model distributions. As is expected, working with an analytical approach would not be time and resource demanding and would allow a faster analysis of a very large circuit.

The article is organized as follows. Section II introduced a general statement of the problem where we relate a combination logic circuit to its graph and explain the statement of the problem as a mathematical problem of delay propagation through that graph. Section III describes the steps that are involved in the analysis of delay propagation through one node (gate): taking the $\max$ operation and performing convolution with gate and/or interconnect delay. Section IV presents the results of simulations and comparison with a reference method (Monte-Carlo). Finally, Section V presents discussions on further development of the method and conclusions.

II. Statement of the Problem

A combinational logic circuit traditionally is represented by its timing graph [2], [5]. Edges of the graph represent gates and vertex set is for inputs and outputs of the logic gates (see Fig. 1). The vertices are either representing inputs of gates or gate's output. Sometimes timing graphs are presented in more detail for gates: each gate is presented by a set of vertices, one of which is output and the rest is input. But we will keep the simple structure as presented in the figure.

Since the gates have internal structure presented by corresponding combination of transistors, this results in a characteristic time needed for gates to operate. This is one of the sources of delays in a circuit. Due to delays, input signals can have different arrival times and, therefore, the delay of a gate is determined by the maximum of input delays.

So, the main problem of timing analysis for such circuits can be formulated as the mathematical problem of calculating the $\max$ function of arrival times. In other words, this is a problem for the graph optimization.

On the other hand, operation time of a gate can have a significant impact on circuit delay, in addition to the arrival times. In such a case the delay of a gate itself should be added to the result of the $\max$ function.

The situation is straightforward in the case of deterministic timing analysis, but it is not the case when uncertainty arises. When it is necessary to include variations of parameters, the SSTA is required. In such a case arrival and gate operation times are described by random variables (RVs) given by corresponding distributions.

The situation becomes even more dramatic in a lower scale, when variations are of the order of the nominal values of parameters. Here, the problem of calculating of the $\max$ of two or more RVs discussed in the Introduction occurs.

At the same time, it is impossible to ignore interconnect delays [39]. However, the latter can be added to the gate delay. Thus, the procedure of

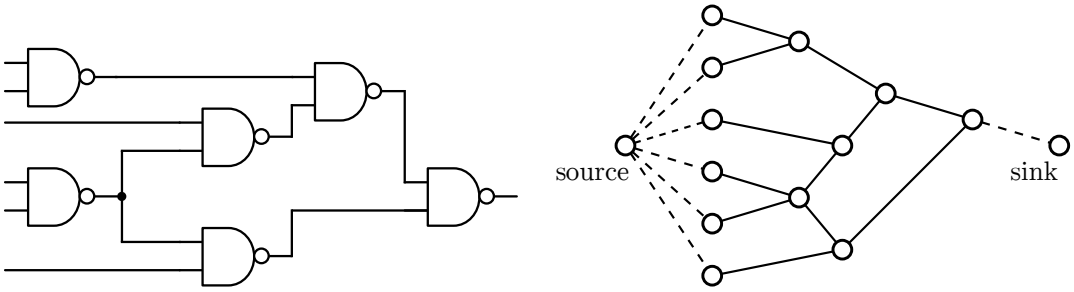

Fig. 1. An example combinational circuit and its timing graph.

the delay computation in one gate with two inputs can be written as

$$\ldots + \max(D_1, D_2) + D_{\text{gate}} + D_{\text{int}} + \ldots, \quad (1)$$

where D_1, D_2 are input signal delays, D_{gate} is a gate delay and D_{int} is an interconnect delay. In the case of Gaussian distributions, the convolution for the latter two terms can be easily performed, resulting to another Gaussian distribution.

In the next section we look in a detail at the delay propagation inside logic gates.

III. Logic Gate Delay

Let us consider a simple logic gate with two inputs, and let us suppose we have two arrival signals with known delays, A and B, and these delays are distributed normally. We shall describe these delays as Gaussian variables, X_1 and X_2, with given mean values, μ_1 and μ_2, and variances, σ_1^2 and σ_2^2. Note, the correlations are not discussed in this consideration, but all obtained results can be easily generalized to the correlated case.

A. Handling the max Operation

The computing of a maximum is not a straightforward task since the operation is non-linear (see [18], [26]). The situation is even more complicated when applied to randomly distributed variables. For the RVs X_1 and X_2 with probability density functions (PDF) $f_1(x)$ and $f_2(x)$ and cumulative distribution functions (CDF) $\Phi_1(x)$ and $\Phi_2(x)$ the task is to determine the PDF of another RV, $\max(X_1, X_2)$. For the case of non-overlapping distributions the max is simply the PDF with a biggest mean value. In other words, the initial Gaussian shape holds after the application of the max operation.

The situation is different if RVs are distributed closely to each other and their PDFs overlap. The PDF of $\max(X_1, X_2)$ in this case is clearly non-Gaussian. If X_1 and X_2 are distributed normally (as we are assuming here), the maximum can be obtained analytically. A well-known result is the PDF $f_{\max}(x)$ of a maximum of two independent Gaussian RVs,X_1 and X_2, equals to

$$f_{\max}(x) = f_1(x)\Phi_2(x) + f_2(x)\Phi_1(x). \quad (2)$$

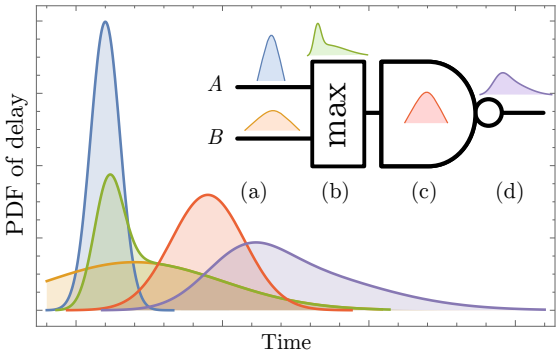

Fig. 2. Illustration for the delay propagation in a logic gate. At the stage (a) two inputs, A and B, with some distributions arrive to a gate. The delay of arrival is determined as $\max(A, B)$ at the stage (b) and leads to a new non-Gaussian distribution. At the same time, a gate has its own operation time which is given by a distribution (c). Thus, the distribution of the gate delay (d) requires the convolution of the obtained distribution (b) and given (c).

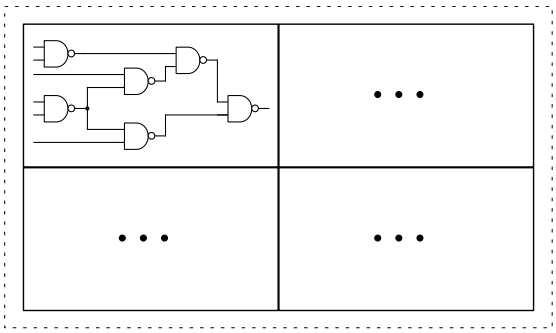

Fig. 3. A cascade of combinational circuits from Fig. 1.

We are not considering correlations between variations in this study (this will be reported elsewhere). However, we would like to point out that introducing correlations at this stage will not make any substantial difficulties. The interested reader can find the correlated case, for instance, in [25].

B. Making the convolution with a gate delay

Let us now assume that the operation time of a gate leads to a delay that can be described as a Gaussian RV X_3 with known mean μ_3 and variance σ_3^2, and the PDF $f_3(x)$. Then, the total delay of a gate is determined by two independent terms, the maximum arrival delay considered above and the delay due to operation time of a gate itself. Since these quantities are RVs, the total delay is also an RV $X = \max(X_1, X_2) + X_3$. In terms of distributions, the *convolution* of $\max(X_1, X_2)$ and X_3 should be performed:

$$(f_{\max} * f_3)(x) = \int_{-\infty}^{\infty} f_{\max}(x') f_3(x - x') dx'. \quad (3)$$

The latter expression (3) leads to the integrals of a kind

$$I(b) = \int_{-\infty}^{\infty} e^{-t^2} \mathrm{erf}(at + b) dt, \quad (4)$$

where a and b stand for some parameters. Such an integral can be taken by differentiation under the sign of an integral over a parameter b (see also [40], [41]). Doing that and integrating the result, $\int_0^b I_b'(x)dx$, one obtains

$$I(b) = \sqrt{\pi} \cdot \mathrm{erf}\left[b \left(\frac{1}{1 + a^2} \right)^{\frac{1}{2}} \right]. \quad (5)$$

Therefore, after the corresponding algebra one obtains the PDF of the total gate delay $f_{\text{tot}}(\ldots)$ as a function of all initial delays in the following form

$$f_{\text{tot}}(\ldots) = \frac{1}{2\sqrt{2\pi}} [I_{12}(x) + I_{21}(x)], \quad (6)$$

where $I_{ij}(x)$ $(i \neq j = 1, 2)$ are

$$I_{ij}(x) = \frac{1}{\sqrt{\sigma_3^2 + \sigma_i^2}} \exp(-\alpha_i x^2 + \beta_i x + \gamma_i) \times \left\{ 1 + \mathrm{erf}\left[b_{ij}(x) \left(\frac{1}{1 + a_{ij}^2} \right)^{\frac{1}{2}} \right] \right\}, \quad (7)$$

and

$$\begin{aligned} \alpha_i &= \frac{1}{2} \frac{1}{\sigma_3^2 + \sigma_i^2}, \quad \beta_i = 2(\mu_3 + \mu_i)\alpha_i, \\ \gamma_i &= -(\mu_3 + \mu_i)^2 \alpha_i = -\frac{1}{2}(\mu_3 + \mu_i)\beta_i \\ a_{ij} &= \frac{\sigma_3 \sigma_i}{\sigma_j \sqrt{\sigma_3^2 + \sigma_i^2}}, \\ b_{ij}(x) &= \frac{\sigma_i^2 x + \sigma_3^2 \mu_i - \sigma_i^2 \mu_3 - (\sigma_3^2 + \sigma_i^2)\mu_j}{\sqrt{2}(\sigma_3^2 + \sigma_i^2)\sigma_j}. \end{aligned} \quad (8)$$

The exact form of a PDF allows one to determine corresponding moments of a distribution. These results are not presented here in view of their excessive length.

C. Summarizing as an algorithm

We have obtained an exact expression for the distribution of a delay through AND-gate assuming that initial delays are normally distributed. Thus, it is crucial for the input delays in a gate to be in a Gaussian form. This allows us to build a closed-loop algorithm as follows.

(i) At the very first step two delays are taken as Gaussian RVs, $X_1 \sim N(\mu_1, \sigma_1)$ and $X_2 \sim N(\mu_2, \sigma_2)$. The mean values and variances are given.

(ii) The delay at the input of a gate is calculated as $\max(X_1, X_2)$ using (2).

(iii) If a gate itself has its own pre-assigned delay, which is also assumed to be Gaussian RV $X_3 \sim N(\mu_3, \sigma_3)$, then the convolution is performed and the PDF of a resulting delay should be calculated according to (6)–(8).

(iv) The mean μ and variance σ^2 of the total skewed non-Gaussian distribution can be calculated now.

(v) The obtained distribution of a delay is approximated now by a Gaussian one with determined μ and σ^2 in (iv). Now this new Gaussian distribution is considered as a distribution for the gate's delay and then translated to the next gate.

Algorithm 1: GATEDELAY finds the PDF of a delay of combinational circuits.

Input: μ_i, σ_i of gates' operation times, number of gates N_{G}

Output: PDF, mean and variance of the delay of a circuit

for $i \leftarrow 1, N_{\mathrm{G}}$ **do**
  max $\leftarrow$ (2)
  convolution $\leftarrow$ (6)–(8)
  Determine μ_{tot} and σ_{tot} of a total gate delay
  Approximate actual PDF with the Gaussian
return final PDF of a circuit

Below a simple realization of the algorithm as well as the discussion of possible extensions.

IV. Simulation Results

To test the performance of the algorithm a set of realistic parameters of input signal delays for the circuit from Fig. 1 were chosen and are summarized in the Table I. Here I_i $(i = 1, \ldots, 6)$ are corresponding delays of input signals. The gate delay G_0 was assumed equally distributed for all gates, and the results for the cases $G_0 \sim N(80, 40)$ and $G_0 \sim N(40, 10)$ are presented correspondingly in Fig. 4 and 5.

In the simulation, 10^7 samples were used for each gate, and the algorithm was 960 times faster than an MC simulation. One can see slight deviation in the average value for both cases, but a more significant error in the determination of σ.

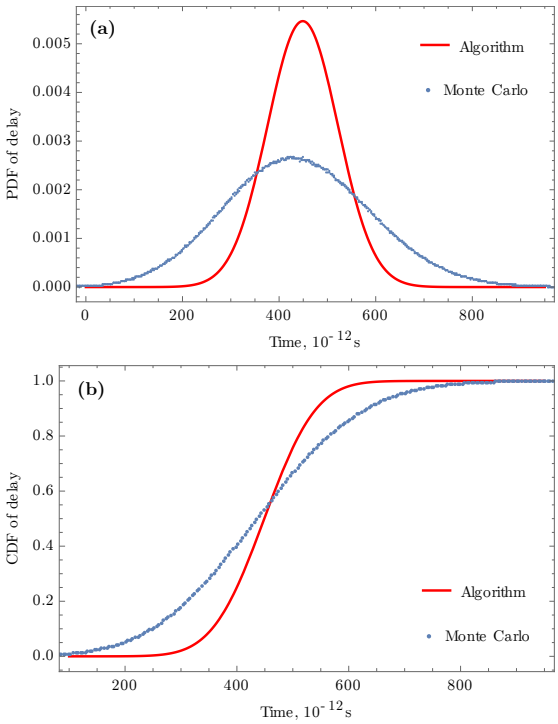

Fig. 4. Probability density function (a) and cumulative density function (b) of the circuit delay ($G_0 \sim N(80, 40)$). The mean is 438 ps from Monte Carlo and 449 ps from the Algorithm, error in mean deviation is 39%.

Also the algorithm was applied to a cascade of circuits (see. Fig. 3) with a total number of 46 gates and to a series of randomly generated graphs with a total number of 100 gates. The results are not presented here.

V. Discussions and Conclusions

The complexity of modern circuits increases and as a result it is impossible to apply Monte-Carlo based methods to verify them. However verification is more important than ever since the uncertainty (parameter variation) is next-generation CMOS circuits will have even greater impact. Statistical static timing analysis is considered to be helpful, but there are certain issues associated with it.

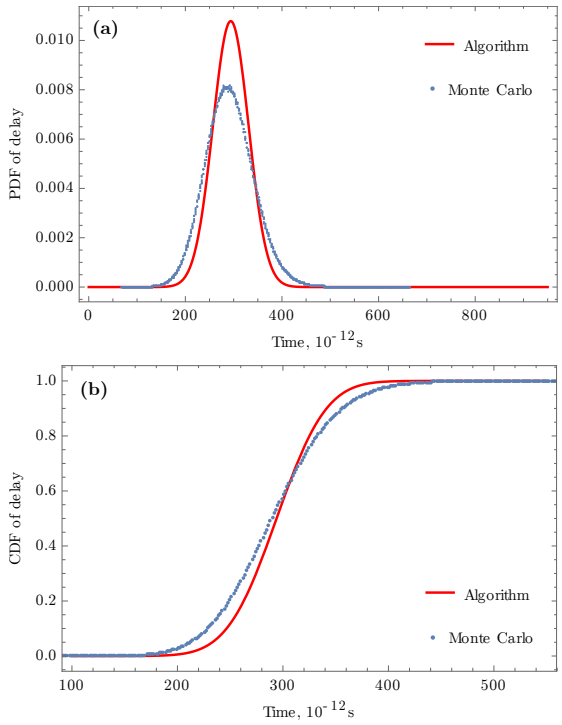

Fig. 5. Probability density function (a) and cumulative density function (b) of the circuit delay ($G_0 \sim N(40, 10)$). The mean is 291 ps from MC and 294 ps from the Algorithm, error in mean deviation is 7.5%.

TABLE I
INPUT SIGNAL DELAY PARAMETERS FOR THE CIRCUIT FROM FIG. 1

pin	distribution
I_1	$N(100, 45)$
I_2	$N(50, 30)$
I_3	$N(140, 60)$
I_4	$N(100, 30)$
I_5	$N(50, 30)$
I_6	$N(75, 35)$

The major issue is that the commonly accepted uncorrelated "Gaussian" assumption is not the case: ongoing research indicates that either a gate delay distribution is not Gaussian, or the result of $\max$ operation is strongly non-Gaussian. This is the weakest link in all current statistical methods because this means that the simple expressions for the delay distributions are not valid any more. To address some of the resulting issues, see e.g. [26].

The $\max$ operation distorts significantly the distribution of the delay. Even though the actual gate and interconnect delays are considered to be Gaussian, when delay propagates it quickly becomes non-Gaussian. The error accumulates and for certain combinations of gate distributions a considerable error results. The effect may not be critical for some parameters but can lead to significant errors in others.

In this work we propose semi-analytical algorithm based on Gaussians distributions but which goes beyond existing results and allows further generalization. The key outcome is the fully analytical expression for the convolution of $\max$ of two Gaussians with the gate and/or interconnect delay. Then, at every iteration of the algorithm the resulting non-Gaussian distribution is approximated by a Gaussian one. Indeed, approximation of non-Gaussian by matching two first moments is a standard tool. Also the approximation can be done in a more accurate way as the error minimization problem [24]. We would like to reiterate that the main aim of this research is to study the feasibility of approximations by Gaussians and the trades-off of these approximations.

We see several advantages and possible extensions of this work as follows. Firstly, it is based on analytical expressions which are fast to compute. Secondly, the results can be expanded to correlated variables: while the expression can be somewhat complex but it will not bring any substantial difficulty. Thirdly, the semi-analytical approach can be, in principle, derived for other model distributions that can accommodate skewness and kurtosis, which are the major sources of the inaccurate prediction of σ. At the moment one of the algorithm steps that makes it semi-analytical is the replacements of the gate output distribution with a Gaussian one. This is, as was pointed out, the weakest link of all statistical approaches which in principal may result in wrong standard deviation. Working with other model distributions will improve this. We are seeking to address these issues in our on-going research.

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