Broadband Fully Integrated GaN Power Amplifier With Embedded Minimum Inductor Bandpass Filter and AM-PM Compensation

Gholamreza Nikandish, *Member, IEEE,* Robert Bogdan Staszewski, *Fellow, IEEE,* and Anding Zhu, *Senior Member, IEEE*

***Abstract*—In this paper, we present a design technique for broadband linearized fully integrated GaN power amplifiers (PAs). The minimum inductor bandpass filter structure is used as the output matching network to achieve low loss and high out-of-band attenuation. Two parallel transistors with unbalanced gate biases are used to mitigate nonlinearity of their transconductance and input capacitance, and consequently, compensate AM-PM distortion of the PA. A fully integrated GaN PA prototype provides 35.1–38.9 dBm output power and 40-55% power-added efficiency (PAE) in 2.0–4.0 GHz. For a 64-QAM signal with 8-dB peak-to-average power ratio (PAPR) and 100-MHz bandwidth at 2.4 GHz, average output power of 32.7 dBm and average PAE of 31% are measured with −30.2 dB error vector magnitude (EVM).**

***Index Terms*—5G, AM-PM, broadband amplifier, GaN, monolithic microwave integrated circuit (MMIC), power amplifier.**

I. Introduction

GaN technology enables implementation of power amplifiers (PAs) with high output power and efficiency. The impressive performance improvements of GaN have attracted new applications in the fifth generation (5G) wireless networks where stringent linearity and efficiency requirements should be satisfied over a broad bandwidth [1].

In monolithic microwave integrated circuit (MMIC) PAs, matching networks should be designed with special attention to minimizing insertion loss and maintaining compact chip area. In a broadband transmitter, the PA is normally followed by a bandpass filter (BPF) to suppress out-of-band distortions. It is desirable to *embed the filtering function* into the PA circuit to improve efficiency and reduce size of the overall system [2]. Linearity of the PA is of paramount importance to accommodate spectrally efficient modulated signals with non-constant envelope. The *soft compression* feature of GaN HEMTs exacerbates nonlinearity of the PA, especially for modulated signals with large peak-to-average power ratio (PAPR) [3].

In this paper, we present a design approach for broadband PAs in a GaN MMIC technology, with AM-PM linearization using a two-transistor power cell structure. The output and input matching networks are realized using a special BPF structure, namely minimum inductor network [4], with superior out-of-band attenuation, low loss, and compact integrated circuit realization.

Manuscript received May 30, revised July 1, 2019. This research has received funding from the European Union's Horizon 2020 Research and Innovation Program under the Marie Sklodowska-Curie grant agreement number 713567, and Science Foundation Ireland (SFI) under grant numbers 13/RC/2077 and 16/IA/4449.

The authors are with the School of Electrical and Electronic Engineering, University College Dublin, Dublin, Ireland (nikandish@ucd.ie, robert.staszewski@ucd.ie, anding.zhu@ucd.ie).

II. Minimum Inductor Matching Networks

The minimum inductor BPF structure can provide wide bandwidth and large out-of-band attenuation with smaller inductors compared to standard filter structures [4]. The large out-of-band attenuation helps to improve efficiency by providing reactive load impedance in the second-harmonic bandwidth, while the small inductor feature is useful in low-loss and compact chip area implementation. This filter cannot be directly synthesized from a low-pass prototype. Thus, we develop a new design approach for output and input matching networks of the PA[1].

A. Output Matching Network

The output matching network should transform the load impedance R_L into the optimum load resistance of the transistor R_{opt} over the bandwidth $\omega_L \leq \omega \leq \omega_H$. It should provide a reactive load impedance in the second-harmonic bandwidth to maximize efficiency of the PA. We propose to use the circuit shown in Fig. 1(a) as output matching network of the PA. It is assumed that $R_{opt} > R_L$, which is usually the case for GaN transistors[2]. Neglecting loss of passive components, it can be shown that the following conditions should be satisfied at the center of the frequency band, $\omega_c = \sqrt{\omega_L \omega_H}$, to achieve the optimum load resistance

$$X_p(\omega_c) = \pm \frac{1}{Q_o} R_{opt} \tag{1}$$

$$X_s(\omega_c) = \mp Q_o R_L, \tag{2}$$

where $Q_o = \sqrt{R_{opt}/R_L - 1}$ is the loaded quality factor of the network. Assuming $C_1 = C_{ds}$, using (1) with plus sign and $X_p(\omega) = L_1\omega/(1 - L_1 C_1 \omega^2)$, L_1 is derived as

$$L_1 = \frac{R_{opt}}{\omega_c} \frac{1}{Q_o + R_{opt} C_{ds} \omega_c}. \tag{3}$$

[1]The design procedure developed here can be extended to multi-section networks which can provide wider bandwidth and lower loss for large impedance transformation ratio.

[2]In the case of $R_{opt} < R_L$, the network should be modified to include a parallel branch with the load resistance, which has the same circuit topology as the series branch.

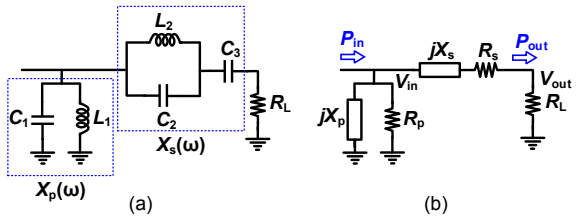

Fig. 1. Output matching network of the PA: (a) circuit schematic, (b) equivalent circuit for efficiency calculation.

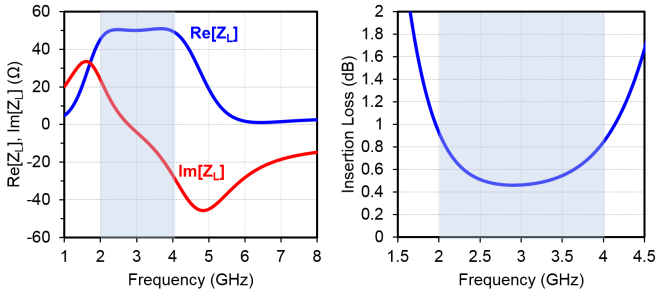

Fig. 2. Load impedance presented to the transistor and insertion loss of the output matching network.

Using the circuit in Fig. 1(a), reactance $X_s(\omega)$ is derived as

$$X_s(\omega) = \frac{(\omega/\omega_s)^2 - 1}{1 - (\omega/\omega_o)^2} \frac{1}{\omega C_3} \tag{4}$$

which acts as an open-circuit at $\omega_o = 1/\sqrt{L_2 C_2}$ and as a short-circuit at $\omega_s = 1/\sqrt{L_2(C_2 + C_3)}$. By choosing $\omega_o = 2\omega_c$, an almost reactive impedance composed of $L_1||C_1$ is achieved at the second-harmonic band, which is required to achieve a high efficiency. Moreover, ω_s can be adjusted within $\omega_c < \omega_s < \omega_o$ to control bandwidth. With chosen ω_o and ω_s, (2) with minus sign and (4) can be used to determine C_3, C_2, and L_2 as follows

$$C_3 = \frac{1 - (\omega_c/\omega_s)^2}{1 - (\omega_c/\omega_o)^2} \frac{1}{\omega_c Q_o R_L} \tag{5}$$

$$C_2 = \frac{C_3}{(\omega_o/\omega_s)^2 - 1} \tag{6}$$

$$L_2 = \frac{1}{C_2 \omega_o^2}. \tag{7}$$

Efficiency of the output matching network is an important metric in integrated circuit PAs. Using the equivalent circuit shown in Fig. 1(b), and assuming that resistances representing losses meet the conditions $R_p \gg R_{opt}$ and $R_s \ll R_L$, it can be shown that the efficiency is derived as

$$\eta_o = \frac{1 - R_{opt}/R_p}{1 + R_s/R_L} \approx 1 - \frac{R_{opt}}{R_p} - \frac{R_s}{R_L}. \tag{8}$$

Using Fig. 1 and (3)–(7), the efficiency can be derived in terms of the circuit parameters.

$$\frac{R_{opt}}{R_p} = \frac{Q_o + R_{opt} C_{ds} \omega_c}{Q_{L1}} \tag{9}$$

$$\frac{R_s}{R_L} \approx \frac{Q_o}{Q_{L2}} \frac{(\omega_o/\omega_s)^2 - 1}{[1 - (\omega_c/\omega_s)^2][(\omega_o/\omega_c)^2 - 1]} \tag{10}$$

where Q_{L1} and Q_{L2} denote quality factors of the inductors. The efficiency degrades for higher impedance transformation ratio R_{opt}/R_L, and hence higher Q_o, while it can be improved using inductors with larger quality factor. The efficiency is also dependent on the process parameter $R_{opt}C_{ds}$, the center frequency ω_c, and the series reactance's open- and short-circuit frequencies, ω_o and ω_s.

We use this design approach for a broadband 2–4 GHz PA in a 0.25-μm GaN-on-SiC technology. The device is composed of two parallel transistors with 6×125-μm width and 28 V supply voltage to achieve 37 dBm output power over the bandwidth. Using load-pull simulations, R_{opt} and C_{ds} are derived as 55 Ω and 1 pF, respectively. The low impedance transformation ratio of 1.1 leads to a small Q_o of 0.32. The single-section network of Fig. 1 is therefore used as output matching network of the PA. Using $\omega_o = 2\omega_c$ and ω_s/ω_c as a design parameter, the circuit elements are derived from (3), (5)–(7). From the circuit frequency response (not shown due to limited space), ω_s/ω_c is chosen as 1.2 to achieve a broadband optimum load resistance. Using (8)–(10), the efficiency of the output matching network is derived as

$$\eta_o \approx 1 - \frac{1.29}{Q_{L1}} - \frac{0.62}{Q_{L2}}, \tag{11}$$

indicating that Q_{L1} is more critical for efficiency. As the inductor L_1 should also meet a minimum width based on electromigration current density limit (16 μm in this process), it is realized as a meandered microstrip transmission line, while a spiral inductor structure with small chip area is chosen for L_2. In this design, $Q_{L1} \approx 18$ and $Q_{L2} \approx 15$, leading to $\eta_o \approx 88.7\%$ (0.52 dB insertion loss)[3].

In Fig. 2, load impedance presented to intrinsic drain of the transistor and insertion loss of the designed output matching network are shown versus frequency. In 2–4 GHz, the real part of the load impedance is almost flat and equal to R_{opt}, while in the second-harmonic band it rolls off to zero. The imaginary part of the load impedance is zero at the center of the frequency band, $f_c = \sqrt{f_L f_H} \approx 2.8$ GHz, as expected from the theory. In the second-harmonic band, load impedance is located inside high-efficiency area of Smith chart determined using load-pull simulations. Insertion loss of the output matching network is 0.46–0.93 dB in the target 2–4 GHz frequency band. The simulated minimum insertion loss is close to the theoretical insertion loss predicted by (11), while this increases toward edges of the frequency band as a result of imperfect impedance matching.

B. Input Matching Network

The design of input matching network is less critical than that of the output matching network. The output power and efficiency are not much sensitive to source impedance mismatch, while a moderate insertion loss can be exploited to improve bandwidth and gain flatness of the PA [5]. We use the circuit shown in Fig. 3 as the input matching network of the PA. This

[3]The out-of-band attenuation is also determined by Q_{L1} and Q_{L2}. It can be shown that $P_{out}(2f_c)/P_{out}(f_c) \approx 0.23/(1 + 0.7Q_{L2})^2 \approx -28$ dB (in this case). It is noted that Q_{L2} has the dominant effect here.

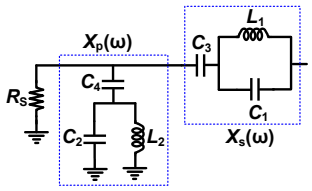

Fig. 3. Input matching network of the PA.

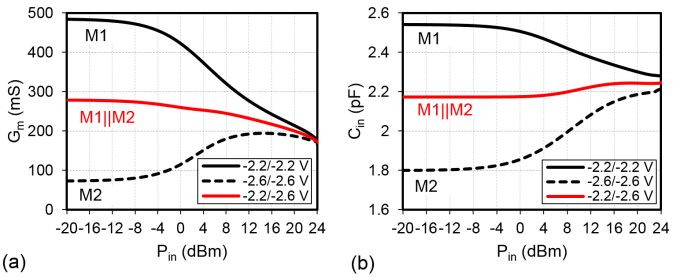

Fig. 4. Simulated (a) average transconductance and (b) input capacitance of two parallel GaN HEMTs versus input power (for a 0.25-μm GaN process).

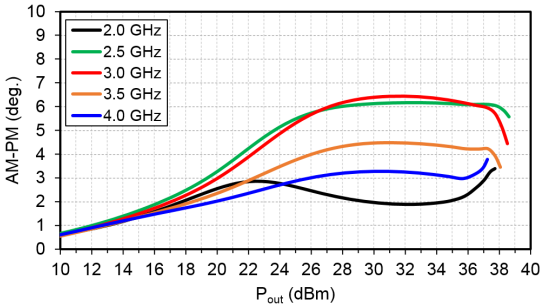

Fig. 5. Simulated AM-PM of the PA in 2–4 GHz.

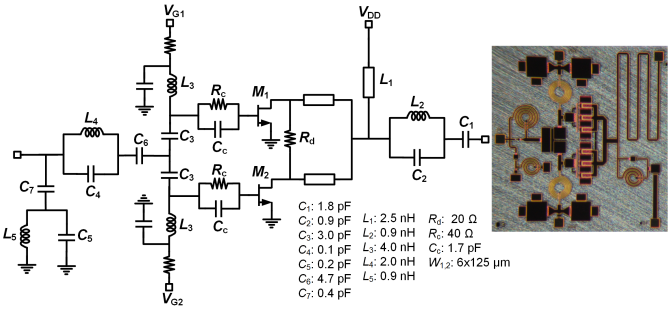

Fig. 6. The PA circuit schematic and chip micrograph (1.8 mm × 1.8 mm).

circuit transforms the source impedance into the complex optimum source impedance $R_{S,opt}+jX_{S,opt}$ with $R_{S,opt} < R_S$. The short-circuit frequency of the parallel reactance can be adjusted to achieve a reactive source impedance at the second-harmonic frequency band, $\omega_{s,P} \approx 2\omega_c$. Furthermore, the source impedance contributes to the nonlinear mechanism that transforms the transistor's input capacitance nonlinearity into AM-PM distortion [3]. It is shown that AM-PM is substantially increased when the input matching network has a high quality factor. The input matching network is designed to provide a moderate input matching $S_{11} < -8$ dB, but a low quality factor of 0.4–0.8 in the 2–4 GHz bandwidth.

III. AM-PM Compensation

GaN HEMT device exhibits some distinct nonlinear behavior that requires special attention in the PA circuit design. The soft gain compression degrades linearity of the PA, especially for complex-modulated signals with large PAPR [3]. The AM-AM and AM-PM distortion mechanisms in the GaN HEMT are investigated and it is shown that nonlinearity of the transistor's transconductance and parasitic capacitances (mainly the input capacitance) dominate nonlinearity of the PA [3]. The input capacitance nonlinearity is composed of the gate-source capacitance nonlinearity and variable feedback effect of the almost voltage-independent gate-drain capacitance, $C_{in} \approx C_{gs}+(1+G_m Z_L)C_{gd}$, where Z_L denotes the transistor's load impedance. It is noted that deviation of the load impedance from R_{opt} over the bandwidth leads to a frequency-dependent nonlinear input capacitance. The form of nonlinearities is dependent on the transistor mode of operation. For low (and zero) bias currents toward the class-C mode, nonlinearity is expanding with the input power, while it becomes compressing when the bias current is increased toward the class-A mode. As shown in Fig. 4, using two parallel transistors with unbalanced gate biases (e.g., $(-2.2,-2.6)$ V in this case), nonlinearity of total average transconductance $G_{m1}+G_{m2}$ and average input capacitance $C_{in1}+C_{in2}$ can be compensated[4]. In practice, the bias setting can be further fine-tuned in modulated-signal measurements to achieve the lowest error vector magnitude (EVM) or adjacent channel leakage ratio (ACLR).

In Fig. 5, AM-PM distortion characteristic is shown in the frequency band 2–4 GHz. The AM-PM remains smaller than 6.4° up to 37 dBm output power, with 4° maximum variations over the bandwidth. As expected, AM-PM characteristic changes with frequency but remains close to the results obtained using the optimum bias setting.

[4]It is possible to use a single transistor with an appropriate gate bias to mitigate the nonlinearity. However, using parallel transistors with separate biases allows to independently compensate the nonlinearities of transconductance and input capacitance, which may not be achieved at the same bias point.

IV. Experimental Results

The PA is implemented in a 0.25-μm GaN-on-SiC technology from WIN Semiconductors. The PA is biased at supply voltage of 28 V and gate voltages of $(-2.2,-2.6)$ V. The circuit schematic and chip micrograph of the PA are shown in Fig. 6. Components $R_c||C_c$ and R_d are respectively used to ensure low-frequency stability and prevent odd-mode oscillations [5]. It is also important to maintain symmetry of the bias circuit to avoid an odd-mode instability.

A. CW Measurements

In Fig. 7, measured gain and PAE are shown versus output power. The maximum PAE of 47.9% is measured with 37.5 dBm output power at 2.0 GHz. The output power, drain efficiency (DE), and PAE versus frequency are shown in Fig.

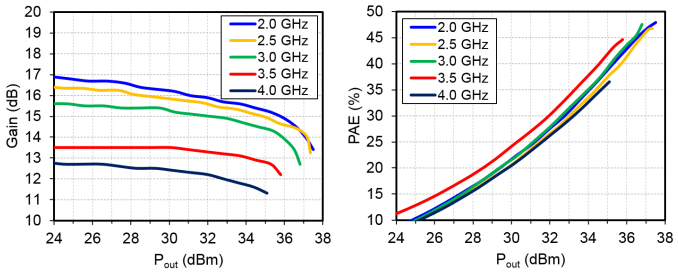

Fig. 7. Measured gain and PAE versus output power.

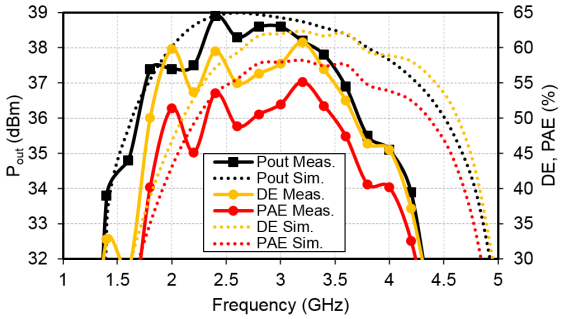

Fig. 8. Measured and simulated output power, DE, and PAE versus frequency at a fixed input power of 27 dBm.

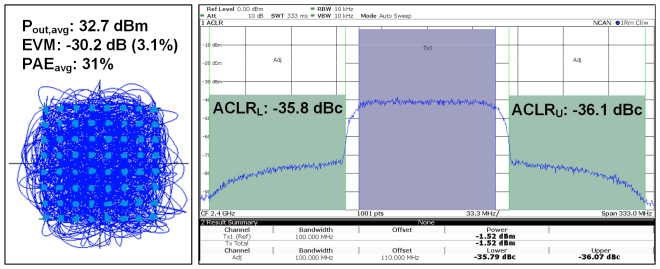

Fig. 9. Measured output constellation and spectrum for 100-MHz 64-QAM signal with 8-dB PAPR at 2.4 GHz.

8, at a fixed 27 dBm input power (saturation). The PA provides 35.1–38.9 dBm output power, 45–61% DE, and 40–55% PAE in 2.0–4.0 GHz.

B. Modulated-Signal Measurements

The modulated-signal measurements are performed using a 64-QAM signal with 100 MHz bandwidth and 8-dB PAPR. Measured output constellation and spectrum are shown in Fig. 9. The average output power and PAE are 32.7 dBm and 31%, with an EVM of −30.2 dB (3.1%). Moreover, an ACLR of −35.8/−36.1 dBc is achieved at lower/upper channels, without any predistortion. In Fig. 10, EVM and average PAE are shown versus average output power.

Performance of the PA is compared with broadband high-efficiency fully integrated GaN PAs in Table I. The proposed PA features high efficiency over a broad fractional bandwidth (FBW) and reports the most compact chip area.

V. Conclusion

We presented a design approach for broadband linearized PAs using minimum inductor matching networks and two

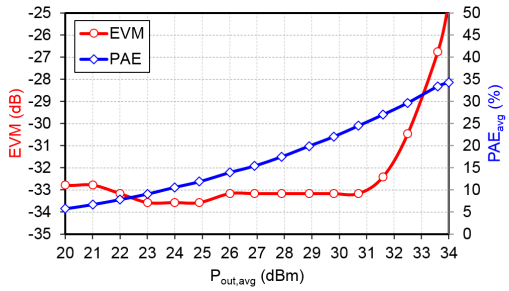

Fig. 10. Measured EVM and average PAE versus average output power for a 100-MHz 64-QAM signal with 8-dB PAPR at 2.4 GHz.

TABLE I
Comparison of Broadband Fully Integrated GaN PAs

	This Work	[6]	[7]	[8]	[9]
BW (GHz)	2.0–4.0	1.0–8.0	6.4–8.3	6.0–18.0	4.9–5.9
FBW (%)	70.7	247.5	26.1	115.5	18.6
P_o (dBm)	35.1–38.9	39.4–40.6	36–36.6	44.8–47.2	37–37.7
PAE (%)	40–55	30–47	40–50	13–30	48–55
Gain (dB)	9.5–11	24.4–26	10–12	9.8–12.2	28.5–31.7
Modulation	64-QAM	—	256-QAM	—	256-QAM
BW_m (MHz)	100	—	7	—	80
PAPR (dB)	8	—	7.4	—	11.25
f_c (GHz)	2.4	—	7	—	5.7
EVM (dB)	−30.2	—	—	—	−32
$P_{o,avg}$ (dBm)	32.7	—	28.7	—	30.6
PAE_{avg} (%)	31	—	26	—	27
Area (mm^2)	3.2	11.7	7.8	47.1	4.7
Process (μm)	0.25	0.15	0.25	0.18	0.25

parallel transistors with unbalanced gate biases. A fully integrated GaN PA prototype provided over 40% PAE in 2–4 GHz (70.7%) bandwidth. Using a 64-QAM signal with 8 dB PAPR, 31% average PAE was achieved with −30.2 dB EVM.

References

[1] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.

[2] K. Chen, J. Lee, W. J. Chappell and D. Peroulis, "Co-design of highly efficient power amplifier and high-*Q* output bandpass filter," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 11, pp. 3940–3950, Nov. 2013.

[3] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "AM/AM and AM/PM distortion generation mechanisms in Si LDMOS and GaN HEMT based RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 799–809, Apr. 2014.

[4] H. Watanabe, "On the circuit with a minimum number of coils," *IRE Trans. Circuit Theory*, vol. CT-7, no. 1, pp. 77–78, Mar. 1960.

[5] G. Nikandish and A. Medi, "A design procedure for high-efficiency and compact-size 5–10-W MMIC power amplifiers in GaAs pHEMT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2922–2933, Aug. 2013.

[6] Qorvo, "1–8 GHz 10 W GaN power amplifier," QPA1003D datasheet, Apr. 2017.

[7] R. Quaglia, V. Camarchia, M. Pirola, J. J. M. Rubio, and G. Ghione, "Linear GaN MMIC combined power amplifiers for 7-GHz microwave backhaul," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2700–2710, Nov. 2014.

[8] M. Litchfield and J. J. Komiak, "A 6–18 GHz 40 W reactively matched GaN MMIC power amplifier," *IEEE MTT-S Int. Microw. Symp. (IMS)*, 2018, pp. 1348–1351.

[9] B. Liu, M. Mao, C. C. Boon, P. Choi, D. Khanna, and E. A. Fitzgerald, "A fully integrated class-J GaN MMIC power amplifier for 5-GHz WLAN 802.11ax application," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 434–436, May 2018.