A 30-GHz Class-F$_{23}$ Oscillator in 28nm CMOS Using Harmonic Extraction and Achieving 120 kHz 1/f^3 Corner

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Abstract—This paper presents a mmW frequency generation stage aimed at minimizing phase noise via waveform shaping and harmonic extraction while suppressing flicker noise upconversion via proper harmonic terminations. A second-harmonic tank resonance is assisted by a proposed embedded decoupling capacitor inside a transformer for shortest and well controlled common-mode current return path. Class-F operation with third-harmonic boosting and extraction techniques allow maintaining high quality factor of a 10 GHz tank at the 30 GHz frequency generation while providing implicit divide-by-3 functionality. The proposed 27.3-31.2 GHz oscillator is implemented in 28-nm CMOS. It achieves phase noise of -106 dBc/Hz at 1-MHz offset and figure-of-merit (FoM) of -184 dB at 27.3GHz. Its flicker phase-noise (1/f^3) corner of 120 kHz is an order-of-magnitude better than currently achievable at mmW.

Keywords—low flicker noise corner; low phase noise; oscillator; 30GHz, 5G Communication

I. INTRODUCTION

Due to the severe bandwidth congestion at the traditional cellular bands, i.e., < 6 GHz, the 5G cellular communications start to utilize lower millimeter-wave (mmW) frequency bands, e.g., 28 GHz. To support high data rates, complex modulation schemes are required, thus placing tough requirements on phase noise (PN) of local oscillators. It is well known that at mmW, the quality factor (Q) of a switched-capacitor (SC) tuning network degrades significantly, thus dominating Q-factor of the LC-tank and leading to worse PN in the thermal noise region ($1/f^2$). Recently, there have been solutions proposed to maintain high Q-factor of the tank, such as: 1) inductor-based oscillator with frequency multiplier using frequency doubler/quadrupler [1-2] or sub-harmonic injection locking [3], and 2) transformer-based class-F oscillator with a tuned PA to extract its 3rd harmonic [4].

Despite reasonably good phase noise performance in the $1/f^2$ region, flicker phase noise corner ($1/f^3$) of >10 GHz oscillators usually exceeds 1 MHz, as surveyed in Fig. 1. More importantly, as CMOS scales, the flicker noise corner ($1/f$) of MOS transistors appears to worsen, thus further degrading the mmW frequency generation. Due to the high multiplication ratio N of mmW PLLs (e.g., N = 300 for a 30 GHz oscillator locked to a typical 100 MHz reference), the loop bandwidth needs to be kept narrow as to prevent the reference noise from dominating the PLL performance. This unfortunately causes only a *partial* attenuation of the oscillator's flicker noise. Consequently, techniques to lower the flicker phase-noise corner are highly desired for frequency generation at mmW.

Recent studies in [5-7] deal with the flicker noise reduction in voltage-biased RF oscillators, i.e., in which the conventional
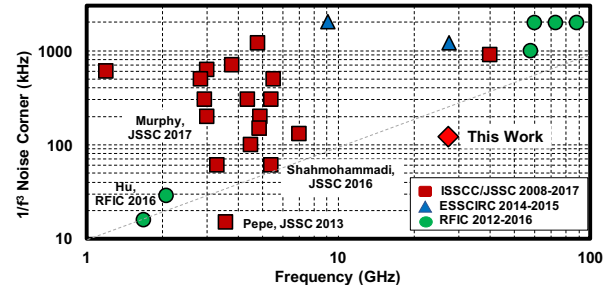

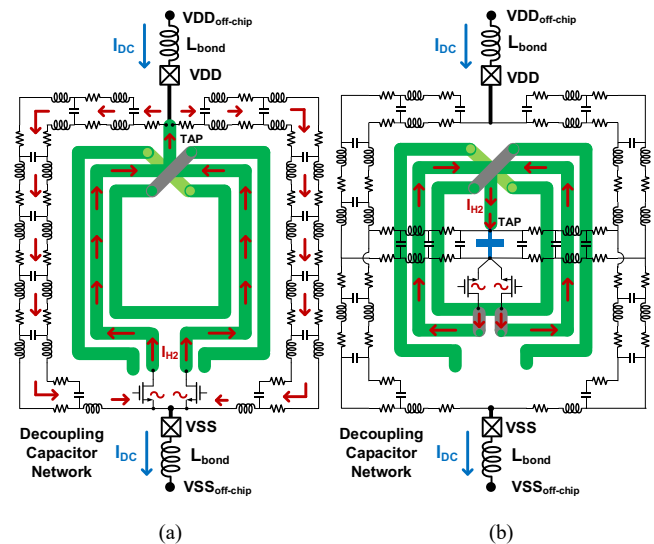Fig.1. Survey of 1/f^3 corner of the state-of-art RF and mmW oscillators.

Fig. 2. (a) Conventional class-F$_{23}$ oscillator [6] w/o the well-controlled CM return path. (b) Proposed 1:2 transformer with embedded decoupling capacitor (blue).
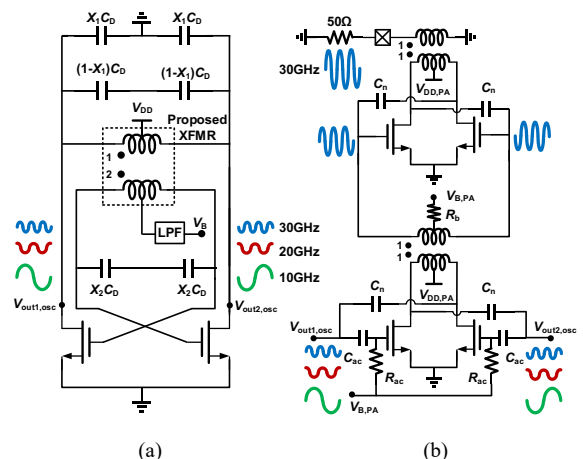

Fig. 3. Proposed 30GHz generation scheme: (a) 10GHz class-F$_{23}$ oscillator w/i proposed 1:2 transformer. (b) 30GHz two-stage PA.

mechanism of flicker-noise upconversion via the tail current source does not appear anymore. In [5], it is suggested that a phase shift between the 1st harmonic voltage and current results in the $1/f^3$ noise corner degradation, which is caused by a 3rd harmonic current (I_{H3}) entering the capacitive path. On the other hand, [6] proposes that the flicker noise up-conversion is due to an asymmetry between rising and falling edges of the tank's voltage waveform, which is a consequence of a 2nd harmonic current (I_{H2}) entering the capacitive path. This is further supported in [7] through an implementation of a 2nd harmonic resonance using an implicit common-mode (CM) LC tank which forces the 2nd harmonic current to enter the resistive path, thus resulting in a low $1/f^3$ noise corner. However, the direct translation of the techniques proposed in [5-7] into mmW do not appear so straightforward. Considering a high-frequency oscillator employing a one-turn inductor [2] or a conventional 1:2 transformer [4], [6], it could suffer from high $1/f^3$ PN corner due to the uncontrolled CM current's (i.e., I_{H2}) return path of the decoupling capacitor (see Fig. 2 (a)), shifting the expected CM resonant frequency.

This paper proposes a 30 GHz frequency generation scheme (shown in Fig. 3) using a 3rd harmonic extraction from a class-F_{23} oscillator that operates at a 10 GHz fundamental and featuring a special 1:2 transformer including a proposed embedded decoupling capacitor for a precisely controlled CM current return path (as illustrated in Fig. 2 (b)). Its PN in the thermal region is kept low via the 3rd harmonic resonance, and its $1/f^3$ PN corner is greatly improved (by an order-of-magnitude vs. state-of-the-art) via a precise implementation of the 2nd harmonic resonance with the assistance of embedded decoupling capacitor. Section II briefly introduces new insights into the understanding of flicker-noise up-conversion in advanced CMOS oscillators with special consideration of both 2nd and 3rd harmonic currents, thus bridging the gap between [5] and [6]. Details of the proposed 30 GHz frequency scheme, focusing on the accurate implementation of the 2nd harmonic mmW resonance, are revealed in Section III. Section IV provides the experimental results.

II. FLICKER NOISE CORNER UP-CONVERSION

A. Flicker Noise Modulation in Scaled CMOS

It is well accepted that the flicker current noise $I_{1/f}$ in a MOS transistor is usually modeled by a product of its wide-sense stationary (WSS) noise voltage source $V_{1/f}$ by its transconductance g_m. Thus, the flicker noise modulation function (NMF) of oscillator is the time-varying transconductance due to the cyclostationary process [6]. However, this model only considers the flicker noise mechanism of carrier number fluctuation (CNF). As CMOS technology scales, another flicker noise mechanism, called correlated mobility fluctuation (CMF), is becoming increasingly important. A more accurate flicker noise model considering both CNF and CMF for advanced CMOS is verified in 14nm FD-SOI under arbitrary bias conditions [8]:

$$\overline{I_{1/f}^2} = \overline{V_{1/f}^2} * (g_m + \Omega I_D)^2 \tag{1}$$

where, $\overline{V_{1/f}^2} = \frac{K}{WL}\frac{1}{\Delta\omega}$ is the flat-band voltage power spectral

density (PSD), K and Ω are the process parameters. The first term in parenthesis represents CNF, which is similar to the conventional flicker noise model, while the second term represents CMF. Based on the oscillator's impulse sensitive function (ISF) theory [9], the cross-coupled pair is in a cyclo-stationary process and its low-frequency noise could be modulated by a NMF to its first harmonic. According to (1), the NMF for flicker noise in cross-coupled pair is the time-varying transconductance and its harmonic current. Assume the output voltage of oscillator is $v_{out}(\omega_0 t) \approx A \cos\omega_0 t$; the 1st harmonic of transconductance is almost in-phase with v_{out} (V_{GS}), if MOS transistor in cross-coupled pair predominantly operates in saturation during one oscillation period, so the time-varying transconductance can be expressed approximately as

$$G_m(\omega_0 t) \approx \frac{1}{2}g_{m,dc} + g_{m,H1}\cos\omega_0 t \tag{2}$$

where, $g_{m,dc}$ and $g_{m,H1}$ are the corresponding Fourier series coefficients. Assume there is a phase shift θ between the 1st harmonic voltage and current as follows:

$$I_D(\omega_0 t) \approx \frac{1}{2}I_{DC} + I_{H1}\cos(\omega_0 t + \theta) \tag{3}$$

Further assume a flicker noise voltage at a low frequency $\Delta\omega$ in cross-coupled pair can be expressed as:

$$v_{\frac{1}{f}}(t) = V_{\frac{1}{f},rms}\cos(\Delta\omega t + \gamma) \tag{4}$$

where $V_{\frac{1}{f},rms}$ is the rms value of $\overline{V_{1/f}^2}$, and γ is an initial phase. Thus, the cyclostationary flicker-noise current is:

$$i_{\frac{1}{f},cyclo}(t) = v_{\frac{1}{f}}(t) * (G_m(\omega_0 t) + \Omega I_D(\omega_0 t)) \tag{5}$$

According to the ISF theory, the normalized impulse sensitivity function $\Gamma(t) \approx -\sin\omega_0 t$, so the phase noise can be derived and the power spectral density for flicker noise energy can be shown:

$$S_{\phi,\frac{1}{f^3}} = \left(\frac{V_{\frac{1}{f},rms}\Omega I_{H1}\sin\theta}{2q_{max}\Delta\omega}\right)^2 \approx \frac{K\Omega^2 I_{H1}^2}{4q_{max}^2 WL\Delta\omega^3} * \sin^2\theta \tag{6}$$

From (6), it is obvious that the θ angle is the key $1/f^3$ noise contributor.

B. Flicker Noise Reduction and Groszkowski Effect

In [10], it is suggested that θ stems from the law of conservation of energy in an LC-tank oscillator (also called "Groszkowski effect"). Briefly, within one oscillation period, the energy generated by a "negative resistance" is consumed by a positive resistance. Similarly, the "imaginary" energy generated by a negative reactance (capacitor) must be consumed by a positive reactance (inductor) within the same cycle. Thus, when the 2nd (I_{H2}) and the 3rd (I_{H3}) harmonic currents enter the capacitive path, they generate more "imaginary" energy, forcing the 1st harmonic current (I_{H1}) to partly enter the inductive path to consume the additional imaginary energy, ultimately introducing the phase shift θ between the 1st harmonic current and voltage. In this work, through a carefully designed implicit CM LC tank, we set CM tank resonance frequency $\omega_{LC,cm}$ a little higher than twice the free running frequency of oscillation ($2\omega_0$). This pushes the 2nd harmonic current to partially enter

the inductor and to consume the "imaginary" energy generated by higher harmonics, i.e. $I_{H4,5}$, which enters the tank's capacitor. Note that the 3rd harmonic current has already entered the resistive path due to the class-F operation. Thus, the 1st harmonic current will enter the purely resistive path ($\theta = 0$), since the imaginary energy is already balanced by the 2nd harmonic current. According to (6), the flicker noise up-conversion will be suppressed.

III. CIRCUIT DESCRIPTIONS

Fig. 3 shows the proposed 30 GHz frequency generation stage, comprising a class-F_{23} oscillator operating at the 10 GHz fundamental and a 30 GHz two-stage PA. By tuning the CM capacitor ratio X_1, the implicit CM resonance can be adjusted. On the other hand, the 3rd harmonic resonance can be properly tuned through secondary and primary capacitor ratio X_2. It is noted that a supply noise in the transformer-based oscillator cannot modulate C_{gs} (but it can only modulate C_{db}), leading to a much better supply pushing than in the inductor-based oscillators. An RC filter is placed in the tap of secondary coil to reduce any noise coupling from V_B. A two-stage 30 GHz PA is used to boost the 3rd harmonic signal and to suppress the lower, i.e., 1st and 2nd harmonics [4]. The C_n is the neutralization capacitor to cancel the Miller effect at the input stage and R_b is used to further suppress the 2nd harmonic in PA.

A. Issue of Uncontrolled Common-Mode Current Return Path

To make $\theta = 0$ for suppressing the flicker noise upconversion, an accurate implementation of the implicit CM tank resonance is required, i.e., the accurate CM inductance is essential. However, the conventional class-F_{23} oscillators do not have a possibility to control the 2nd harmonic (CM) current return path in the decoupling capacitor, as illustrated in Fig. 2(a). The total CM inductance consists of the implicit CM inductance of primary coil and also the parasitic inductance (L_{decap}) of the decoupling capacitor between the tap of primary coil and source terminal of the cross-coupled pair. Modeling and simulations of such a large distributed RLC network of the decoupling capacitor is time-consuming and grossly inaccurate. Moreover, due to the long distance from the tap to the source of the MOS cross-coupled pair (e.g., in the conventional 1:2 transformer or one-turn inductor for mmW oscillators), several hundred pH of L_{decap} is expected, which is similar in order-of-magnitude to the implicit CM inductance of the one-turn inductor or 1:2 transformer. Despite the use of tail filtering or implicit CM resonance techniques in mmW oscillators, if the L_{decap} is not correctly modelled, the expected CM resonance frequency will be shifted, much degrading the $1/f^3$ corner.

B. Proposed Transfomer w/i Embedded Decoupling Capacitor

Fig. 2(b) shows the proposed transformer with the embedded decoupling capacitor inside. The decoupling capacitor network (the blue part) is placed inside the coil, which makes the tap close to the source of MOS transistor as much as practically possible. Thus, it provides the shortest return path and significantly decreases L_{decap}. Fig. 4 shows details of the embedded decoupling capacitor technique. Fig. 5 shows the study of different injection points (TAP$_{inj1, 2, 3}$) of the embedded
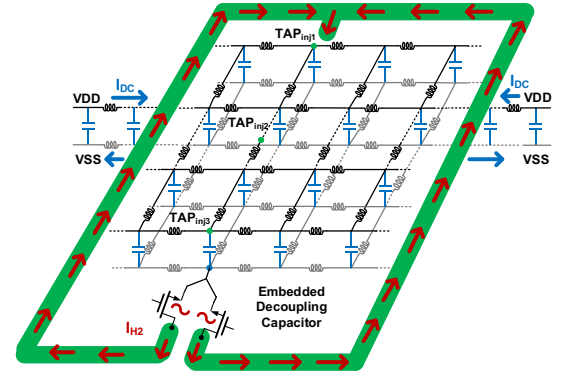

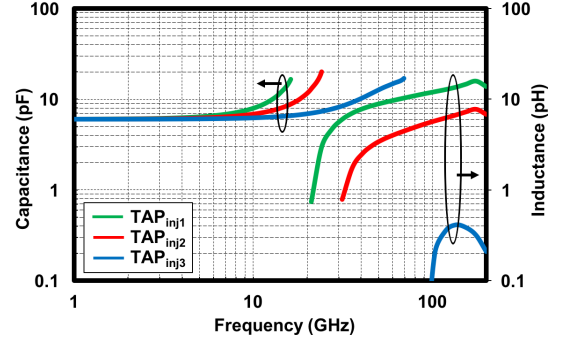Fig. 4. Embedded decoupling capacitor for controlled CM current return path.

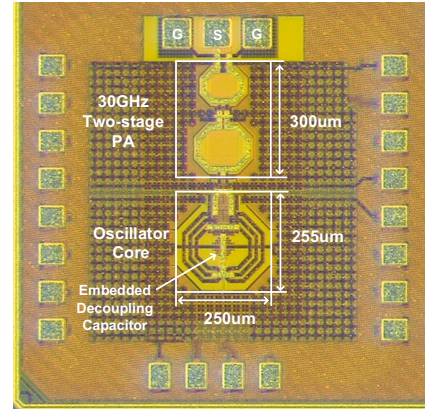Fig. 5. The equivalent capacitance and inductance of different injection points.

Fig. 6. Chip micrograph. The 30 GHz output is probed.

decoupling capacitor which results in different parasitic inductance but the same capacitance. When the tap is placed close to the source at TAP$_{inj3}$, the parasitic inductance can be neglected, and a well-defined return path can be created. It is obvious that placing the embedded decoupling capacitor may degrade the Q-factor of tank. From simulations, if the decoupling capacitor area is less than 25% of the coil's internal area, the degradation would be less than 1 without affecting the inductance and coupling factor.

IV. EXPERIMENTAL RESULTS

The prototype of the proposed 30 GHz frequency generation stage comprising the 10 GHz class-F_{23} oscillator and the two-stage 30 GHz PA is fabricated in TSMC 28-nm LP CMOS. The chip micrograph is shown in Fig. 6 and it occupies a core area of

TABLE I: Performance comparison with relevant state-of-the-art CMOS oscillators

Feature		[7]	[5]	[6]	[13]	[11]	[12]	[4]	This Work	
Feature		Implicit Resonan.	Drain Resistances	Implicit Resonan.	-	-	-	-	Implicit Resonance in Class $F_{2,3}$ and Short-Return Path	
Technology (nm)		28	65	40	65	28	65	65	**28**	
Tuning Range (%)		27	18	25	25	32	10	25	14	
Area (mm^2)		0.19	0.08	0.13	0.13	0.13	0.2	0.13	0.15	
Freq. (GHz)		3.3	3.3	7	7.4	12.7	27.5	57.8	27.3	31.2
Power (mW)		6.8	0.72	10	15	8.3	23*	24*	11.58/22*	13.5/23*
Phase Noise (dBc/Hz)	100k	-106	-94	-102	-98	-80	-72	-72	-83	-80
	1M	-130	-114	-124	-125	-107	-100	-100	-106	-104
	10M	-150	-134	-144	-147	-132	-126	-122	-126	-125
FoM** (dBc/Hz)	100k	-188	-186	-189	-184	-172	-167*	-173*	**-181/-178***	**-179/-177***
	1M	-192	-186	-191	-191	-179	-177*	-181*	-184/-181*	-183/-180*
	10M	-192	-186	-191	-193	-184	-181*	-183*	-184/-181*	-184/-181*
$1/f^3$ Corner (kHz)		200	20	130	700	4000	1200	1000	**120**	**210**

*Including power consumption from the frequency multiplier/first-stage buffer, **FoM=PN-20log(f_{osc}/f_{offset})+10log(P_{DC}/1mW)

0.15mm^2. Phase noise is evaluated using an Agilent E5052B signal source analyzer (SSA) and a 11970A harmonic mixer. The tuning range is from 27.3 GHz to 31.2 GHz (14%) and Fig. 7 shows measured phase noise at 27.3 GHz and 31.2 GHz. At a 27.3 GHz carrier, drawing 11.58 mW from 1 V supply of the main oscillator, it achieves -82.8 dBc/Hz and -126 dBc/Hz at 100 kHz and 10 MHz offsets, respectively. At 31.2 GHz, it achieves -80.2 dBc/Hz and -125.2 dBc/Hz at 100 kHz and 10 MHz offsets, respectively. The supply pushing is only 30 MHz/V. As shown in Table I, which compares this work with other flicker-noise aware designs (albeit at single GHz) as well as mmW CMOS designs, the proposed oscillator achieves 120 kHz and 220 kHz flicker noise corners at 27.3 GHz and 31.2 GHz carriers, respectively, which confirms validity of the proposed approach. This is the lowest $1/f^3$ corner among the > 10GHz oscillators, which usually report > 1MHz, and comparable to those oscillators with flicker-noise-aware designs but at much lower frequencies [6], [7]. To the best of authors' knowledge, it achieves the best PN FoM at 100 kHz offset while maintaining competitive FoM at 1 MHz across its tuning range when compared with >10 GHz oscillators.

V. Conclusions

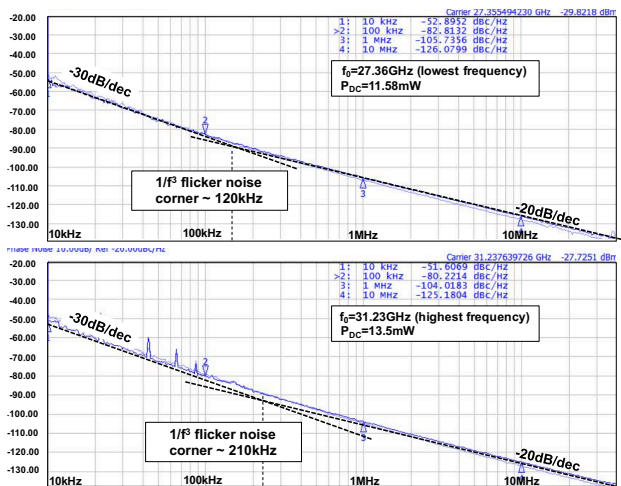A 30 GHz frequency generation stage using a 3rd harmonic extraction and a 2nd/3rd harmonic tuning is proposed. The novel 2nd harmonic resonance technique with careful consideration and control of parasitics in the CM current return path results in state-of-the-art performance with an order-of-magnitude reduction in flicker-noise among >10GHz oscillators. A new understanding of the flicker noise upconversion in advanced CMOS oscillators with consideration of energy balance for low flicker noise is also discussed.

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Fig. 7. Measured phase noise performance at 27.3 GHz and 31.2 GHz.