A 15-µW, 103-fs step, 5-bit Capacitor-DAC-based Constant-Slope Digital-to-Time Converter in 28nm CMOS

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***Abstract*—Instead of using a conventional variable-slope method, this paper proposes a power-efficient capacitor-array-based digital-to-time converter (DTC) in a constant-slope approach. Fringe-capacitor-based digital-to-analog converter (C-DAC) array is used to regulate supply voltage of the slope generator that generates different digitally controlled slopes to a threshold comparator. The proposed DTC consumes only 15 µW from a 1V supply, while achieving fine resolution of 103fs when running at 40MHz. The measured INL and DNL are 0.73/0.35 LSB within a 5-bit range. The DTC achieves the best figure-of-merit of 8.5fJ among state-of-the-art when normalizing the product of power and INL to the product of input frequency and range.**

Keywords—digital-to-time converter (DTC); low-power; low voltage; power-efficient; capacitor-based DAC (C-DAC); constant slope; high resolution; INL; PLL

I. INTRODUCTION

CMOS scaling and configurability of all-digital phase-locked loops (ADPLL) have spurred significant development in its architectures and building blocks. Traditionally, to achieve low in-band phase noise, a fine-resolution time-to-digital converter (TDC) with at least one oscillator period of dynamic range is required [1]. With such a wide range, it is usually one of the most power-hungry building blocks in the ADPLL. Moreover, high linearity is essential in avoiding significant in-band spurious tones. Recent publications show significant interests in the use of a *digital-to-time converter* (DTC) in ADPLLs, e.g., snapshot technique to reduce the TDC detection range [2, 14], dithering reference phases to recover noise regime and to suppress spurs in near integer-*N* channels [3], *etc*. Due to the benefits of high detection gain, recent publications also adopt DTC for the use in subsampling PLLs or ADPLLs to achieve fractional-*N* operation, which require high resolution with wide dynamic range [4, 5]. The dynamic range of DTC can be relaxed using multi-phase outputs from DCO divider [14]. Furthermore, it can be significantly reduced with an assistance of phase interpolator (PI) in the feedback path (e.g., quadrature divider and 4-bit PI can reduce required dynamic range of a 5 GHz oscillator from 200 ps to 3 ps) [5]. Consequently, the design of low-power DTC with fine resolution and good linearity becomes increasingly important for modern frequency synthesizers.

A conventional DTC is based on the delay of inverter/buffer [2]. However, this approach suffers from limited resolution and high-power consumption due to a large number of delay cells. Recent developments of high-resolution DTCs usually concern two main components, *i.e.*, input/output buffers and delay generation part. The input buffer is used to drive the delay generation circuit and the output buffer is used to drive the output load. The delay generation part is digitally controlled to regulate the desired time delay. When comparing different DTC architectures, the main differences are in the delay generation circuits. Another popular method to use is a *variable-slope* method, in which the delay is regulated by a variable voltage ramp which drives a threshold comparator. The slope of the voltage ramp is tuned through tunable capacitances and resistances. Even though fine resolution <500fs can be achieved [4, 7], conventional DTCs based on the *variable-slope* method suffer from poor linearity due to comparator-limited bandwidth and nonlinear relationship between propagation delay and input ramp time [8]. This problem can be suppressed by exploiting the *constant-slope* method, which generates a voltage ramp with a different start voltage. As shown in Fig. 1(a), the slope is maintained and it produces an ideally linear relationship for a constant delay after a threshold comparator. Despite the significant improvement in resolution and linearity, the main power contributor in [8] is the current DAC which consumes over 1mW.

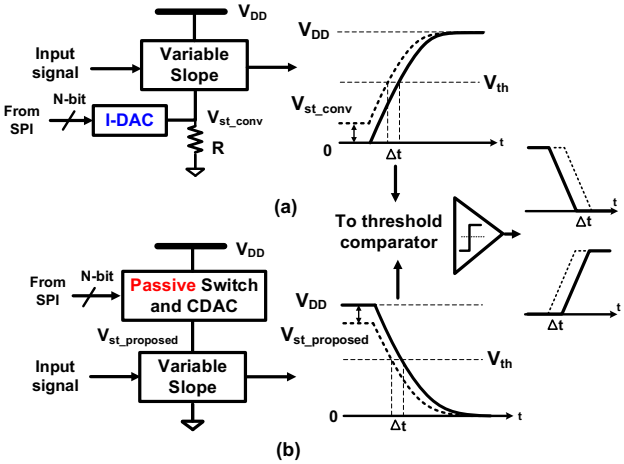

Fig.1. Conceptual diagram of the delay generation circuit in (a) conventional constant-slope DTC using I-DAC [8], (b) proposed passive C-DAC-based constant-slope DTC.

We propose a DTC featuring high resolution and high linearity using a passive DAC in the constant-slope architecture. By exploiting a capacitor-based DAC (C-DAC) as part of the ramp generator, power consumption is significantly reduced while maintaining comparable performance in terms of resolution and linearity. In this work, fringe capacitive array is used as the DAC for regulating the supply of ramp generator with high resolution and good matching. The DAC output further drives the threshold comparator to convert the constant slope into a variable delay with extremely fine resolution, as shown in Fig. 1(b). Similar to the case when C-DAC is applied

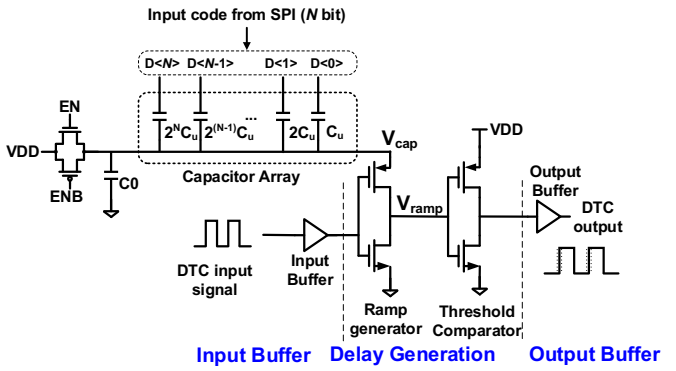

Fig. 2. Proposed power-efficient C-DAC-based digital-to-time converter (DTC)

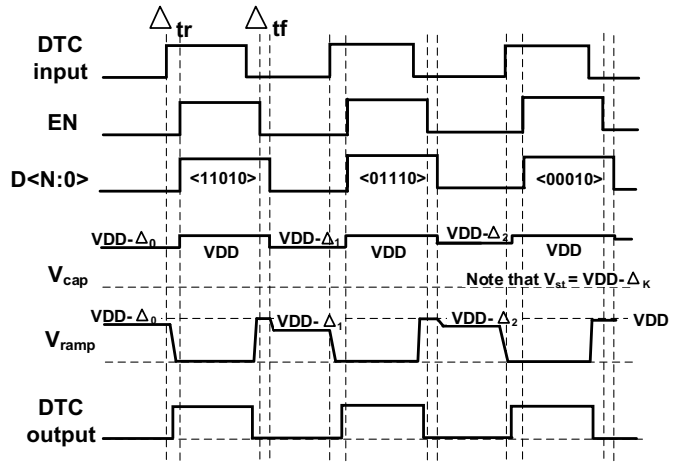

Fig.3. Timing Diagram of the proposed passive C-DAC-based constant-slope DTC at all the corresponding nodes

in Successive Approximation Register Analog-to-Digital Converter (SAR-ADC) [9,10], due to its mostly passive structure, it consumes significantly lower power consumption when compared to any of previous DTC architectures while achieving high resolution with good linearity due to good matching from the layout geometry [10].

II. Design of Proposed Digital-to-Time Converter (DTC)

Due to the constant-slope method and charge sharing technique, the proposed DTC architecture is more suitable for ultra-low power (ULP) and low-voltage (LV) operations. In a constant-slope DTC, the delay generation part is implemented using a ramp generator and a threshold comparator, in which the threshold comparator is realized based on a simple inverter. In contrast, in [8] the ramp generator is composed of a Current-DAC (I-DAC), a resistor, a pulse generator and a current mirror as shown in Fig. 1(a), ultimately consuming considerable amount of power.

In this work, a C-DAC-based constant-slope ramp generator is proposed to modulate the power supply directly, as shown in Fig. 1(b). The output of ramp generator drives the threshold comparator to generate the time delay corresponding to how much the initial voltage deviates from the ideal supply (V_{DD}). Here we use a simple CMOS inverter due to its compact size and low power consumption. The detailed schematic of the proposed DTC is shown in Fig. 2. Since the capacitor array and switch are passive, the inverter cell is the only power-consuming block in the ramp generator. Instead of using the I-DAC and the resistor to generate the start voltage of ramp generator, the proposed design lets the ramp start around the supply voltage (V_{DD}) and lets to regulate the initial voltage (V_{cap}) through the charge re-distribution technique from the fringe-capacitor array. Energy consumed by the switching input digital code and the enable/disable signal for transmission gate are negligible and the main power consumption only flows from the input of the transmission gate to the ramp inverter, which is also known as the charge-sharing technique. The timing diagram of the proposed DTC is shown in Fig. 2 and it operates as follows:

Timing Consideration: Compared to the conventional DTC, there is one extra control signal whose timing should be taken care of. It is the control signal for the transmission gate. Together with the digital control codes, the rising edges of enable signal EN should come after the DTC input's rising edge. Δt_r is the time to allow the ramp inverter output, V_{ramp}, to drop to ground and settle before EN rises. After the transmission gate is enabled, V_{cap} is reset to V_{DD}. The time difference between EN and DTC delay control codes, *i.e.*, D<N:0>, does not require strict timing except that the falling edge of EN should reach the ground before the falling edge of D<N:0>. After the transmission gate is disabled, the charges stored on the capacitors are $(C_0+K*C_u)*V_{DD}$ where C_u is the unit capacitance of C-DAC and K is denotes how many of unit capacitances are chosen. Δt_f is reserved for the transmission gate to be disabled completely. The pulse width for EN and D<N:0> could be less than half of the period. The minimum pulse width is determined by the settling time for the digital control nodes and V_{cap} node. After D<N:0> is reset to zero, the stored charge is shared over C_0+C_a. (C_a is the total capacitance of the capacitor array) and V_{cap} drops to $V_{DD}-\Delta_K$, which is the initial voltage for the ramp. When the next DTC input arrives, the falling edge of V_{ramp} drops from $V_{DD}-\Delta_K$ to ground.

III. Circuit Implementation

The proposed DTC contains two main blocks: the input/output buffers and delay generation block, which consists of the ramp generator and the threshold comparator. In this design, the input buffer is sized relatively larger since it is critical for phase noise contribution. On the other hand, the proposed ramp generator is made up of the transmission gate, the capacitor array and the ramp inverter, in which their designs are discussed below.

1) C-DAC-based Ramp Generator

The size of transmission gate is carefully chosen to minimize its on-resistance and to reduce settling time for V_{cap} so that it does not limit the operating speed of the DTC.

The implementation of capacitor array of small unit values is important to achieve high power efficiency and high accuracy. In this work, similar as to the use in [9], a custom-designed metal-oxide-metal (MOM) capacitor of a small value is used, as shown in Fig. 4. In this design, the unit capacitance is laid out using Metal-2 to Metal-7 with 0.05µm width and 7.2 µm length. The layout extraction reveals a unit capacitance of 6.3fF.

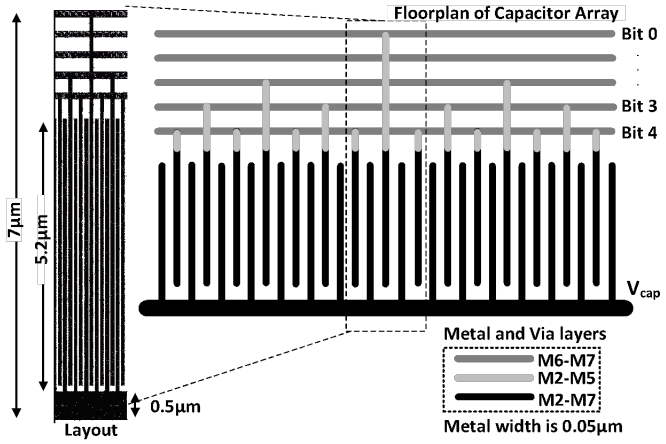

Fig.4. Floorplan and layout of the capacitor array as part of the ramp generator in the proposed DTC

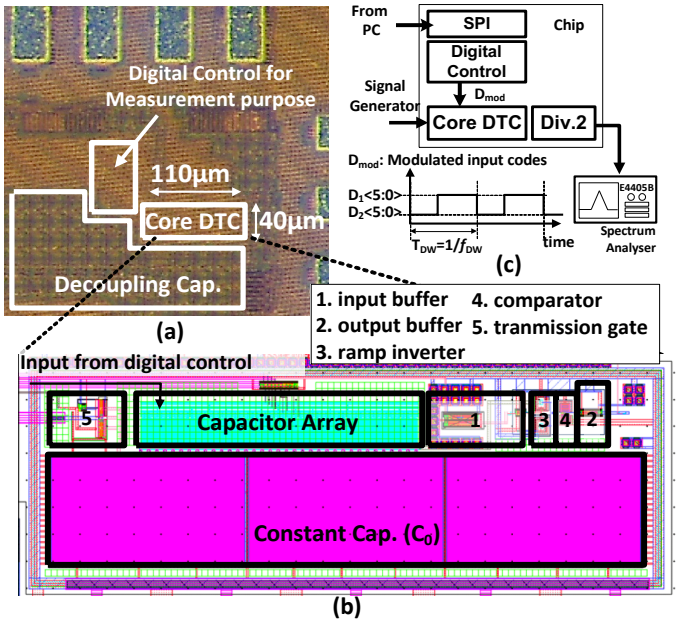

Fig.5. (a) Chip micrograph of the proposed DTC and power consumption of each block (b) layout of core area of the proposed DTC (c) measurement setup

The constant capacitor (C_0) is built as a MOM capacitor from the PDK with a value of 9.43pF. The capacitors occupy most of the core area. The power consumption and area could potentially be even smaller when choosing smaller capacitors since the ratio between the total capacitance from the capacitor array over the constant capacitor value determines the V_{cap} variation range, rather than the absolute capacitor value. The voltage variation range for the V_{cap} is from the minimum initial voltage ($V_{st,min}$) to V_{DD}, whereas $V_{st,min}$ can be determined as:

$$V_{st,min} = \frac{C_o}{C_a + C_o} V_{DD} \quad (1)$$

In the layout, Metal-1 and Metal-2 are not used in C_0 in order to reduce the substrate interference. The ramp inverter size should not be overly large as to avoid large self-parasitic capacitance. Without a cascade structure in the ramp inverter, the proposed DTC is more suitable for low supply voltage. In the layout, guard-ring is used for noise isolation.

2) Threshold Comparator

The size of the inverter is optimized to slow down the input ramp and to cover the desired dynamic range using a relatively larger size. The threshold voltage (V_{th}) of this comparator can be adjusted through sizing of PMOS and NMOS in order to ensure enough margin from $V_{st,min}$. Moreover, the chosen comparator size can provide enough driving capability to its following output buffer.

IV. Experimental Results

To demonstrate the effectiveness of the proposed idea, the proposed DTC has been implemented in TSMC 28-nm LP CMOS. Fig. 5 shows the die microphotograph and chip core layout, respectively. The effective DTC area is 0.004mm^2. When operating at 1.0V supply, it consumes only 15µW when running at 40MHz. Since the supply is common, power breakdown of each building block is derived from simulations. The input buffer dominates more than half of the total power. The transmission gate consumes 7% of power due to one inverter generating the complementary control signal ENB. Ramp inverter and comparator both consume 11% of power.

To measure the DTC nonlinearity, a sensitive frequency domain method used in [12] is employed as shown in Fig. 5 (c). The digital control block is provided to generate periodic digital control codes modulating the DTC delay. The spurious tone level then corresponds to the resolution. Similar to the method in [12], the DTC output is divided by 2, yielding a 20MHz square wave as the output. The spectrum is measured using Agilent E4405B ESA-E. The relation between the spur level and the relative time can be expressed as:

$$spur_h(f_{Div} \pm f_{DW}) = 20\, log_{10}\left(\frac{\tau_h}{T_{CK}}\right) \text{ [dBc]} \quad (2)$$

In which, τ_h is the delay difference between two different control codes D_1<4:0> and D_2<4:0>; T_{CK} is the period of DTC

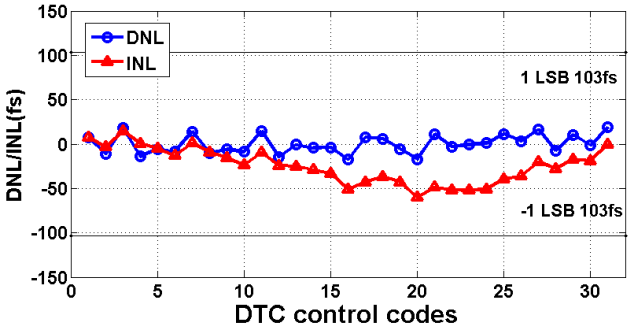

Fig. 6. Measured DNL/INL

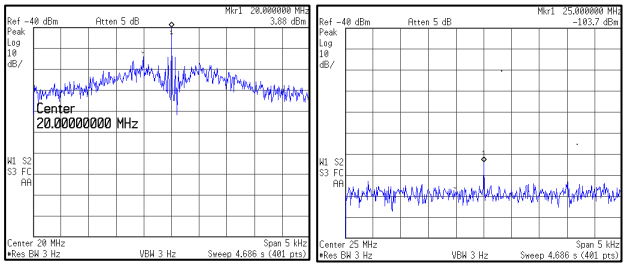

Fig. 7. Measured output spectrum when input frequency is 40MHz and the DTC is being modulated by 1LSB code difference

TABLE I: PERFORMANCE COMPARISON WITH THE-STATE-OF-THE-ART DIGITAL-TO-TIME CONVERTER (DTC)

	[6] ISSCC11	[7] ISSCC11	[4] ESSCIRC14	[8] JSSC15	[13] JSSC16	[11] VLSI06	[2] ISSCC14	This work
Method	Variable Slope	Variable Slope	Variable Slope	Constant Slope (I-DAC)	Interpolation	Variable Threshold	Buffer-based	Constant Slope (C-DAC)
Technology (nm)	65	65	28	65	28	90	40	28
Supply Voltage (V)	1.1	1.2	0.9	1.2	1.1	1.0	1	1.0
Resolution (fs)	4700	241-330	550	19	244	1000	21500	103
Number of bits	5.3	10	10	10	11	6	6	5
INL (fs)	1900	3000	990	64	1200	3200	67600	75
Power (mW)	>0.22@ 48MHz	2.2@ 40MHz	0.5@ 40MHz	0.8+1.0@ 55MHz	19.8@2GHz	N/A	0.0137@ 32MHz	**0.015@ 40MHz**
FoM[1](fJ)	46.8	541.0	22.0	107.7	23.8	NA	21.4	**8.5**

[1] FoM=Power*INL/(Freq*Range), only core DTC is considered

input clock; f_{Div} is the fundamental frequency of the divided DTC output; f_{DW} is the frequency of the code waveform. As shown in Fig. 7, referring to the fundamental frequency at 20MHz, the relative spur level at 5MHz offset frequency is -107.6 dBc when the modulated DTC control codes have a 1 LSB difference. This corresponds to a 104.2 fs delay step. The measured DNL and INL are 0.35 and 0.73LSB with 103fs resolution, respectively, as shown in Fig. 6.

The measured phase noise of the divided DTC output shows an integrated jitter of 1209fs, which is limited by the input buffer as per post-layout simulations. Avoiding the use of cascode devices in the proposed DTC makes it more suitable to operating at a low supply voltage. It is verified through measurements that when operating at 0.76V, which appears to be the lowest ever reported, the DTC consumes only 8.6µA (i.e., 6.5µW). The key performance metrics of the proposed DTC are compared with state-of-the-art DTCs in Table I. It can be observed that the constant-slope DTC can achieve the fine resolution and good linearity. In this work, the proposed DTC maintains such performance while consuming significantly less power. To fairly compare the proposed work with other publications, the INL of the DTC is normalized to the product of input frequency and range as figure-of-merit (FoM). Note that in [8], INL is normalized to the range but power consumption and input frequency have not been included. As a result, the proposed DTC achieves an FoM of 8.5fJ, which appears to be the best to our knowledge. As the very first demonstration of the proposed idea, the range only covers 5 bits, thus limiting its applications to a few cases, such as dithering and PI assisted synthesizer [5]. However, the C-DAC range can be easily extended to more bits, thus showing good potential for widened use in modern low-power frequency generation.

V. CONCLUSIONS

In this paper, we have proposed a high-resolution low-power DTC. When operating at 1V, it achieves 103fs resolution at 15µW consumed power. Benefited from the constant slope operation, the DTC achieves 75fs INL. The proposed DTC makes use of a simple inverter structure with scalable passive capacitor array as a DAC. It can offer high resolution with good linearity while consuming extremely low power which is suitable for the Internet-of-Things (IoT) applications.

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