# Use of Voltage Limits for Current Limitation in Grid-forming Converters

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***Abstract*—Renewable generation interfaced through grid-forming converters are proposed as a replacement for synchronous generators in the power system. However, compared to the synchronous generator, the power electronics converter has a strict limit on the current to avoid overcurrent damage. The grid-forming converter acts like a voltage source, controlling the voltage directly. This conflicts with the operation of the conventional current limit control, which is applied to a current source. The switch between voltage control and current control aimed to impose the current limit leads to synchronization instability. This paper proposes a novel control scheme which can be applied to the grid forming voltage control in order to enforce current limits. The proposed method has been verified through simulation and hardware tests to perform the current suppression while maintaining synchronization stability in voltage control mode.**

***Index Terms*—Grid-forming Converter, Voltage Limit, Angle-Power Curve, Current Limit.**

## I. Introduction

Power generation is moving from conventional fossil fuels dominated synchronous generation (SG), such as thermal power plant, to renewable energy dominated converter-interfaced generation (CIG) such as wind and photovoltaics (PV) in the face of the globally increasing electricity demand and a desire to lessen $CO_2$ emissions. Most of the existing CIG are grid-feeding [1], in that they behave like a current source purely feeding the power into the grid. However, in the transition to the replacement of the SG by the CIG, some of the CIGs have to take the responsibility to form the grid, i.e. to establish the voltage in the grid, thus, they must move to behave as grid-forming, voltage sources [1].

The grid-forming converter applies outer voltage, inner current control to directly control the voltage in terms of both amplitude and phase. Its power or current output is indirectly determined by the voltage difference across the impedance between the converter controlled output voltage and the grid voltage. This differs to the grid-feeding converter, which can directly control the current feeding to the grid, but its output voltage is indirectly determined as a consequence of the assigned current [2]. The synchronization method of the grid-forming converter is based on power feedback [3], instead of voltage [4] as used in the grid-feeding converter. This power synchronization method is analogous to the electromechanical synchronization of the SG, which uses the power balance to determine the phase difference between the EMF and the point of common coupling (PCC) voltage. The implementation of this power synchronization can be as simple as a proportional gain from power to converter frequency, defined as droop control, which is widely used in microgrids [5]. A PID controller for the fast power reference tracking [6,7], or a low pass filter for the inertia and damping emulation [8] are other possible options. The last one is widely recognized as virtual synchronous generator (VSG) control [9-16]. Due to its inertia emulation, and the analogy between its control parameters and conventional power system concepts such as inertia and damping, it appears as the most effective control for the grid-forming converter in the conventional power system. The drawback of the grid-forming converter is the coupled active and reactive power [17], due to the direct voltage control; but this can be alleviated by the inclusion of the virtual impedance [18] or the decoupled voltage control [19,20].

Unlike the SG, which can tolerate overcurrent for a certain time, the converter has a rigid current limit in order to avoid overcurrent damage. Since the grid-feeding converter controls the current directly, it is easy to limit the current for this type of the converter by the means of adding a saturation block at the current reference of the current control [21]. However, for the grid-forming converter, the inclusion of the current saturation would force the converter to work as a constant current source during the period of current excess [22]. In this situation, its terminal voltage loses direct control, and its power output becomes uncontrollable as its value is the product of the constant current and the uncontrolled point of common coupling (PCC) voltage. This breaks the power balance necessary for the power synchronization and the converter loses the synchronization and becomes unstable as consequence [23]. In general, to deal with this a back-up PLL is invoked during this period [3, 22]. Although, the phase remains locked when the PLL is used, the power is still unbalanced in the power synchronization algorithm. In other words, the locked phase from the PLL differs to the phase determined by the power synchronization. Thus, it is a problem to switch back to the power synchronization in the post-fault condition. To avoid this switch between two synchronization methods, some references [24-27] propose that the grid-forming converter should continue to work on power synchronization during the period of the excess current. With this in mind, [24] proposes an adaptive parameter method to slow down the phase movement in order to try to maintain the present power output when the overcurrent occurs . However, the successful operation of this method is

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dependent on the duration time of the overcurrent. Other works propose an additional control loop to suppress the current for the fault ride through of the gird-forming converter. For example, reference [25,26] proposes a phase regulation method to avoid the synchronization instability. Reference [27] proposes a voltage amplitude or EMF re-setting loop to limit the current. Reference [28] proposes to increase the virtual impedance during the fault in order to limit the current. Although these methods [25-28] can maintain the converter stability and limit the current, they need to break from the original control loop and switch to the new additional loop during the fault. This of course degrades the robustness of the converter, compared to the current limitation method in the grid-feeding converter, which only uses a saturation block to limit the current reference and does not change the original control strategy. A less complex and more elegant current limitation method in the grid-forming converter should also only use a simple saturation block and maintain its original control strategy. The references in the grid-forming converter include both the power and EMF, a successful current limit technique should limit both the power and EMF in order to maintain a stable synchronization and at the same time limit the current. It is important to note that the limit of the power is actually the limit of the voltage phase angle.

Therefore, the first contribution of the paper is the analysis of the constraints and possible instability arising from the use of the conventional current limitation methods in the grid-forming converter. A further contribution of this paper is then to propose a voltage limit for the grid-forming converter which ensures that current limits are respected. Moreover since the grid code [29] requires the converter to compensate active and reactive power differently under different grid states, then different selections of values for the current limit in the grid-feeding converter are required. The paper also takes this situation into account and shows how to determine the value for the voltage limit in response to the grid code requirements.

The paper is structured as follows: Section II reviews the grid-forming converter and analyses the possible failure of the conventional current limit on this type of the converter. Section III introduces a novel voltage limitation method for the grid-forming converter in respect to the current limitation. Section IV shows the failure of the conventional current limit via the simulation in Matlab/Simulink. Section V verifies the proposed voltage limitation method via the hardware in-the-loop experiment, while section V draws the conclusions.

## II. Overview of Grid-forming Converter Controls

The control scheme and topology of the grid-forming converter has been extensively described in previous literature and here we only give a quick review for the understanding of the presented content. As shown in Fig. 1, the underlying control of the grid-forming converter is the outer voltage, inner current control (VSC control in Fig. 1), which needs the voltage phase angle and amplitude reference. The outer control in one branch applies the power-to-frequency control (P-f control) in order to determine the phase or achieve synchronization and meanwhile controlling the active power output. The other branch applies the reactive power to the voltage control (Q-V control) or automatic voltage regulation (AVR) to determine the voltage amplitude (EMF) meanwhile sharing the reactive power or supporting the grid voltage respectively. In some topologies, the virtual impedance [30] block is placed between the outer control and the underlying control and is used to shift the voltage output from the EMF in order to decouple the active and reactive power [18], improve the converter stability [31] or reduce the harmonics. For the sake of simplicity, the virtual impedance is not explicitly included in the analysis but could be considered as a part of the line impedance.

The output power from the VSG is determined by the voltage difference between the PCC voltage and the converter output voltage. Defining the EMF as the reference at $0^{o}$ phase,

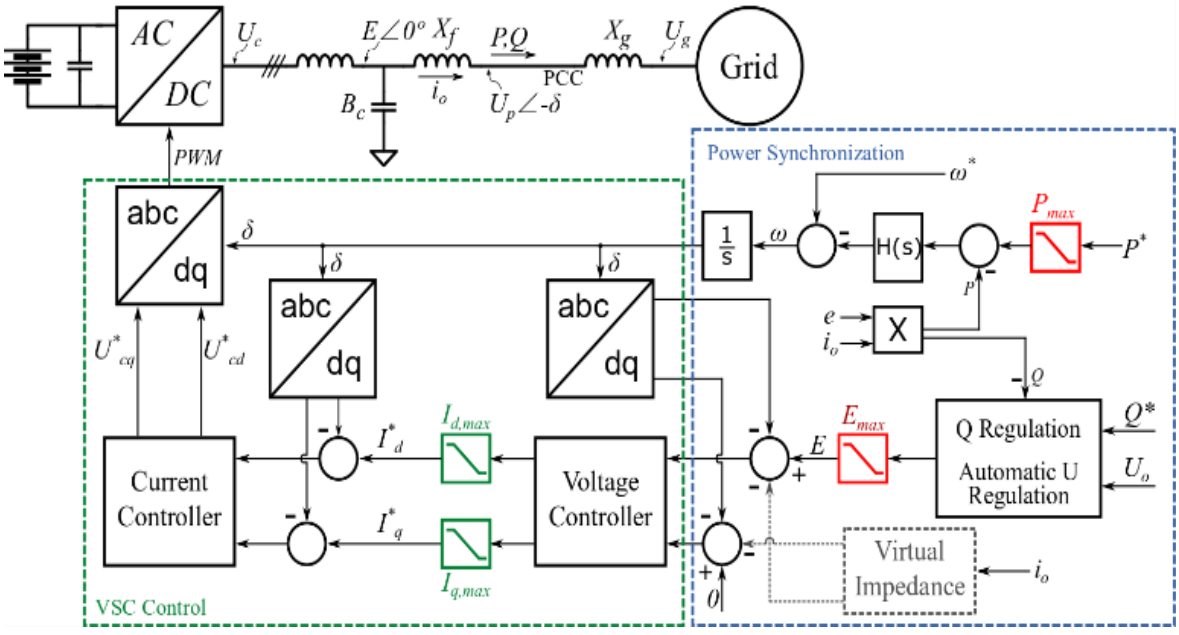



Fig. 1. Grid-forming converter control scheme; $I_{d,max}/I_{q,max}$ is the conventional current limit; $P_{max}/E_{max}$ is the proposed voltage limit.

i.e., $E\angle 0$, then the PCC voltage is defined as $U_P\angle -\delta$. Assuming the outer inductive filter $X_f$ has no resistance, then the power at the PCC can be computed as (1) and (2).

$$P = \frac{EU_P}{X_f} sin\delta \tag{1}$$

$$Q = \frac{E^2}{X_f} - \frac{EU_P}{X_f} cos\delta \tag{2}$$

Since the EMF is the reference at $0^o$ phase, the current at the EMF is decoupled in the synchronous dq-frame and can be computed via the power divided by the EMF as given in (3) and (4) respectively.

$$I_{od} = \frac{U_P}{X_f} sin\delta \tag{3}$$

$$I_{oq} = \frac{E}{X_f} - \frac{U_P}{X_f} cos\delta \tag{4}$$

The grid-forming converter controls the active power $P$ and EMF $E$ directly, so that the phase can be determined as a result from (1). The reactive power is uncontrolled, being the consequence of the determined phase and EMF in (2). Hence the reactive power is coupled to the active power regulation, although some decoupling method can be applied by a proper regulation of the EMF. The converter output current as presented in (3) and (4) is related to the PCC voltage, which is dependent on the grid voltage $U_g$ as shown in Fig. 1. Therefore, the current is uncontrollable which makes it difficult to limit. In general, the current is saturated during the PCC voltage $U_P$ reduction resulting from a fault, e.g. $U_g$ reduction or grid impedance $X_g$ change. Using $U_g$ reduction as an example, the rest of this section analyzes the existing current limit methods for the grid-forming converter.

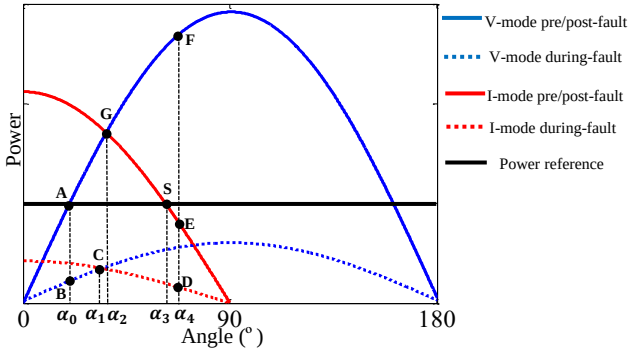



Fig. 2. Power-angle curve: converter operation under conventional current limit

### A. Adaptive power synchronization control

The analysis of the grid-forming converter operation is based on the angle-power curve [22] as shown in Fig. 2, where the solid and dashed blue lines represent the operation under the nominal and grid fault voltage respectively, when the converter is working in the voltage source mode. The solid and dashed red lines represent the operation under the nominal and fault grid voltage respectively, when the converter is working in the current source mode.

Initially, the operating point is stable at A with phase $\alpha_0$ in the pre-fault line, where the reference power and converter output are balanced. If there is no current limit, at the beginning of the $U_P$ reduction, the operation of the converter moves from the solid blue line to the dashed blue line and its operating point moves to B since the phase angle cannot experience a step change. $I_{od}$ reduces as shown by (3), but $I_{oq}$ increases as represented in (4). As long as the reference power is greater than the converter output power, the converter virtual speed accelerates with the phase increasing and its operating point moves along the dashed blue line. The increase in the phase $\delta$ increases both $I_d$ and $I_q$. After a certain time, the current would be greater than the limit value resulting in damage to the converter. It can be seen from Fig. 2 that the operating point moves through the operating point C with phase $\alpha_1$, at which corresponds to the point when the current is exactly saturated. Furthermore, if the fault continues, the phase will increase continuously until it exceeds $90^o$ resulting in the converter working in the unstable region. In this process, the fault clearing time is critical. If the fault is cleared before the phase reaches $\alpha_1$, then the current will not be excessive. Based on this characteristic, the adaptive power synchronization control [24] has previously been proposed to slow down the rate of the phase increase by enlarging the damping effect in the control.

However, this method is constrained by the initial operating point of the converter. If the initial phase is close to the critical phase $\alpha_1$, the tolerated fault cleaning time will be shorter. In the worst case, the converter is working in the heavy loading situation with the initial phase greater than $\alpha_1$, in which case the current would exceed the limit at the instant of the fault occurrences. In this situation, the adaptive power synchronization control would be ineffective, since the phase continues to increase leading to the current increase as a consequence.

### B. Current limit for grid-forming converter

A current limiter placed on the current reference of the inner current control is the conventional method used to limit the current (as highlighted in green blocks in Fig. 1). In this case, during the fault, after the phase exceeds $\alpha_1$, the operation of the converter changes to the current mode and moves along the dashed red line. Since the reference power is still greater than the converter output, the converter virtual speed keeps accelerating and its phase increases continuously, but now the current is limited.

If the fault is cleared before the phase reaches $\alpha_2$, the converter operating point returns to the solid blue line in the stable region and finally stabilize at the initial point A. If the fault is cleared when the phase has increased to the range between $\alpha_2$ to $\alpha_3$, the actual operation cannot go back to the solid blue line due to the current limit, but will instead start moving along the solid red line in the current mode. Since in this range the converter output power is greater than the reference power, the converter decelerates with the operating point moving to G, and then its operation returns to the solid blue line and finally stabilizes at the initial point A. However, if the fault is cleared after the phase exceeds $\alpha_3$, the converter loses synchronization and becomes unstable. This is because although the operation of the converter moves along the solid red line, it continues to accelerate as beyond this point the converter output power is less than the reference. The resulting increase in phase reduces output power further and instability occurs. Note that the inclusion of the current limiter

extends the tolerance of the fault cleaning time in terms of the maximum allowable phase from $\alpha_1$ to $\alpha_3$.

### C. Use of Backup PLL

As described above, the continued use of the power synchronization with the saturated current limit has a problem in terms of synchronization stability. A backup PLL has been proposed to be used in this context to avoid such synchronization instability [3]. The PLL can lock the phase at the original, for example at $\alpha_0$ in Fig. 2. However, the phase resulting from power synchronization control, due to the power unbalance, continues increasing and departs from the phase locked by the PLL. This presents a difficulty in switching back to power synchronization. If the fault is cleared before the phase from the power synchronization exceeds $\alpha_2$, then the operation can move back to the voltage mode and stabilize back at point A. Switching back from the PLL to power synchronization when the phase exceeds $\alpha_2$, would cause a peak power with overcurrent. For example, the phase could move to $\alpha_4$ in the power synchronization, although the operating point was at B under the action of the PLL. In this case, when it switches back to the power synchronization after the fault is cleared, the operating point experiences a step change to point F with a peak power and overcurrent. Therefore, although the backup PLL can maintain a stable synchronization with limited current, it requires more strict fault cleaning times than the pure power synchronization method with current limiter.

To conclude, a successful current limitation of the grid-forming converter should not only limit the current but also maintain a stable synchronization with a proper phase, i.e. $\delta \leq \alpha_2$ in Fig. 2.

## III. Voltage limitation Control

In the grid-feeding converter, the use of the conventional current limit block in the converter current control loop can effectively and stably saturate the current for any time duration. However, from the above analysis, the use of this method on the grid forming converter is constrained in terms of the duration time of the saturated current operation if instability is to be avoided. This is because the input reference for the grid-feeding converter is the current, for which of course the current limit is directly valid, while on the other hand, the input reference for the grid-forming converter is the voltage phase angle and amplitude. Essentially the control on the current leaves the voltage uncontrollable and leads to the error in the voltage reference. Consequently, the voltage error accumulation makes the converter lose its synchronization stability. To avoid this situation, an effective current limitation method for the grid-forming converter should be based on its reference voltage. This section proposes such a method, namely a voltage limiter and then provides a method for the selection of the limitation value corresponding to the current limitation value under different grid states and in accordance with grid code requirement.

### A. Voltage limit for grid-forming converter

The objective of the voltage limitation is still to limit the current. When the current is controlled to be fixed, the converter output voltage would be automatically changed as a consequence of this current flow to the PCC point. Conversely if the converter output voltage can be actively controlled to be the same value, then the current would be automatically changed to be the desired value.

Defining the current limit in the dq-frame as $I_{d,max}$ and $I_{q,max}$. It should be noted that $I_{d,max}^2 + I_{q,max}^2$ should be a constant value. The current should be limited at the converter terminal. The output current is the sum of the converter terminal current and the capacitor current. If the resistance of the capacitor can be neglected, then the capacitor current is purely reactive in the q-axis. Thus, the output current during the current limitation can be obtained as.

$$I_{od} = I_{d,max} \tag{5}$$

$$I_{oq} = I_{q,max} + EB_c \tag{6}$$

Rewriting (4) as (7).

$$E = I_{oq}X_f + U_P cos\delta \tag{7}$$

Substituting (6) into (7) yields the relationship between the saturated voltage magnitude and the saturated current.

$$E_{max} = \frac{I_{q,max}X_f + U_P cos\delta}{1 - X_f B_c} \tag{7}$$

Considering $U_P cos\delta = \sqrt{{U_P}^2 - {U_P}^2 sin^2\delta}$. Substituting (3) and (5) into (7) obtains:

$$E_{max} = \frac{I_{q,max}X_f + \sqrt{{U_P}^2 - {I_{d,max}}^2 {X_f}^2}}{1 - X_f B_c} \tag{8}$$

From (8), an increase in the active power limit, $I_{d,max}$, reduces the value of the term $\sqrt{{U_P}^2 - {I_{d,max}}^2 {X_f}^2}$, and also reduces the value of $I_{q,max}$. Hence, the increase in $I_{d,max}$ reduces the maximum voltage amplitude, $E_{max}$. Note, the condition for the stable solution in (8) is $U_P \geq I_{d,max}X_f$, which restricts the maximum value of the active current in the d-axis. Otherwise, it would lead to the voltage instability detailed in [2].

The voltage amplitude limit is set to be $E_{max}$ from (8), while the voltage phase limit is related to the converter power reference. Thus, the setting of the power limit would help limit the voltage phase.

The power at the saturated voltage with saturated current can be easily obtained as:

$$P_{max} = E_{max} I_{d,max} \tag{9}$$

Referring to Fig. 2, the power at point G is the maximum power $P_{max}$ corresponding to the phase limited to $\alpha_2$ in the nominal grid voltage case.

### B. Voltage limit under different situations

The current limit in the grid-feeding converter varies with the change of grid state. Correspondingly, the voltage limit should also be different for different states of the grid.

In the grid-forming converter, the output power/current is coupled. Defining $I_m$ as the converter current amplitude limit. When the grid voltage works at the nominal, the converter output voltage is nominal, $U_0$. In this case, the maximum dq component currents with the corresponding maximum phase can be solved from a set of equations (10~12).

$$I_{d,max,0} = \frac{U_0}{X_f} sin\delta_{max,0} \quad (10)$$

$$I_{q,max,0} = \frac{U_0}{X_f}(1 - X_f X_c - cos\delta_{max,0}) \quad (11)$$

$$I_{d,max,0}^2 + I_{q,max,0}^2 = I_m^2 \quad (12)$$

The power limit in this case can be easily obtained.

$$P_{max,0} = \frac{{U_0}^2}{X_f} sin\delta_{max,0} \quad (13)$$

Referring to (3), a decrease in the grid voltage would increase the phase if the current in d-axis is a fixed value. Then, at the instant that the grid voltage returns to the nominal, the increased phase leads to a excessive transient power/current with risk of damage to the converter. Therefore, the obtained phase value $\delta_{max,0}$ from (10~12) is the maximum boundary for the phase of the grid-forming converter. On the other hand, the current in d-axis cannot be a fixed value and should be varied with the grid voltage changes as indicted by (14).

$$I_{d,max} = \frac{U_P}{X_f} sin\delta_{max,0} = \frac{U_P}{U_0} I_{d,max,0} \quad (14)$$

The reduction of the active current gives more freedom to increase the reactive current for the grid voltage support.

$$I_{q,max} = \sqrt{I_m^2 - I_{d,max}^2} \quad (15)$$

Then the EMF limit can be obtained by substituting (14) and (15) into (7) and the power limit can be obtained by substituting (15) and (16) into (9).

$$E_{max} = \frac{I_{q,max} X_f + U_P cos\delta_{max,0}}{1 - X_f B_c} \quad (16)$$

$$P_{max} = \frac{I_{q,max} X_f + U_P cos\delta_{max,0}}{1 - X_f B_c} \cdot \frac{U_P}{U_0} I_{d,max,0} \quad (17)$$

Fig. 3 power-angle curve illustrates the proposed voltage limit method during the above situation, where the solid and dashed blue curve represent the constant voltage operation with voltage at nominal and at $E_{max}$ in (16) respectively. The solid and dashed red curve is the constant current operation with the current limit $I_{d,max,0}$ in (10) and $I_{d,max}$ in (14) respectively. Initially, the grid voltage is nominal, and the converter output power is balanced with its reference at the operating point A. At the instant of the fault, the voltage limit is changed with the grid voltage dip and the converter works on a new operating curve (dashed blue line) starting at point B with its $E_{max}$ from (16). Meanwhile, the maximum reference power moves down from the purple line computed from (13) to the gray line determined from (17), in order to maintain the maximum allowable phase to be the constant $\delta_{max,0}$ and the maximum allowable current at $I_{d,max}$. Since the reference power is limited by the maximum power but still greater than the converter output power, the converter accelerates until stabilizing at operating C. When the fault is cleared, the operating point changes to point D at the maximum power (purple line) with saturated current (solid red line) in the nominal situation. Now the reference power is below the maximum power and the converter output power, and the converter decelerates until its operating point moves back and stabilizes at point A.

When the grid voltage drops to less than, for example, 0.5 pu, according to the German grid code, the converter should maximize its reactive power for the grid voltage support, i.e. $I_{d,max} = 0, I_{q,max} = I_m$. Substituting these conditions into (3), (9) and (8) obtains the maximum phase, power and EMF.

$$\delta_{max} = 0 \quad (18)$$

$$P_{max} = 0 \quad (19)$$

$$E_{max} = \frac{I_m X_f + U_P}{1 - X_f B_c} \quad (20)$$

In this case, during the fault, the maximum power becomes 0 W and the operating point moves from B to O in Fig. 3. Note, the current operation curve overlaps with the x-axis, due to $I_{d,max} = 0$, and the cross point between the converter current operation and voltage operation now is O. The converter only feeds the maximum reactive power. After the fault, the converter works along the solid blue curve from O and stabilizes to A.

Note, in order to safely ride through the asymmetric fault, the voltage limitation picks the lowest value of the three phase PCC voltage, $U_P$. The symmetric three phase fault presents the worst case in terms of voltage reduction when ompared with the asymmetric fault. Thus if , the voltage limitation is effective for this worst case then it has the ability to handle other asymmetric fault cases. Of course, the current in the asymmetric fault would have a larger suppression which may even be below its current rating. This could be avoided by including negative-sequence or/and zero-sequence voltage control loops, with the proposed voltage limitation used to limit the positive-sequence voltage control loop. Full analysis of this aspect is beyond the scope of this paper and remains to be addressed in future work. In this paper, we solely apply a positive-sequence voltage control loop, with $U_P$ equal to the lowest value of the three phase PCC voltages.

The voltage limit is set only as a saturation block in the power reference and EMF reference of the grid-forming converter (red blocks highlighted in Fig. 1) and the rest of the control remains the same as the original. In the different situations exposed, the limiting value changes as follows: In the nominal PCC voltage case, the value of the voltage limit is set according to (13); in the reduced PCC voltage case, it is set according to (16)(17); in the extreme case, it is set according to (19)(20).

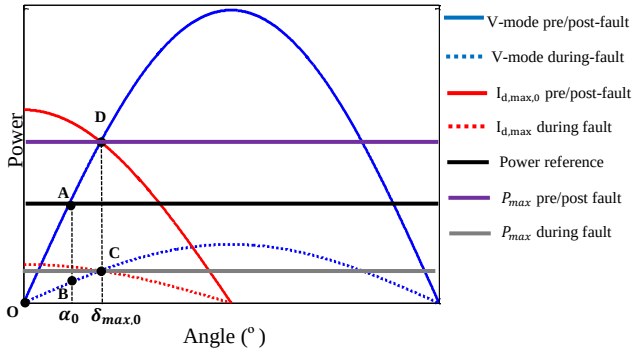



Fig. 3. Power-angle curve: Converter operation under proposed voltage limit

## IV. Results for Failure of Current Limitation

The failure of the conventional current limitation methods of the grid-forming converter reviewed in Section II has been validated via simulation in Matlab/Simulink using the EMT model of the converters but has not been validated in hardware experiment, to avoid the overcurrent damage on converter. The VSG method is used for the power synchronization of the grid forming-converter, although other methods could also be used. The converter applies the automatic voltage regulation for the voltage support. The converter parameters and control settings are given in Table I.

TABLE I
GRID-FORMING CONVERTER SETTINGS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| **PWM** | 1350 | **Sampling time** | 14.8e-6 s |
| **Current limit $I_m$** | 7 A | **Inner filter inductance** | 33 mH |
| **Nominal voltage $U_0$** | 100 V | **Filter resistance** | 0.12 Ω |
| **Frequency** | 50 Hz | **Filter capacitance** | 80 μF |
| **AVR gain** | 0.5 | **Outer filter inductance** | 30 mH |
| **VSG Inertia** | 2 | **Line inductance** | 5 mH |
| **damping** | 80 | **Line resistance** | 2 Ω |
| **Current controller P/I** | 66/326.6 | **Voltage controller P/I** | 0.028/6.31 |

The effectiveness of the conventional current limit depends on the duration time of the saturated current and the initial position of the operating point. In order to trigger the failure of the conventional current limit, the converter is purposely set to work in a heavy loading condition and the duration of the fault is allowed to last for a sufficient time. The system experiences a power reference step change from 0 W to 800 W at 1 s, a grid voltage decreases from 100 V to 20 V at 2 s and then recovers at 3 s. Note, at 3 s, not only does the grid voltage return to the nominal, the grid-forming converter also reverts power synchronization control without a current limit, i.e. operation according to the solid blue line in Fig. 2. This is in order to show the instability resulting from the change in operation. Fig. 4 presents results for the following FRT methods:

1). The grid-forming converter remains working on power synchronization as a voltage source, without imposing the current limit, i.e. defined as "power synchronization no current limit";

2). The grid-forming converter remains working on power synchronization, with the current limit imposed, i.e. defined as "power synchronization + current limit";

3). A backup PLL is enabled during the fault, and the control reverts back to the VSG synchronization after the contingency, i.e. defined as "power synchronization with backup PLL + current limit".

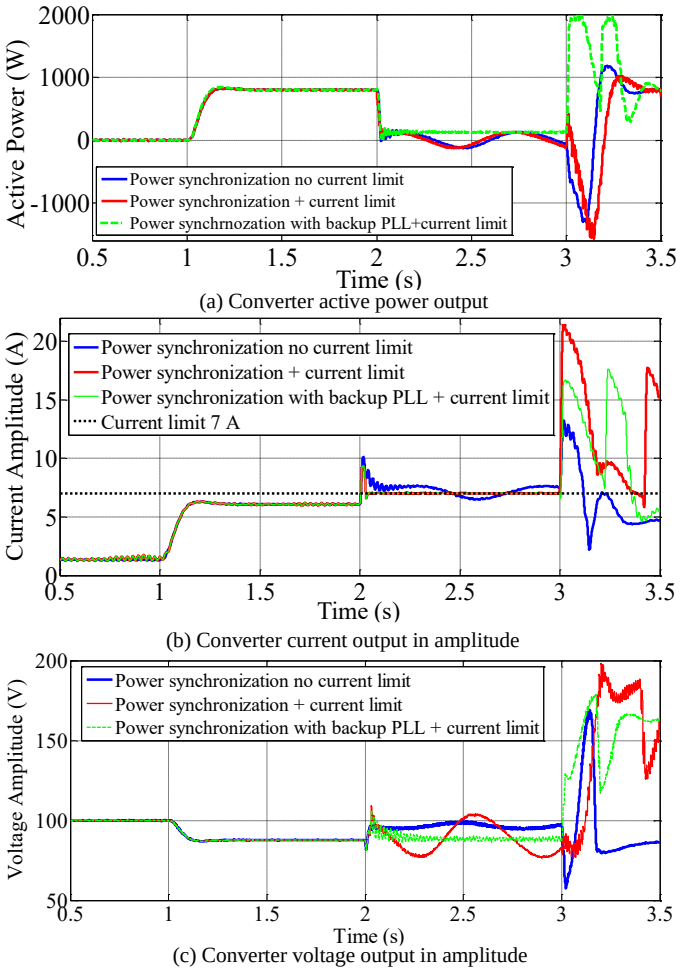



Fig. 4. Simulation result: Current limit failure in grid-forming converter, the power reference changes to 800 W at 1 s, the grid voltage dips to 0.2 pu at 2 s and recovers to 1 pu at 3 s.

It can be seen in Fig. 4 that at the instant of the contingency, 2 s, the power drops corresponding to the operating point moving from A to B in Fig. 2. Without the current limit, due to the reference power being greater than the real power, the converter is accelerating, and the operating point moves along the dashed blue line. After point C in Fig. 2, the VSG is in an overcurrent state as shown in Fig. 4 (b). Since the fault is not cleared in time, when the operating point phase exceeds $90^o$, the system becomes unstable as shown in Fig. 4 (a). On the other hand, with the current limit, the operating point turns moving along with dashed red line after point C. Thus, the current is limited at maximum 7 A. But because the VSG system is still accelerating, the angle keeps increasing and the active power output oscillates as seen in Fig. 4 (a). After the contingency, as aforementioned, due to the uncontrolled phase, it inevitably has a transient power peak with associated current peaks. The backup PLL in this case can lock the phase at the operating point C in Fig. 2 so that the current is limited meanwhile the power is stable as shown in Fig. 4. However, the phase VSG from the swing equation emulation keeps increasing and is not equivalent to the phase from the PLL. Therefore, without a seamless switching, it leads to a transient power peak when it reverts back to the power synchronization

as shown in Fig. 4. From these tests, the conventional current limit in the grid-forming converter has been shown to have problems in terms of the synchronization instability.

It can be seen from Fig. 4 (a) that at the instant of the fault clearance, power synchronization control with and without current limit has a similar response in terms of active power.. This indicates that the angle and active current between these two cases currently are similar. However, due to a higher converter output voltage as shown in Fig. 4 (c), the transient current of the "power synchronization + current limit" at this time is higher and presents a high reactive component.

## V. Hardware Validation of Proposed Voltage Limitation under Symmetric Faults

The proposed voltage limitation method has been validated via the hardware-in-the-loop experiments using an OPAL-RT platform. The hardware set-up is shown in Fig. 5, where the grid is emulated as a voltage-controlled voltage source converter. The parameters of the tested grid-forming converter are taken from Table I, in the same way as in the Matlab/Simulink tests. The hardware experimental tests verify the proposed voltage limitation under different grid states corresponding to the limit sets in (16,17) and (19,20) respectively.

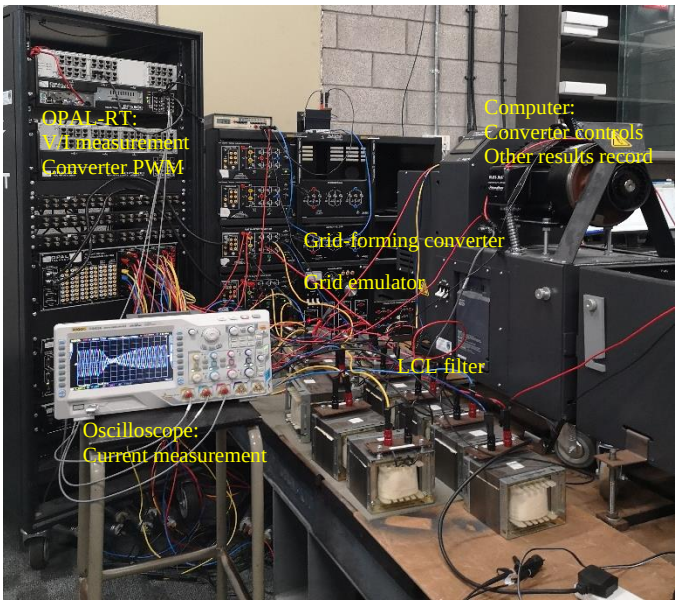



Fig. 5. Hardware experiment set-up

The proposed voltage limit has constraints on the duration time of the saturated current or the initial position of the operating point. Thus, for the different grid states, the setting of the voltage limits is different. Correspondingly, the control is tested under grid voltage dips of 0.5 pu and 0.2 pu separately.

The current limit $I_m$ for the converter is 7 A and the nominal voltage $U_0$ is 100 V. Substituting these into (10~12) gives the initial maximum current in d-axis, $I_{d,max,0} = 6.993\,A$, and the maximum allowable phase, $\delta_{max,0} = 0.6634\,rad$. Since the line impedance between the PCC voltage and the grid voltage has resistance, there is an interaction between the PCC voltage and the current due to the voltage drop. Table II records the PCC voltage under different grid states as well as the corresponding voltage limit computed from either (16,17) or (19,20).

TABLE II
Voltage Limit at Different Grid State

| Grid state | State 1 $U_0 = 100\,V$ $P=0\,W$ | State 2 $U_0 = 100\,V$ $P=800\,W$ | State 3 $U_0 = 50\,V$ $P=690\,W$ | State 4 $U_0 = 20\,V$ $P=0\,W$ |
|---|---|---|---|---|
| $U_p\,(V)$ | 100 | 105.8 | 57.9 | 24.1 |
| $E_{max}\,(V)$ | 100 | 100 | 113.6 | 102.8 |
| $P_{max}\,(W)$ | 980 | 1074 | 690 | 0 |

### A. Symmetric fault experiment Test 1: moderate voltage dip

The first test verifies the proposed voltage limit under a moderate voltage dip corresponding to the set of the voltage limits in (16,17). The system experiences a power reference step change from 0 W to 800 W at 1 s, a grid voltage decrease from 100 V to 50 V at 2 s and then recovers at 3 s. Fig. 6 presents the active power, phase angle between the converter output and PCC voltage, and voltage amplitude, where the PCC phase is measured via a PLL. Fig. 7 presents the converter current in response to fault.

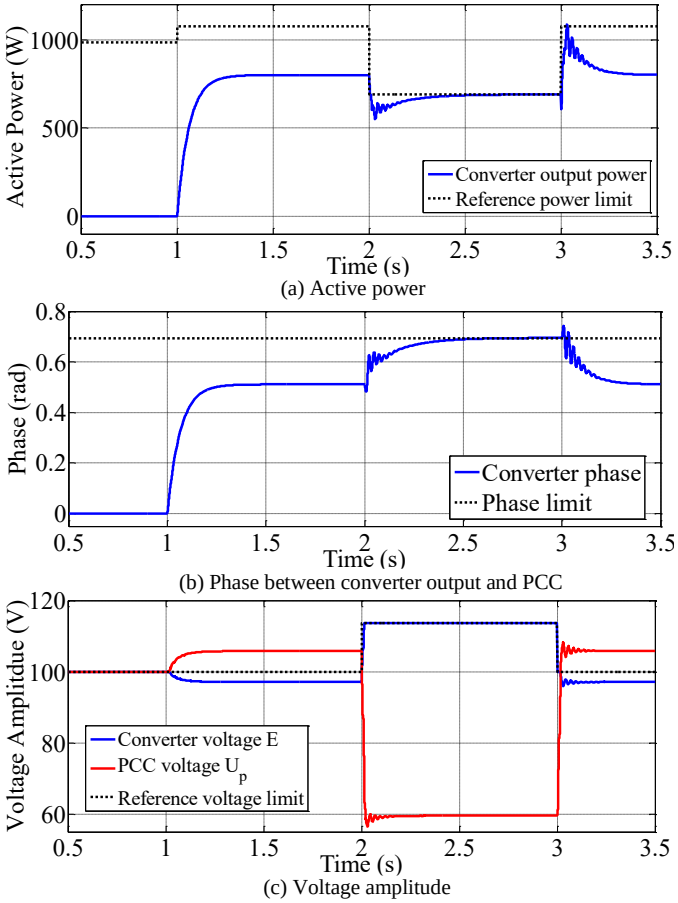


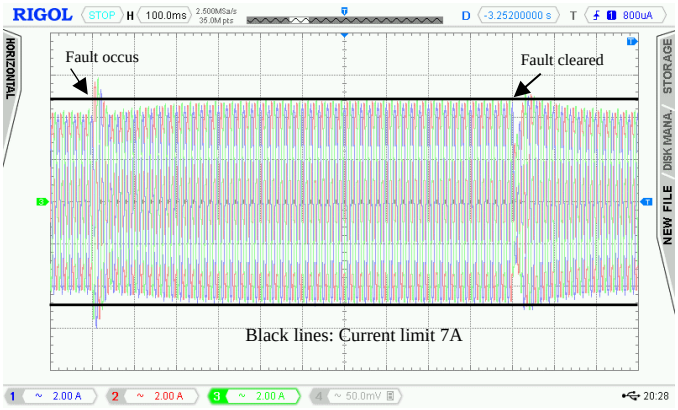

Fig. 6. Test 1: Voltage limit validation in a moderate symmetric voltage dip, the power reference changes to 800 W at 1 s, the grid voltage dips to 0.5 pu at 2 s and recovers to 1 pu at 3 s.

It can be seen in Fig. 6 (a) that at the instant of the contingency, 2 s, the power drops, corresponding to the operating point moving from A to B in Fig. 3. According to (16) and (17), the reference power limit moves from the purple line to the gray line and the reference voltage limit in Fig. 6 (c) increases from the nominal value to 113.6 V. Note, the

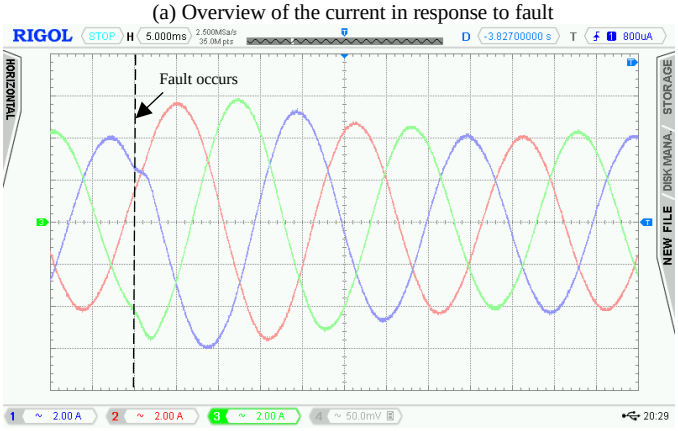
reference voltage from the AVR control is 100+(100-57.9)×0.5=121.05 V. Since the reference power is greater than the converter output power, the converter accelerates and the phase increases as shown in Fig. 6 (b) until it reaches its maximum allowable phase $\delta_{max,0} = 0.6634$ rad, corresponding to the converter stabilizing at operating point C in Fig. 2. The system is stable and can continuously run during the fault. At 3 s, the fault is cleared, and the grid voltage recovers. The operating point experiences a step change from C to B hitting the updated maximum power reference (purple line) as shown in Fig. 6 (a) and then moves back to A with the power and phase recovering to the initial values.

Fig. 7 shows the converter current in response to fault. At the instant of fault occurrence, there is a transient peak current because the converter voltage cannot instantly change and grid voltage reduction results in a large reactive current as indicated by (4), i.e. $I_{oq}$ increases with $U_P$ reduction if other parameters remain fixed. After the voltage measurement detects the change in PCC voltage, the voltage limitation changes its state from State 1 in Table II to State 2 and then the current is limited at 7 A in one cycle as shown in Fig. 7 (b). At the instant of fault clearance, a sudden increase in the grid voltage leads to the charge of the filter capacitor of the grid-forming converter, thus, the current in first cycle after fault reduces and then increases in Fig. 7 (c), due to the phase now being at its maximum value as shown in Fig. 6 (b). Correspondingly, the converter output power at 3 s has a dip and then step changes to the maximum allowable value as shown in Fig. 6 (a).

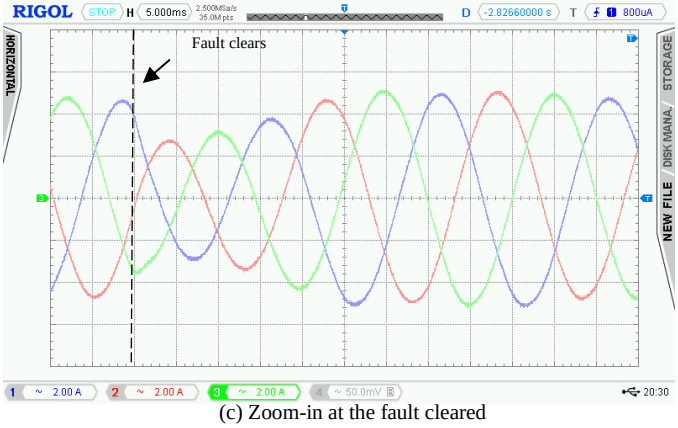
In this test, the voltage limit effectively suppresses the current and outputs the maximum active power during the fault.




(a) Overview of the current in response to fault




(b) Zoom-in at the fault occurrence




(c) Zoom-in at the fault cleared

Fig. 7. Test 2: Current in response to a severe symmetric voltage dip.

### *B. Symmetric fault experiment Test 2: severe voltage dip*

The second test verifies the proposed voltage limit in a severe voltage dip corresponding to the setting of the voltage limit in (19,20). In this test, the system experiences the same change as in the Group 1 test. Fig. 8 presents the active power, reactive power, and voltage amplitude. Fig. 9 presents the converter current in response to fault.

It can be seen in Fig. 8 (a) that during the fault from 2 s, the reference power is limited to be 0 W (State 4 in Table II) and the operating point moves from B to O in Fig. 3. The reactive power output is maximized as shown in Fig. 8 (b) with the saturated reactive current as shown in Fig. 9 (a). After the fault clearance, the system recovers with its operating point back to A. In this test, the voltage limit effectively

suppresses the current and outputs the maximum reactive power during the fault.

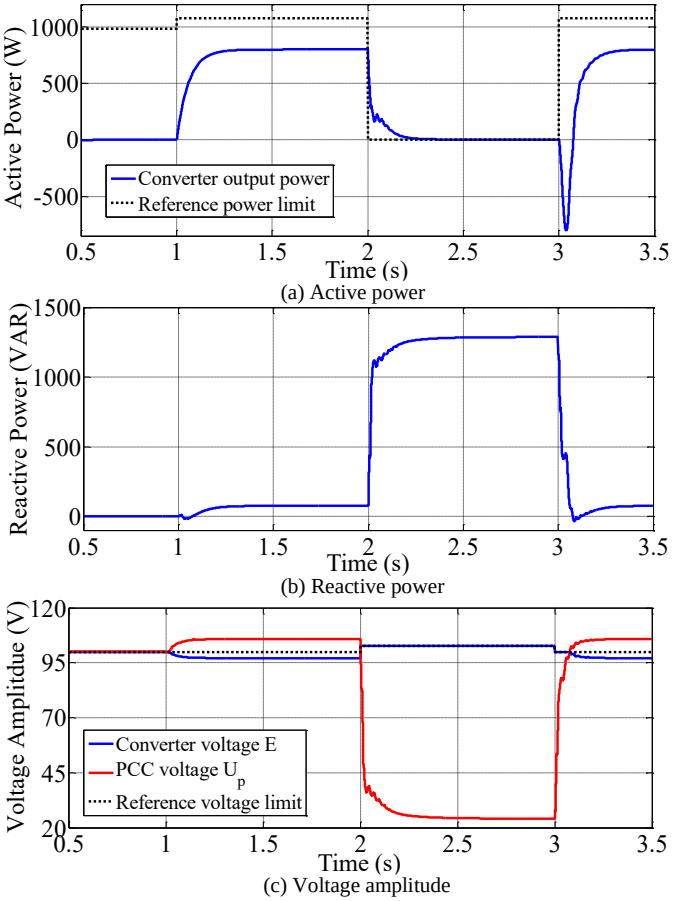



Fig. 8. Test 2: Voltage limit validation in a severe symmetric voltage dip, the power reference changes to 800 W at 1 s, the grid voltage dips to 0.2 pu at 2 s and recovers to 1 pu at 3 s.

Fig. 9 shows the converter current in response to the fault. At the instant of fault occurrence, there is a transient fault current as shown in Fig. 9 (b), which is similar with that in Fig. 6 (b) but has a higher peak due to the lower grid voltage. This transient current again can be limited at 7 A within one cycle. Because in this test during the fault the converter outputs 0 W power, at the instant of fault clearance, there is a significant reverse power from the grid to charge the capacitor. This is why there is a power dip in Fig. 8 (a) and this continues for one cycle, and then the converter starts to generate power. Hence, a significant phase shift can be seen in Fig. 9 (c).

In this test, the voltage limit effectively suppresses the current and outputs the maximum reactive power during the fault. The transient overcurrent in these two tests at the instant of the fault occurrence and clearance lasts only for 1, cycle which can be tolerated by the converter according to [32][33], thus, it would not damage the converter.

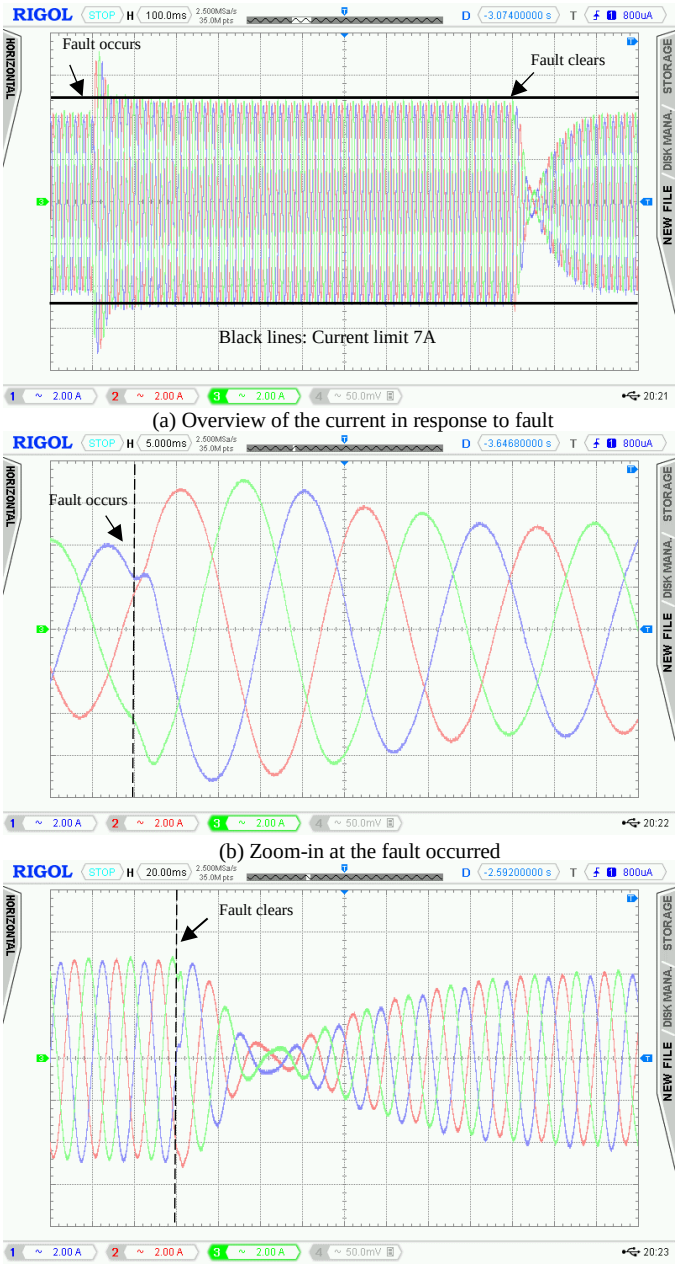



Fig. 9. Test 2: Current in response to a severe symmetric voltage dip.

## VI. Simulation Validation of Proposed Voltage Limitation Under Asymmetric Faults

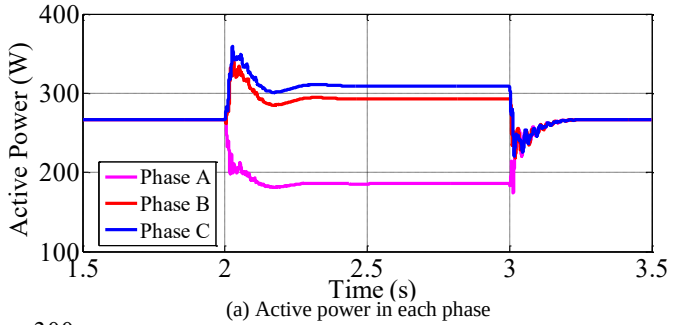
The proposed voltage limitation has been validated for the symmetric fault, this section aims to verify its effectiveness under asymmetric faults. The tests are performed in Matlab/Simulink simulations only, since the grid emulator in the hardware set-up cannot output unbalanced voltage. The grid-forming converter solely uses the positive-sequence voltage control but no negative-sequence and zero-sequence voltage control, so that $U_P$ in the voltage limitation is taken as the lowest value of the three phase PCC voltages. Test 1 and Test 2 are repeated but the grid voltage dip only occurrs in phase-A at 2 s while phase-B and phase-C remain fixed in each test. Other conditions remain the same. Table III shows the voltage limit for these two asymmetric faults.

TABLE III
VOLTAGE LIMIT AT ASYMMETRIC FAULTS

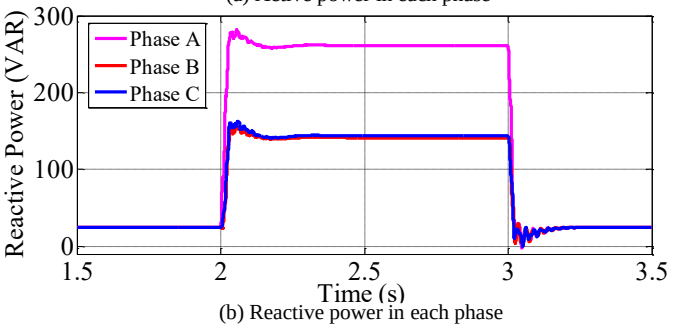
| Phase-A voltage | Test 1 $U_0 = 50\ V$ | Test 2 $U_0 = 20\ V$ |
|---|---|---|
| $U_p\ (V)$ | 64.2 | 32.5 |
| $E_{max}\ (V)$ | 132.6 | 112.5 |
| $P_{max}\ (W)$ | 893 | 0 |

### A. *Asymmetric fault simulation Test 1: moderate voltage dip*

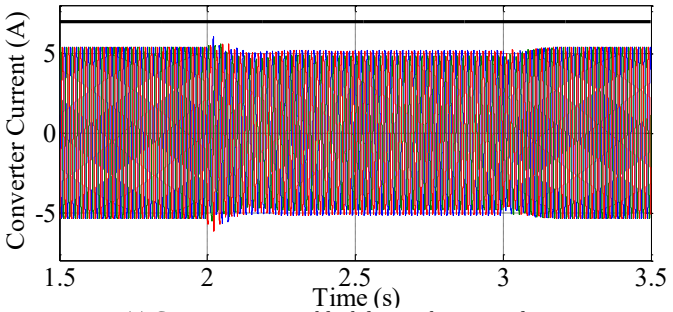
Fig. 10 shows the result of the converter in response to a 0.5 pu grid voltage dip on phase-A. As see in Table III, the reference active power of 800 W during the fault does not hit the limitation which is 893 W, and similarly for the voltage (100+(100-64.2)×0.5=117.5 V). It can be seen that following the fault, active power in phase-A decreases while that in phase-B and phase-C increases. This is because of the increase in the converter voltage. Referring to (1,2), the increase in $E$ leads to both active and reactive power increase, whenever $E > U_P cos\delta$; while the reduction in $U_P$ leads to active power reduction and reactive power increase. This is the reason that the reactive power in phase-A is higher than others. Since the voltage limitation covers the worst situation, which is a symmetric fault, the current is less than the limit in the asymmetric fault as shown in Fig. 10 (c) and lower than the limited value during the fault.



(a) Active power in each phase



(b) Reactive power in each phase

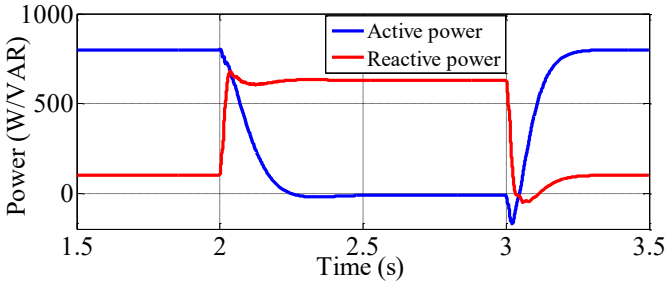


(c) Converter current; black line is the current limit

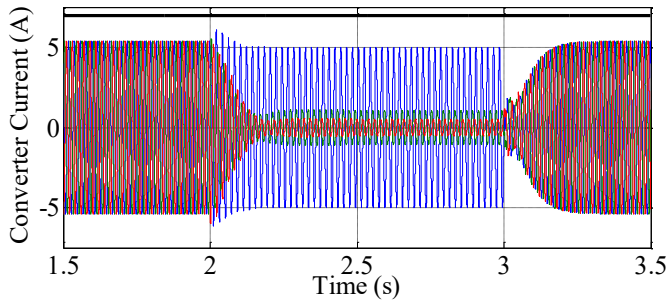
Fig. 10. Test 3: Voltage limit validation in a moderate asymmetric voltage dip. Initially the converter stabilizes at 800 W or 266.7 W for each phase, phase-A voltage dips to 0.5 pu at 2 s and recovers to 1 pu at 3 s.

### B. *Asymmetric fault simulation Test 2: severe voltage dip*

Fig. 11 shows the result of the converter in response to a 0.2 pu grid voltage dip on phase-A. In this case, both the power and voltage reference are limited by the proposed voltage limitation to the values shown in Table III. It can be seen in Fig. 11 (a) that the active power reduces to 0 W and the reactive power increases significantly after the fault occurrence. The current is satisfied and below the limitation as shown in Fig. 11 (b), but the current in phase-A is much higher than that in the other two phases. This is because the value of the voltage limitation picks the conditions in phase-A.



(a) Power



(d) Converter current

Fig. 11. Test 3: Voltage limit validation in a severe asymmetric voltage dip. Initially the converter stabilizes at 800 W, phase-A voltage dips to 0.2 pu at 2 s and recovers to 1 pu at 3 s.

These tests verify the effectiveness of the proposed voltage limitation is in the case of an asymmetric fault.

## VII. CONCLUSIONS

This paper proposes a voltage limitation method for the grid-forming converter to avoid overcurrent damage. The conventional current limitation used in the grid-forming converter has constraints on the duration of the saturated current and the initial loading, which would otherwise, lead to the synchronization instability. The proposed voltage limitation method has no such constraints and can fit to different situations. The setting of the voltage limitation can maximize the converter active power output or reactive power output according to the state of the grid. This voltage limitation only requires a saturation block in the voltage reference and can be applied to any control of the grid-forming converter. The proposed voltage limitation as presented has only considered its use in the positive-sequence control loop. The inclusion of the voltage limitation in a negative-sequence or/and zero-sequence control loop could

give further improvement of the performance, and this will be the subject of investigations in future work.

## VIII. References


[1] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of power converters in AC microgrids," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4734–4749, 2012.

[2] T. Chen, Junru; Milano, Federico; O'Donnell, "Assessment of grid-feeding converter voltage stability," Trans. Power Syst., vol. 34, no. 5, pp. 3980–3982, 2019.

[3] L. Zhang, L. Harnefors, and H. P. Nee, "Power-synchronization control of grid-connected voltage-source converters," IEEE Trans. Power Syst., 2010.

[4] A. Timbus, R. Teodorescu, F. Blaabjerg, and M. Liserre, "Synchronization methods for three phase distributed power generation systems. An overview and evaluation," in PESC Record - IEEE Annual Power Electronics Specialists Conference, 2005.

[5] U. B. Tayab, M. A. Bin Roslan, L. J. Hwai, and M. Kashif, "A review of droop control techniques for microgrid," Renewable and Sustainable Energy Reviews. 2017.

[6] R. Majumder, A. Ghosh, G. Ledwich, and F. Zare, "Angle droop versus frequency droop in a voltage source converter based autonomous microgrid," in 2009 IEEE Power and Energy Society General Meeting, PES '09, 2009.

[7] R. Majumder, B. Chaudhuri, A. Ghosh, R. Majumder, G. Ledwich, and F. Zare, "Improvement of stability and load sharing in an autonomous microgrid using supplementary droop control loop," IEEE Trans. Power Syst., 2010.

[8] S. D'Arco and J. A. Suul, "Equivalence of virtual synchronous machines and frequency-droops for converter-based Microgrids," IEEE Trans. Smart Grid, 2014.

[9] S. D'Arco, J. A. Suul, and O. B. Fosso, "A Virtual Synchronous Machine implementation for distributed control of power converters in SmartGrids," Electr. Power Syst. Res., 2015.

[10] Q. C. Zhong and G. Weiss, "Synchronverters: Inverters that mimic synchronous generators," IEEE Trans. Ind. Electron., 2011.

[11] Q. C. Zhong, P. L. Nguyen, Z. Ma, and W. Sheng, "Self-synchronized synchronverters: Inverters without a dedicated synchronization unit," IEEE Trans. Power Electron., 2014.

[12] J. Liu, Y. Miura, and T. Ise, "Comparison of Dynamic Characteristics between Virtual Synchronous Generator and Droop Control in Inverter-Based Distributed Generators," in IEEE Transactions on Power Electronics, 2016.

[13] L. Huang et al., "A Virtual Synchronous Control for Voltage-Source Converters Utilizing Dynamics of DC-Link Capacitor to Realize Self-Synchronization," IEEE J. Emerg. Sel. Top. Power Electron., 2017.

[14] J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "Distributed Power System Virtual Inertia Implemented by Grid-Connected Power Converters," IEEE Trans. Power Electron., 2018.

[15] Y. Cao et al., "A Virtual Synchronous Generator Control Strategy for VSC-MTDC Systems," IEEE Trans. Energy Convers., 2018.

[16] J. Chen, M. Liu, C. Oloughlin, F. Milano, and T. Odonnell, "Modelling, simulation and hardware-in-the-loop validation of virtual synchronous generator control in low inertia power system," in 20th Power Systems Computation Conference, PSCC 2018, 2018.

[17] T. Chen, Junru; O'Donnell, "Analysis of virtual synchronous generator control and its response based on transfer functions," IET Power Electron., vol. 12, no. 11, pp. 2965–2977, 2019.

[18] H. Mahmood, D. Michaelson, and J. Jiang, "Accurate reactive power sharing in an islanded microgrid using adaptive virtual impedances," IEEE Trans. Power Electron., 2015.

[19] D. Shuan and C. Chen, "Improving Active-power Transfer Capacity of Virtual Synchronous Generator in Weak Grid," 20th IEEE Work. Control Model. Power Electron. IEEE COMPEL, 2019.

[20] D. Shuan and C. Chen, "Reducing Transient Active-and Reactive-power Coupling in Virtual Synchronous Generators," 28th IEEE Int. Symp. Ind. Electron., 2019.

[21] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications. 2010.

[22] H. Xin, L. Huang, L. Zhang, Z. Wang, and J. Hu, "Synchronous Instability Mechanism of P-f Droop-Controlled Voltage Source Converter Caused by Current Saturation," IEEE Transactions on Power Systems, 2016.

[23] L. Huang, L. Zhang, H. Xin, Z. Wang, and D. Gan, "Current limiting leads to virtual power angle synchronous instability of droop-controlled converters," in IEEE Power and Energy Society General Meeting, 2016.

[24] W. Fan, X. Yan, and T. Hua, "Adaptive parameter control strategy of VSG for improving system transient stability," in 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia, IFEEC - ECCE Asia 2017, 2017.

[25] T. Chen, L. Chen, T. Zheng, X. Chen, and S. Mei, "General control strategy to limit peak currents of Virtual Synchronous Generator under voltage sags," in IEEE Power and Energy Society General Meeting, 2016.

[26] K. Shi, W. Song, P. Xu, R. Liu, Z. Fang, and Y. Ji, "Low-Voltage Ride-Through Control Strategy for a Virtual Synchronous Generator Based on Smooth Switching," IEEE Access, 2017.

[27] K. Shi, H. Ye, P. Xu, D. Zhao, and L. Jiao, "Low-voltage ride through control strategy of virtual synchronous generator based on the analysis of excitation state," IET Gener. Transm. Distrib., 2018.

[28] X. Lu, J. Wang, J. M. Guerrero, and D. Zhao, "Virtual-impedance-based fault current limiters for inverter dominated AC microgrids," IEEE Trans. Smart Grid, 2018.

[29] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms," in IET Renewable Power Generation, 2009.

[30] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-Impedance-Based Control for Voltage-Source and Current-Source Converters," IEEE Trans. Power Electron., 2015.

[31] J. Chen and T. O'Donnell, "Parameter constraints for virtual synchronous generator considering stability," IEEE Trans. Power Syst., 2019.

[32] F. Katiraei et al., "Investigation of Solar PV Inverters Current Contributions during Faults on Distribution and Transmission Systems Interruption Capacity," Quanta Technol., pp. 1–7, 2012.

[33] SMA Solar Technology AG, "Technical Information Short-Circuit Currents: Information on short-circuit currents of SMA PV inverters," pp. 1–5, 2012.