Cryogenic Low-Drop-Out Regulators Fully Integrated with Quantum Dot Array in 22-nm FD-SOI CMOS

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***Abstract* — This brief presents two monolithically integrated output-capacitor-less ("caples") low-drop-out (LDO) linear regulators implemented in 22-nm fully depleted silicon-on-insulator (FD-SOI) to support on-die scalable CMOS charge-based quantum processing unit (QPU). The proposed LDOs are used to regulate 0.8 V and 1.5 V input voltages for the programmable capacitive digital-to-analog converter (CDAC) and single-electron detector, respectively. Measured results show that both LDOs can maintain their respective output voltages with a maximum deviation <2% from ∼270 K down to ∼ 3.7 K.**

***Keywords* — Cryogenic CMOS, FD-SOI, LDO, single-electron detector, position-based qubits, charge qubits, quantum dot (QD), quantum dot array (QDA), quantum processing unit (QPU).**

I. Introduction

Quantum computers promise an exponential speed-up in solving certain classes of important computational problems that classical computing cannot handle. However, due to decoherence of qubits, a quantum core or quantum processing unit (QPU) must operate at cryogenic temperatures, currently in the millikelvin region. Aiming to achieve massive scalability in the number of qubits while addressing the input/output (I/O) congestion and system complexity, one of the possible solutions is to employ position-based charge qubits in CMOS technology that can operate at 4 K [1], [2]. Moreover, external interconnections have to be minimized by embedding the control and detector circuitry inside the same QPU. In this work, we utilize a charge-based QPU performing single-electron operations on quantum dots (QD). It is designed in 22-nm fully depleted silicon-on-insulator (FD-SOI), which provides key advantages over bulk CMOS [3], [4].

In Fig. 1, the quantum state of the quantum dot array (QDA) can be controlled by adjusting its potential barrier profile through the capacitive digital-to-analog converters (DACs). The final quantum state of the QDA can be read out by the single-electron detectors [4], [5]. The circuits involved in the operation require an accurate and stable voltage integrated in the QDA. Thus, the regulators must provide a clean power supply to the tightly integrated DACs and detectors. Good load regulation of LDO could be achieved by attaching bulky capacitors (of several μF) to the regulator output. Unfortunately, this would result in either high cost due to the large chip area or in additional I/O interconnections

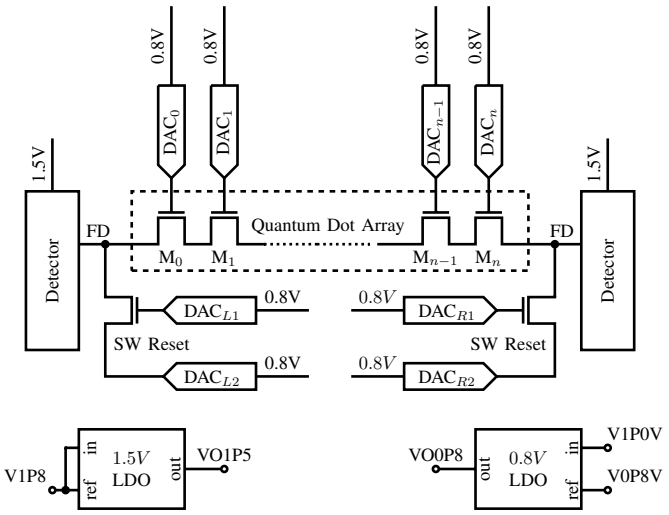


Fig. 1. "Capless" LDOs provide clean and regulated power supply to the DACs and detectors that directly interface with the QDA.

with excessively long interconnects. Thus, it is preferable to employ a so-called "capless" topology [6] which offers good line regulation and stable frequency response by introducing controlled current sinking at the output node [7].

Under the cryogenic operation, the electrical parameters of semiconductor devices experience large deviations, *e.g.* higher effective carrier mobility (μ_{eff}) [8], and higher threshold voltage (V_{TH}) [9]. The most effective way to estimate the electrical parameter deviations, and to include additional circuitry to compensate for their effects on performance, requires accurate models compatible with standard simulation tools. Unfortunately, reliable transistor models for temperatures below 100 K are still not commercially available. For this reason, the compensation strategy must be considered together with semiconductor physics knowledge, and extrapolation of circuits simulated at different temperatures to ensure reliable operation. To the best of the authors' knowledge, this paper presents the first cryogenic CMOS LDO designed as part of a QPU operating at cryogenic temperatures down to 4 K, unlike [10] which makes use of off-the-shelf components.

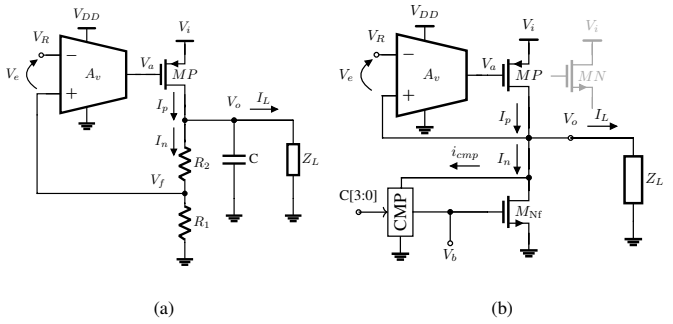


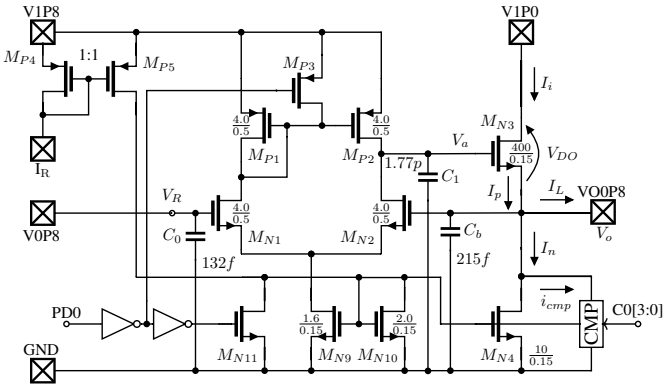
Fig. 2. (a) Conventional LDO that typically requires a large load capacitance. (b) Proposed cryogenic "capless" LDO with two options of the regulating transistor: PMOS to regulate 1.5 V, and NMOS to regulate 0.8 V.

II. Proposed Cryogenic Capless LDOs

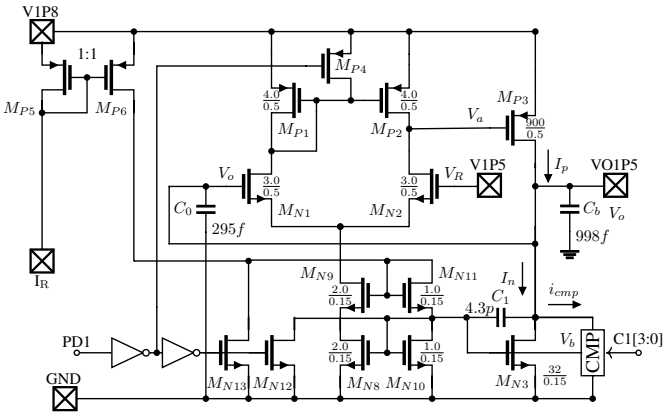
Fig. 2(a) shows the most commonly found LDO topology consisting of an error amplifier driving a PMOS transistor that adjusts the current flown to the output node whenever there is any sudden change in the current load such that the output voltage V_f is maintained. The dominant pole of the circuit is drastically shifted with the load, being the worst at the minimum current where the stability is compromised. This effect is usually compensated by a large capacitor C attached to the output acting as local charge storage compensating high current demands. This is not possible in our cryogenic QPU design.

As an alternative, Fig. 2(b) depicts the conceptual diagram of a so-called "capless" LDO which is composed of the error amplifier driving the PMOS regulator in the 1.5-V LDO design, and the NMOS regulator for the 0.8-V counterpart. The feedback signal is directly taken from the output and the quiescent current is controlled by the transistor $M_{\rm Nf}$. The compensation network can be digitally controlled to increase the quiescent current to compensate for possible deviations of $V_{\rm TH}$ and $\mu_{\rm eff}$ across the temperature range from 300 K down to 3.7 K. The two regulators were designed using the minimum number of transistors possible to limit the power consumption and its temperature contribution to the system, as well as to place the regulators as close as possible to the target quantum circuits.

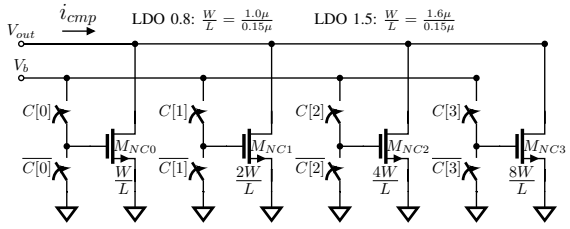
Schematics of the 0.8-V and 1.5-V "capless" LDOs are shown in Figs. 3(a) and (b), respectively. Both cores consist of a single-ended operational transconductance amplifier (OTA). The tail current for the 1.5-V LDO is a cascode current mirror M_{N8-9} to improve its impedance, whereas the 0.8-V LDO adopts a Widlar structure to guarantee all the transistors are in saturation since it operates at a relatively low supply. Both mirrors use an internal current reference I_R of 10 μA. The regulators can be turned off by the power-down signal PD0/PD1, which shunts the OTA's active load and the tail current mirrors, thus helping to limit the total generated heat. Both regulators have been designed with high-voltage transistors with thicker oxide devices and higher current driving capabilities.



(a) 0.8-V LDO core.



(b) 1.5-V LDO core.



(c) compensation network.

Fig. 3. Detailed schematics of 0.8-V and 1.5-V LDOs and its compensation network.

The compensation circuit is shown in Fig. 3(c). It consists of switchable binary-sized transistors $M_{\rm NC0}$–$M_{\rm NC3}$, acting as a programmable current sink. They can be programmed through $C[3:0]$, increasing the total current I_n from 5× I_R to 7.5× for the 0.8-V LDO, and from 32× I_R to 56× for the 1.5-V LDO. To overcome the model limitations, simulations were performed at different temperatures from room temperature (RT) down to –150°C for the whole circuit, and some extra simulations for single transistors of different geometries such that the estimates for 4 K could be extrapolated.

III. Measurements

Fig. 4 shows the chip micrograph and zoom-in view of core layout of the QPU with the two LDOs closely located to the QDA. The compensation network and I/Os are controlled

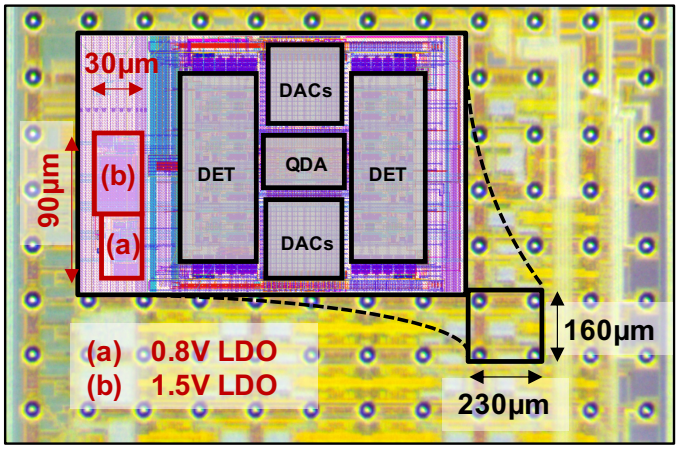


Fig. 4. Chip micrograph and zoom-in view of the layout of the quantum processing unit (QPU) in 22-nm FD-SOI with the proposed cryogenic LDOs tightly integrated.

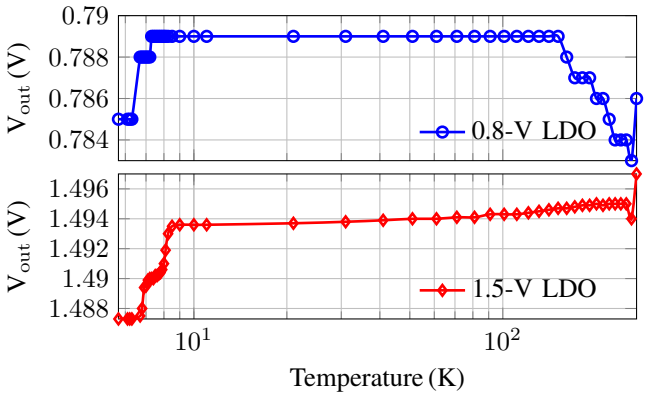


Fig. 5. Output voltage from the 0.8-V and 1.5-V LDOs across temperature.

via a Linux server and FPGA interface board working at RT, while the chip is operating at 4 K [11]. The regulators were measured for temperatures ranging from RT down to 3.7 K. Both circuits are functional in the whole temperature range and the output voltage versus temperature sweep is shown in Fig. 5 with no load and the compensation block off. It can be noticed that the 0.8-V LDO output is almost constant in the range of 100 K down to 10 K; the 1.5-V LDO exhibits a very gentle slope until the temperature falls below 8 K. Fig. 6 shows the output voltage for the 1.5 V regulator at RT and 3.7 K when the current load sweeps from 0 to the point where the output voltage drops 1% of the nominal output. As in the previous case, the compensation network is disabled. The maximum current delivered by the circuit, while maintaining the output voltage within 1%, is 41.2 mA at RT and 64 mA at 3.7 K, which is almost 1.5× higher.

Table 1. LDO Parameters.

Param.	(a) 0.8-V	(b) 1.5-V
V_{out}(V)	0.8	1.5
$\Delta V_{out,max}$(%)	1.76	0.65
$I_{out,max}$(mA)	-	41.2mA@RT, 64mA@3.7K
Area (μm^2)	706	1417

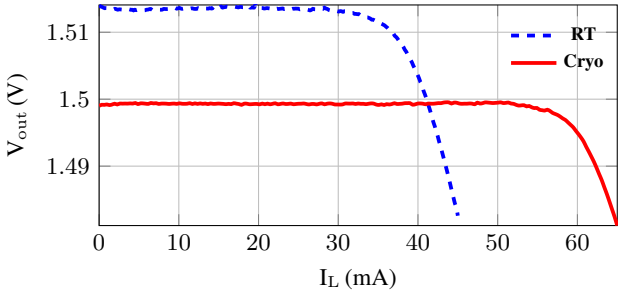


Fig. 6. Output voltage of the 1.5-V LDO across load current at RT (270 K), and cryogenic temperature (3.7 K).

IV. Conclusions

In this paper, two CMOS "capless" LDO regulators for 0.8 V and 1.5 V were demonstrated operational from room temperature down to the cryogenic temperature of ≃4 K. To the best of our knowledge, this is the first time monolithic linear regulators have been tested and proven functional at such a wide temperature range. This makes them suitable for an integration with a QPU, especially based on QDA. Both regulators exhibit a total voltage deviation of less than 2% within the temperature range 270 K down to 4 K. The 1.5-V regulator can effectively drive current loads of 41.2 mA at RT and 64 mA at ≃ 4 K while maintaining a stable output voltage within a 1% variation.

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