Investigation of First-Order Digital Bang-Bang Phase-Locked Loops with Reference Clock Jitter

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***Abstract*—Bang-bang phase-locked loops (BBPLLs) are a class of PLLs with a binary-quantized phase detector (BPD). They are widely used in clock and data recovery circuits and have recently been implemented as digital BBPLLs for high-bandwidth synthesis. This paper investigates a first-order digital BBPLL with reference clock jitter. We derive the Chapman-Kolmogorov equation which statistically characterizes the timing jitter process. The numerical solution of this equation allows us to compute the timing jitter probability density function (PDF) in steady-state and to examine the effect of varying loop detuning and RMS reference clock jitter on the timing offset, the RMS timing jitter and the mean number of steps to slip a cycle. The analysis shows that the steady-state PDF is Gaussian-like only for a small range of RMS clock jitter values, which leads to a new curve for the BPD gain as a function of jitter.**

I. Introduction

Bang-bang phase-locked loops (BBPLLs) are a class of PLLs with the distinct feature that the phase detector (PD) binary-quantizes the phase difference between its two input clocks, giving it the name binary (or bang-bang) PD (BPD). BBPLLs are widely used in clock and data recovery circuits because of their inherent sampling phase alignment and high-frequency capabilities [1]. Although they are commonly implemented using an analog loop filter driving a voltage-controlled oscillator, the binary output of the BPD lends itself naturally to a digital loop filter (DLF) implementation. In fact, recent developments in low-noise LC digitally-controlled oscillators (DCOs) have enabled an implementation of a digital BBPLL (DBBPLL) suitable for high-bandwidth synthesis [2], benefiting from the many advantages of a digital implementation. The hard nonlinearity introduced by the BPD, however, makes the loop analysis difficult. In practice, BBPLLs are analyzed by linearizing the BPD, similar to the steady-state linearization in traditional PLLs. Although linear system theory can then be applied, the very nonlinear behavior of the timing jitter remains unexplained.

This paper investigates the timing jitter in a first-order DBBPLL in the presence of reference clock jitter. Following the approach in [3] we derive the Chapman-Kolmogorov (CK) equation which, together with the probability density function (PDF) of the initial condition, gives a complete statistical description of the timing jitter process. The numerical solution of the CK equation allows us to compute the timing jitter PDF in steady-state, which reveals that it is decidedly non-Gaussian and is Gaussian-like only for a small range of RMS clock jitter values. The influence of varying loop detuning (frequency offset) and RMS clock jitter on the timing jitter performance is evaluated by numerically computing the mean, variance, skewness and kurtosis of the PDF. Moreover, the timing jitter PDF is used to obtain a new curve for and interpretation of the BPD gain as a function of the RMS clock jitter. Finally, the cycle slipping performance of the loop is investigated by adopting the CK equation.

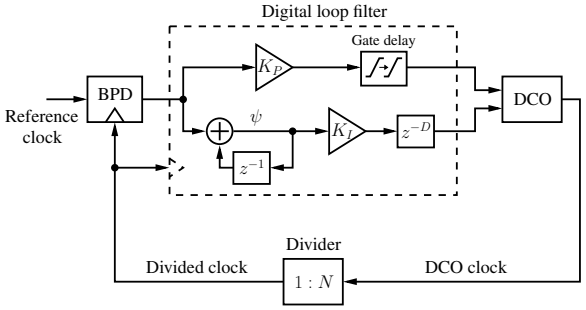


Fig. 1. Second-order digital bang-bang PLL architecture [4].

II. DBBPLL Architecture and Model

This section reviews the DBBPLL architecture implemented in [2] and its model analyzed in [4] and [5]. A block diagram of the architecture is shown in Fig. 1. The BPD compares the phase difference between the reference clock and the divided clock and delivers a binary phase information at its output, with a logical value high (low) if the reference clock leads (lags) the divided clock; its operation is therefore logically equivalent to that of a sampling register. The bit stream from the BPD output is then fed into the DLF, which consists of a proportional branch with gain coefficient K_P and an integral branch with gain coefficient K_I. To improve the jitter performance of the loop, the two branches are added inside the DCO and control the DCO frequency directly, without needing a digital-to-analog converter [2]. The delay due to possible pipeline stages in the integral path is modeled by the delay element of D reference clock cycles, whereas the delay of some gates in the proportional path can be neglected. The high-frequency output clock of the DCO is finally divided by the feedback divider by N and is fed back as divided clock to both the BPD and the DLF.

The quantity of interest in our study is the timing jitter Δt

between the reference clock and the divided clock. Because updating the BPD output and clocking the DLF occurs only every cycle of the divided clock (see Fig. 1), the loop behavior can be described at discrete time instants $n = 0, 1, \ldots$, and we only need to consider the time instants of the rising edges of the reference clock and the divided clock, denoted by t_r and t_d, respectively. With the state ψ of the integrator in the DLF as an additional state variable, the dynamics of the second-order DBBPLL is described by the 2D system of first-order difference equations [5]

$$\Delta t_{n+1} = \Delta t_n + T_{r,n} - NT_{v0} - NK_I K_T \psi_{n-D} - NK_P K_T \operatorname{sgn} \Delta t_n \quad (1)$$

$$\psi_{n+1} = \psi_n + \operatorname{sgn} \Delta t_{n+1} \quad (2)$$

where $\Delta t_n = t_{r,n} - t_{d,n}$ and ψ_n are, respectively, the timing jitter and the integrator state at the nth sampling instant, $T_{r,n}$ is the nth reference clock period, and the signum function is defined as $\operatorname{sgn} x = 1$ for $x \geq 0$, and $\operatorname{sgn} x = -1$ for $x < 0$. The DCO is modeled by the free-running clock period T_{v0} and the period gain constant K_T.

As mentioned in Sec. I, linear system theory can be applied to analyze the nonlinear loop by replacing the BPD with a gain. This BPD gain depends on the jitter between the reference clock and the divided clock (untracked jitter) and has been derived by considering the jitter on the reference clock only, neglecting the loop dynamics [6]. To include the loop dynamics in the analysis, Markov chain theory was applied in [7] to derive a more general expression for the BPD gain.

Following [7] we assume noise-free PLL blocks and consider only jitter on the reference clock, so that the nth reference clock period

$$T_{r,n} = T_{r0} + \tau_n \quad (3)$$

where T_{r0} is the nonmodulated and jitter-free period and τ_n is a random variable modeling the jitter value at the nth sampling instant. Since our primary interest in this work is a first-order loop we substitute $K_I = 0$ and (3) into (1) and obtain the first-order stochastic difference equation

$$\Delta t_{n+1} = \Delta t_n + \Delta T - NK_P K_T \operatorname{sgn} \Delta t_n + \tau_n \quad (4)$$

where $\Delta T = T_{r0} - NT_{v0}$ is the loop detuning due to a frequency offset between the reference clock and the divided free-running DCO clock. In [7] the BPD gain was derived for (4) with $\Delta T = 0$, which applies to a first-order loop with zero detuning or (approximately) to the second-order loop (1) – (2) with $K_I \ll K_P$; in the latter case, the loop delay D can be neglected and the assumption $\Delta T = 0$ is justified because a second-order loop will track out any frequency offset. Since we focus on the first-order loop in (4) with nonzero detuning, our analysis will also include the case treated in [7].

It is convenient to normalize (4) by the quantization step $NK_P K_T$ of the divided clock period [4], so that we obtain

$$u_{n+1} = u_n + m - \operatorname{sgn} u_n + \xi_n \quad (5)$$

where $u_n = \Delta t_n / (NK_P K_T)$ is the normalized timing jitter at the nth sampling instant and $m = \Delta T / (NK_P K_T)$ is the normalized detuning. The normalized jitter sequence[1] $\{\xi_n\}$ is assumed to be a sequence of independent and identically distributed Gaussian random variables with zero mean and variance σ^2. We further assume that the detuning m is either zero (in case of the first-order loop approximating the second-order loop) or, without loss of generality, positive and irrational; the latter assumption is justified since the natural tolerances in an implementation make the exact period of the reference clock and the free-running DCO clock unknown, and with probability 1 they will be irrational [4], [8].

To aid the understanding of the timing jitter PDF plots in Sec. IV, let us summarize the deterministic dynamics of (5) in the jitter-free case $\{\xi_n\} \equiv 0$. Then the difference equation describes a single-loop sigma-delta modulator with a 1-bit quantizer and constant input [4]. The system is stable if $|m| < 1$, and for any initial condition u_0, the timing jitter sequence $\{u_n\}$ will lie in the interval $[m-1, m+1)$ in steady-state [8]. If $m \in (0, 1)$ is irrational, the timing jitter sequence will be uniformly distributed on this interval and thus have mean m (timing offset) and standard deviation $1/\sqrt{3}$ (RMS timing jitter). If $m = 0$, the timing jitter sequence will jump back and forth between two values, meaning that the DBBPLL has entered a limit cycle.

III. Analysis Of The First-Order DBBPLL

A. Chapman-Kolmogorov Equation and Steady-State PDF

The stochastic difference equation (5) describes the timing jitter process in a first-order DBBPLL in the presence of reference clock jitter. Since at each time instant n, the next timing jitter value u_{n+1} depends only on its current value u_n (independent of its past) and on the value of the jitter random variable ξ_n, the timing jitter sequence $\{u_n\}$ forms a discrete-time, continuous-valued Markov process. Consequently, $p_n(u|u_0)$, the conditional PDF of u_n conditioned on the initial value u_0, satisfies the CK equation [3]

$$p_{n+1}(u|u_0) = \int_{-\infty}^{\infty} q_n(u|z) p_n(z|u_0) dz \quad (6)$$

where $q_n(u|z)$ is the transition PDF of u_{n+1} given $u_n = z$. Since at each time instant n, the jitter random variable ξ_n in (5) is independent of u_n, the transition PDF $q_n(u|z)$ is Gaussian with (conditional) mean $E\{u|z\} = z + m - \operatorname{sgn} z$ and variance σ^2, i.e.,

$$q_n(u|z) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-(u - z - m + \operatorname{sgn} z)^2 / (2\sigma^2)\right]. \quad (7)$$

The independence of n in (7) means that the discrete-time Markov process is time-homogeneous, and by dropping the subscript n and defining the transition kernel $K(u, z) := q(u|z)$, the CK equation (6) becomes

$$p_{n+1}(u|u_0) = \int_{-\infty}^{\infty} K(u, z) p_n(z|u_0) dz \quad (8)$$

[1]For simplicity, these three quantities will in the following be referred to without the qualifier "normalized".

which, together with the PDF $p_0(u)$ of the initial value u_0, completely characterizes the timing jitter sequence $\{u_n\}$.

In practice we are interested in the behavior of the timing jitter in steady state, i.e., after sufficiently long time. Let

$$p(u) = \lim_{n\to\infty} p_n(u) \tag{9}$$

be the steady-state PDF of the timing jitter, where conditioning on u_0 will in the following be understood. Assuming that a unique stationary steady-state PDF exists, it follows that this PDF is the unique solution of the integral equation

$$p(u) = \int_{-\infty}^{\infty} K(u,z)p(z)dz \tag{10}$$

which is independent of the initial value u_0.

A problem with the numerical integration of (8) is that the signum function in (7) makes the integrand discontinuous in z. By dividing the domain of integration into the two disjoint intervals $(-\infty, 0)$ and $[0, \infty)$, over each of which the integrand is continuous in z, we can write (8) as

$$p_{n+1}(u) = \int_{-\infty}^{0} K^-(u,z)p_n(z)dz + \int_{0}^{\infty} K^+(u,z)p_n(z)dz \tag{11}$$

where

$$K^{\pm}(u,z) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-(u-z-m\pm 1)^2/(2\sigma^2)\right]. \tag{12}$$

The results of the numerical solution of (11) will be presented in Sec. IV.

B. Mean Number of Steps To Slip a Cycle

We saw in Sec. II that in a DBBPLL without reference clock jitter, the timing jitter stays within an interval in steady-state. If Gaussian jitter is added, the timing jitter may take on arbitrary values. This implies that, starting now from the initial condition u_0 in steady state, the timing jitter sequence $\{u_n\}$ may increase or decrease by 2π radians, in which case the loop is said to have slipped a cycle. The parameter of practical interest is the mean time to slip a cycle. However, since our model (5) does not specifically refer to a clock period, we will rather compute the mean number of steps to slip a cycle. To this end we must solve the first-passage time problem associated with the timing jitter sequence $\{u_n\}$. Following the approach in [3], absorbing boundaries are placed at $u_0 \pm 2\pi$, implying that $p_n(u) = 0$ for $|u - u_0| \geq 2\pi$ and for all $n \geq 0$. The CK equation (8) may therefore be written as

$$p_{n+1}(u) = \int_{u_0-2\pi}^{u_0+2\pi} K(u,z)p_n(z)dz. \tag{13}$$

Now, let N_{sc} be a discrete random variable denoting the number of steps to slip a cycle. Since N_{sc} can take on only positive integers, the mean number of steps to slip a cycle $E\{N_{sc}\}$ may formally be computed as

$$E\{N_{sc}\} = \sum_{n=1}^{\infty} nP\{N_{sc} = n\} \tag{14}$$

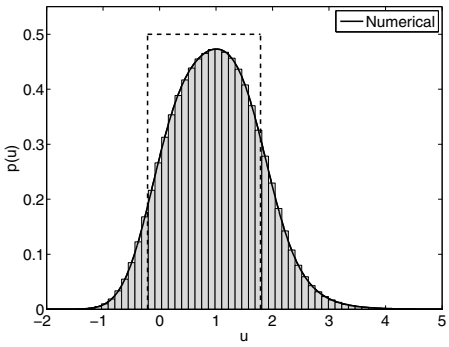


Fig. 2. Comparison of the steady-state timing jitter PDF $p(u)$ obtained numerically (solid) and estimated from simulation (histogram). The dashed box corresponds to the uniform PDF in the jitter-free case. Parameters: $m \approx 0.7889$ (irrational) and $\sigma = 0.4$.

where $P\{N_{sc} = n\}$ is the probability that the loop slips a cycle after n steps. In [3] it was shown that $E\{N_{sc}\}$ in (14) can be found by

$$E\{N_{sc}\} = 1 + \int_{u_0-2\pi}^{u_0+2\pi} \sum_{n=1}^{\infty} p_n(u)du \tag{15}$$

where $p_n(u)$ is obtained from (13) after n iterations, with the domain of integration again split up.

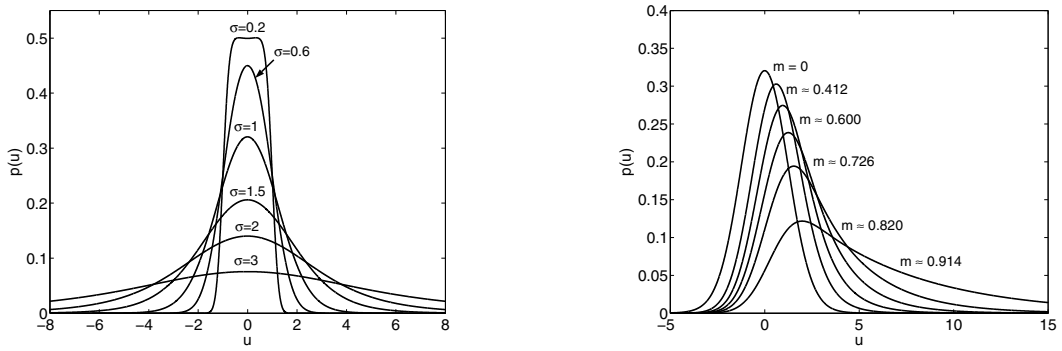
IV. Numerical and Simulation Results

This section compares the results obtained by numerically solving the CK equation (11) with the simulation results obtained from 10^7 iterations of the stochastic difference equation (5). For the numerical solution, the steady-state PDF defined in (9) was assumed to have been obtained when the maximum of two consecutive PDFs in the iteration was less than a predefined amount [3]. The domain of integration was taken to be the interval spanned by the maximum and minimum bin number of the histogram obtained from simulation. The initial timing jitter u_0 was assumed to be zero, giving an initial PDF $p_0(u) = \delta(u)$.

A. Steady-State Timing Jitter PDF

As an example to verify the approach based on the CK equation, the steady-state PDF was numerically computed for $m \approx 0.7889$ and $\sigma = 0.4$. The result plotted in Fig. 2 shows that the numerical PDF matches the estimated PDF given by the histogram.

The shape of the steady-state PDF can be qualitatively explained as follows. According to Sec. II, if the reference clock is jitter-free and the detuning m is irrational (as in the figure), the steady-state timing jitter will have a uniform distribution on the interval $[m-1, m+1)$, which is shown by the dashed box. If the reference clock is subject to Gaussian jitter, the steady-state timing jitter will be unbounded and leave this interval on both sides, so that the probability mass is spread out on the real line. Moreover, since the detuning $m > 0$, more probability mass is spread to the right of the interval than to the left of it, giving the PDF its asymmetric shape.



(a) (b)

Fig. 3. Steady-state timing jitter PDF $p(u)$ for (a) fixed $m = 0$ and varying σ, and (b) fixed $\sigma = 1$ and varying m.

The effect of reference clock jitter and detuning on the shape of the steady-state timing jitter PDF is further illustrated in Fig. 3. In particular, Fig. 3(a) shows several PDFs for fixed detuning $m = 0$ and varying jitter σ. For small σ, the PDF is similar to a uniform PDF since the reference clock jitter is small compared to the quantization step of the divided clock period. As σ increases, the PDF becomes Gaussian-like, indicating that the reference clock jitter effectively linearizes the hard nonlinearity in the BPD. As σ increases further, the PDF becomes rather peaked with long tails (compared to a Gaussian PDF), and the variance of the steady-state timing jitter increases significantly. Notice in the figure that the PDFs are symmetric about zero, since the zero detuning makes it equally likely that the steady-state timing jitter will leave the interval $[-1, 1)$ on either side.

Figure 3(b) shows several timing jitter PDFs for the opposite case, namely for fixed jitter $\sigma = 1$ and varying detuning m. It can be seen that as m increases, the PDF becomes increasingly asymmetric, with the right tail being longer than the left tail (and vice versa if we assumed negative m). This implies that the timing offset, given by the expected value of the timing jitter in steady-state, will be larger than in the jitter-free case, which is equal to m (see Sec. II).

B. Timing Offset and RMS Timing Jitter

The PDF plots in the previous subsection do not only qualitatively describe the steady-state timing jitter of the DBBPLL but also allow us to quantitatively evaluate the jitter performance. More specifically, the timing offset and the RMS timing jitter can be determined by numerically computing the mean and the variance of the timing jitter PDF, respectively. With the kth moment μ'_k of the PDF $p(u)$ defined as [9]

$$\mu'_k = E\left\{u^k\right\} = \int_{-\infty}^{\infty} u^k p(u) du \tag{16}$$

the timing offset μ_u equals the mean μ'_1, and the RMS timing jitter σ_u equals the square-root of the variance $\mu'_2 - \mu_u^2$, both of which are plotted in Fig. 4 for different values of m and σ. For each marker we numerically computed the timing jitter PDF $p(u)$ and used it in (16) to obtain the first and second moment μ'_1 and μ'_2, and thus the mean and variance μ_u and σ_u^2, respectively.

Figure 4(a) plots the timing offset μ_u as a function of (irrational) detuning $m \in (0, 1)$ with parameter σ. The dashed line corresponds to the jitter-free case for which the timing jitter is uniformly distributed with $\mu_u = m$, as discussed in Sec. II. It can be seen that for small jitter σ, the timing offset is only slightly larger than in the jitter-free case, even for large detuning m. Likewise, for small detuning m, the timing offset is also only slightly larger than in the jitter-free case, even for large jitter σ. As both jitter and detuning increase, however, the timing offset increases significantly, corresponding to a steady-state PDF with a long right tail, as observed in Fig. 3(b).

Figure 4(b) shows the RMS timing jitter σ_u as a function of σ with parameter m. The dashed line corresponds again to the jitter-free case for which the timing jitter is uniformly distributed with $\sigma_u = 1/\sqrt{3}$ (if m is irrational), as discussed in Sec. II. The figure shows that decreasing σ causes the RMS timing jitter to become independent of m and tend to the value of the uniform PDF. By contrast, increasing σ leads to an increase in the RMS timing jitter, with higher values if detuning is larger (longer PDF tails), and the lowest value if detuning is zero (symmetric PDF).

Notice in both plots that the numerical values agree well with the simulated values; the disagreement for large m and large σ is due to numerical inaccuracies caused by the large domain of integration.

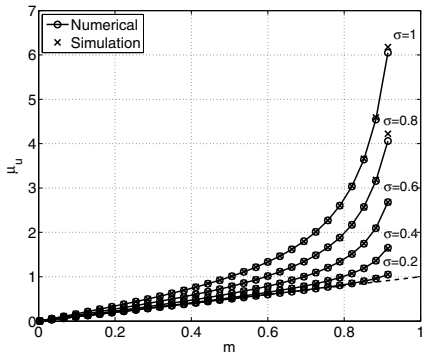
C. Skewness and Kurtosis of the Steady-State PDF

The description of the PDF shape (asymmetry and peakedness) in the previous subsections can be made more precise by using two statistical measures: the skewness and the kurtosis.

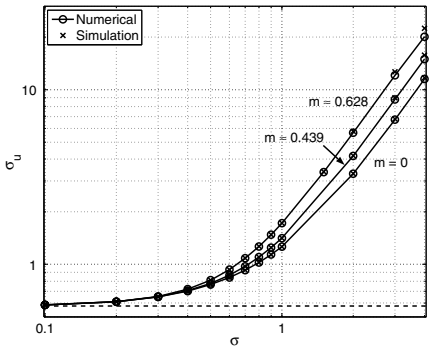
The skewness γ_1 is a measure of the degree of asymmetry of a PDF and is defined as [9]

$$\gamma_1 = \frac{\mu_3}{\sigma_u^3} \tag{17}$$

where μ_3 is the third moment about the mean of $p(u)$. The kurtosis, on the other hand, is a measure of the degree of peakedness of a PDF and is not uniquely defined. We will use



(a)



(b)

Fig. 4. (a) Timing offset μ_u and (b) RMS timing jitter σ_u as a function of σ for different detuning values m.

the kurtosis excess γ_2 defined as [9]

$$\gamma_2 = \frac{\mu_4}{\sigma_u^4} - 3 \tag{18}$$

where μ_4 is the fourth moment about the mean of $p(u)$. Since γ_2 is zero for the Gaussian PDF, a nonzero γ_2 means a non-Gaussian PDF (zero skewness presumed), and so the kurtosis excess is suitable to characterize the degree of which the timing jitter PDF deviates from a Gaussian PDF.

Figure 5 plots the skewness and the kurtosis excess as a function of σ with parameter m. Similar to Fig. 4, for each marker we numerically computed the timing jitter PDF $p(u)$ and used it in (16) to obtain the first four moments μ_1', μ_2', μ_3' and μ_4'. To determine the skewness in (17) we then computed the third moment about the mean by the moment transformation $\mu_3 = \mu_3' - 3\mu_u\mu_2' + 2\mu_u^3$, and the variance by $\sigma_u^2 = \mu_2' - \mu_u^2$. The kurtosis in (18) was determined similarly by the moment transformation $\mu_4 = \mu_4' - 4\mu_u\mu_3' + 6\mu_u^2\mu_2' - 3\mu_u^4$. The following conclusions can be drawn from the figure:

- For $m = 0$, the skewness $\gamma_1 = 0$ independent of σ; this means that the steady-state PDF is symmetric about zero, as was observed in Fig. 3(a).
- For $m \in (0, 1)$, the skewness $\gamma_1 > 0$ (although hardly visible for small σ) and increases with increasing σ; this means that the right tail of the steady-state PDF is more pronounced than the left tail and becomes even more so with increasing σ. The same is true for fixed σ and increasing m, as was observed in Fig. 3(b).

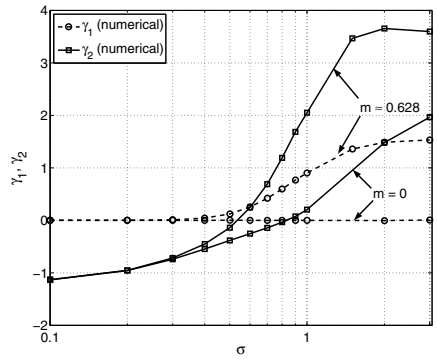


Fig. 5. Skewness γ_1 and kurtosis excess γ_2 of the steady-state timing jitter PDF as a function of σ for different detuning values m.

- For each m, there is one particular σ^* for which the kurtosis excess $\gamma_2 = 0$, so that γ_2 is positive if $\sigma > \sigma^*$, and negative if $\sigma < \sigma^*$, with the corresponding interpretation of the PDF shape.
- For $m = 0$, the previous point (and $\gamma_1 = 0$) imply that the steady-state PDF is, in fact, Gaussian only for $\sigma = \sigma^*$; in this case, the loop behaves effectively linearly since the Gaussian PDF of the reference clock jitter is transformed into the Gaussian PDF of the timing jitter with different variance.
- Independent of m, the skewness and kurtosis excess tend each to a constant value with decreasing σ; this follows from the discussion in Sec. II that in the jitter-free case, the timing jitter has a uniform PDF, for which the skewness $\gamma_1 = 0$ and the kurtosis excess $\gamma_2 = -1.2$ (see the left end of the curves) [9].

The important conclusion that the steady-state PDF is Gaussian-like only in a small range around σ^* reveals the effect the hard nonlinearity has on the loop dynamics and thus on the statistical properties of the timing jitter.

D. BPD Gain K_{bpd}

It was mentioned in Sec. II that linear system theory can be used to analyze the nonlinear loop by replacing the BPD with a gain. For a first-order loop with zero detuning, or for a second-order loop with $K_I \ll K_P$, the BPD gain K_{bpd} is defined as [6], [7]

$$K_{bpd} = 2p(0) \tag{19}$$

where $p(0)$ is the timing jitter PDF $p(u)$ evaluated at zero. Assuming $p(u)$ to be Gaussian (i.e., neglecting the loop dynamics), two expressions for K_{bpd} reported in the literature are $K_{bpd} = 1/(\sqrt{2\pi}\sigma)$ for $\sigma \ll 1$ [10] and $K_{bpd} = 2/(\sqrt{2\pi}\sigma)$ for $\sigma \gg 1$ [6]. By modeling the loop dynamics using a Markov chain, the more general (approximate) expression

$$K_{bpd} = \frac{1}{\sqrt{2\pi}\sigma}\left(1 + e^{-\frac{(NK_PK_T)^2}{2\sigma^2}}\right) \tag{20}$$

was derived in [7] and includes the other two as asymptotes.

The results in the previous subsection, however, have shown that the steady-state timing jitter PDF resembles a Gaussian

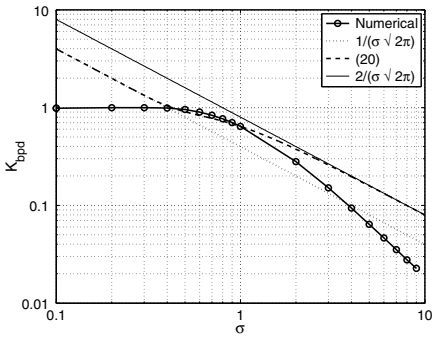


Fig. 6. BPD gain K_{bpd} as a function of σ for $m = 0$.

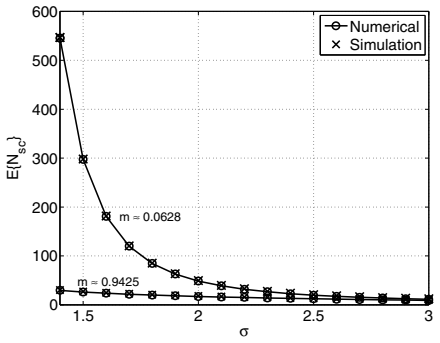


Fig. 7. Mean number of steps to slip a cycle $E\{N_{sc}\}$ as a function of σ for small and large detuning m.

PDF only for a small range around σ^*. To give a new interpretation of the BPD gain in view of these results we computed K_{bpd} in (19) by evaluating the numerical PDFs at zero. The result, together with the two asymptotes and (20), is plotted in Fig. 6 as a function of σ (see also Fig. 6 in [7]). Distinguish the following three areas:

- For $\sigma \ll 1$, the BPD gain is constant since the steady-state timing jitter PDF resembles a uniform PDF, which leaves $p(0)$ constant for a range of σ values.
- For σ close to 1, the BPD gain is close to that given by (20) (with NK_PK_T normalized to 1) since the steady-state timing jitter PDF is Gaussian-like.
- For $\sigma \gg 1$, the BPD gain falls off quickly and approaches an asymptote that is different from the asymptote $K_{bpd} = 2/(\sqrt{2\pi}\sigma)$; this is because the latter was derived assuming a Gaussian timing jitter PDF whereas the PDF plots and the statistical characterization in the previous subsections have revealed the non-Gaussianity.

Note that for simplicity we assumed a uniform steady-state timing jitter PDF for small σ even if $m = 0$; this is only an approximation because as σ tends to zero, the limit cycle for the jitter-free case mentioned in Sec. II will persist (see [10]).

E. Mean Number of Steps To Slip a Cycle

To evaluate the cycle slip performance of the DBBPLL, the CK equation (13) was numerically integrated and assumed to have converged as described above. The initial value u_0 in steady state was set to the mean m in the jitter-free case, giving an initial PDF $p_0(u) = \delta(u - m)$. The PDFs resulting from the iterations were summed up and used in (15) to obtain the mean number of steps to slip a cycle $E\{N_{sc}\}$. The result is plotted in Fig. 7 as a function of σ for both small and large detuning m. For small σ, it takes on average fewer steps to slip a cycle if m is large than if it is small, which can be attributed to the larger tails of the steady-state timing jitter PDF (see Fig. 3(b)). As σ increases, though, the mean number of steps to slip a cycle becomes independent of m because the PDF is significantly spread out over the real line. Observe that the numerical results agree well with the simulation results independent of m and σ; numerical inaccuracies were small because of the constant domain of integration in (15) compared with that in (11).

V. Conclusions

In this paper we have given a statistical characterization of the timing jitter in a first-order DBBPLL in the presence of reference clock jitter. The numerical solution of the CK equation has allowed us to evaluate the effect of varying clock jitter and detuning on the jitter performance (timing offset and RMS timing jitter) and on the shape of the timing jitter PDF, revealing its non-Gaussianity and leading to a new BPD gain curve. Ongoing work in this area includes an analytical description of the timing jitter process, and an extension of the numerical approach based on the CK equation to first-order loops with additional loop delay and to the more commonly used second-order loops.

VI. Acknowledgement

This research is funded by Science Foundation Ireland.

References

[1] R. C. Walker, "Designing bang-bang PLLs for clock and data recovery in serial data transmission systems," in *Phase-Locking in High-Performance Sytems - From Devices to Architectures*, B. Razavi, Ed. IEEE Press, 2003, pp. 34–45.

[2] N. Da Dalt, E. Thaller, P. Gregorius, and L. Gazsi, "A compact triple-band low-jitter digital LC PLL with programmable coil in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1482–1490, July 2005.

[3] A. Weinberg and B. Liu, "Discrete time analyses of nonuniform sampling first- and second-order digital phase lock loops," *IEEE Trans. Commun.*, vol. 22, no. 2, pp. 123–137, February 1974.

[4] N. Da Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 1, pp. 21–31, January 2005.

[5] ——, "Linearized analysis of a bang-bang digital PLL and its validity limits applied to jitter transfer and jitter generation," *IEEE Trans. Circuits Syst. I*, to appear.

[6] Y. Choi, D.-K. Jeong, and W. Kim, "Jitter transfer analysis of tracked oversampling techniques for multigigabit clock and data recovery," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 11, pp. 775–783, November 2003.

[7] N. Da Dalt, "Markov chains-based derivation of the phase detector gain in bang-bang PLLs," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 11, pp. 1195–1199, November 2006.

[8] R. M. Gray, "Oversampled sigma-delta modulation," *IEEE Trans. Commun.*, vol. 35, no. 5, pp. 481–489, May 1987.

[9] M. Abramowitz and I. A. Stegun, *Handbook of Mathematical Functions with Formulas, Graphs, and Mathematical Tables*, 9th ed. New York: Dover, 1972.

[10] J. L. Sonntag and J. Stonick, "Digital clock and data recovery architecture for multi-gigabit/s binary links," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1867–1875, August 2006.