

# Analysis of Limit Cycles in a PI Digitally Controlled Buck Converter

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**Abstract**—Digital control of power converters has been an area of considerable research interest in recent times. One of the problems which arises in these systems is that of the limit cycle oscillations that occur due to quantization in the feedback loop. This paper investigates the limit cycle oscillations that occur in the digitally controlled version of the buck converter with a proportional-integral controller. The amplitude and frequency of the oscillations that may occur on two duty cycle levels are investigated and related to the controller gain parameters. The analysis shows that it is not possible to guarantee that limit cycle oscillations on two levels will not occur simply by adjusting the gain parameters, and yields a condition which will prevent oscillations on two levels from occurring.

## I. INTRODUCTION

The area of digital control in power electronics has attracted considerable research interest in the last number of years. Digital control has numerous potential advantages over the more traditional analog control. These include low power consumption, lower sensitivity to parameter variations, and the possibility for increased complexity and flexibility of control laws [1]. The buck converter is widely used in a variety of applications in power electronics, for example in portable electronic devices.

The existence and containment of limit cycle oscillations which arise in these systems owing to the quantization effects of the analog-to-digital (A/D) converter and the digital pulse-width modulator (DPWM) are of interest [2]. These limit cycles are undesirable as they degrade output voltage regulation [3], alter the output spectrum, cause increased power losses, and their amplitude and frequency are difficult to predict [1]. Previous work [1], [4], on digitally controlled power converters has focused on the describing function approach, in which it is assumed that the limit cycles are of a sinusoidal nature. This is not always the case in converters of this nature and does not guarantee that limit cycles will not occur [5]. Using this approach time domain simulations are often required in order to ascertain that limit cycle oscillations will not occur over a range of operating conditions. Other work in this area has used an incremental energy approach [5], and a statistical method for predicting when limit cycle oscillations occur [6], which yield expressions for the probability of limit cycles occurring. Ref. [7] analysed a digitally controlled buck converter with an integral controller, and conditions for the prevention of limit cycles in this system were derived. In this paper, we extend this form of analysis to a system with a PI controller.

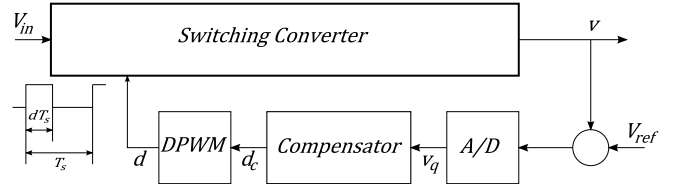


Fig. 1. Switching power converter from [4]

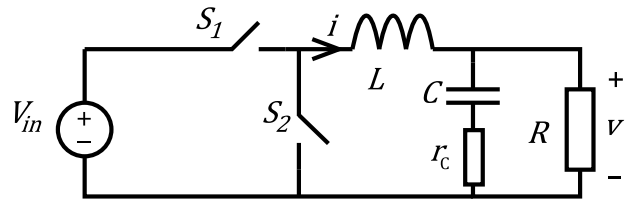


Fig. 2. Synchronous buck converter

## II. MODEL OF SYSTEM

The circuit which we will consider is the dc-dc switching power converter shown in Fig. 1, where the switching converter is the buck circuit from Fig. 2. The purpose of an ideal buck converter is to convert an input voltage  $V_{in}$  to a lower output voltage  $dV_{in}$ ,  $d \in (0, 1)$ . Switches  $S_1$  and  $S_2$  are switched in a complementary fashion. If switch  $S_1$  is open for a time  $dT_s$  and closed for a time  $(1 - d)T_s$ , where  $d$  is called the duty cycle and  $T_s$  is the switching period, then the output voltage of the converter will be given by  $v \approx dV_{in}$  in steady state. From Fig. 1, we see that the output voltage  $v$  is compared to a reference voltage  $V_{ref}$ , which is the desired output of the system, generating error voltage  $v_e$ . This is quantized by the A/D converter, generating a signal  $v_q$ , which is then passed to the compensator, which generates the duty-cycle command  $d_c$ , according to a control law.  $d_c$  is then quantized to a signal  $d$  by the DPWM, which opens and closes the switches as previously described. In what follows, we shall assume that all circuit components are ideal, except for the capacitor, the equivalent series resistance (ESR) of which is given by  $r_c$ , which was not included in [7], that the error voltage  $v_e$  is sampled at the frequency  $f_s = \frac{1}{T_s}$  at the start of a switching period, and that there is no quantization in the compensator.

The buck circuit is described by the equations

$$\frac{d}{dt} \begin{bmatrix} v(t) \\ i(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_n C} - \frac{R}{R_n} \frac{r_c}{L} & \frac{R}{R_n} \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \cdot \begin{bmatrix} v(t) \\ i(t) \end{bmatrix} + \delta \begin{bmatrix} \frac{R}{R_n} \frac{r_c}{L} \\ \frac{1}{L} \end{bmatrix} V_{in}, \quad (1)$$

with  $\delta = 1$  for the switch  $S_1$  closed and  $\delta = 0$  for  $S_1$  open, where  $R_n = R + r_c$ . Instead of the current  $i$  it is convenient to consider the new variable  $u = \frac{R}{R_n} \frac{1}{\omega C} i - \frac{\sigma}{\omega} v$  in order to simplify the equations. We will let  $W = [v, u]^T$ , and (1) becomes

$$\frac{d}{dt} W(t) = A W(t) + \delta \begin{bmatrix} r_c C (\omega^2 + \sigma^2) \\ (1 - \sigma r_c C) \frac{\omega^2 + \sigma^2}{\omega} \end{bmatrix} V_{in} \quad (2)$$

with the constant matrix  $A = \begin{bmatrix} -\sigma & \omega \\ -\omega & -\sigma \end{bmatrix}$ , where  $\sigma = \frac{1}{2R_n C} + \frac{R}{2R_n} \frac{r_c}{L}$  and  $\omega = \sqrt{\frac{R}{R_n} \frac{1}{LC} - \sigma^2}$ . It is not hard to derive that after the equation (2) acts for the time  $dT_s$  with  $\delta = 1$  and then the time  $(1-d)T_s$  with  $\delta = 0$ , a starting value  $W_0$  is transformed into  $W_1 = e^{AT_s} W_0 + N(d) V_{in}$ , where

$$N(d) = (e^{(1-d)T_s A} - e^{T_s A}) \begin{bmatrix} 1 \\ \sigma/\omega - \left( \frac{\sigma^2 + \omega^2}{\omega} \right) r_c C \end{bmatrix},$$

and the matrix exponential is given by

$$e^{tA} = e^{-\sigma t} \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix}, \quad t \text{ real.} \quad (3)$$

We shall use the following equations to model the feedback system, assuming a proportional-integral compensator:

$$d(n) = Q_{\text{DPWM}}[d_c(n)], \quad d_c(n) = -K_p v_q(n) - K_i d_i(n-1) \quad (4)$$

$$d_i(n) = d_i(n-1) + v_q(n), \quad v_q(n) = Q_{A/D}[v(n) - V_{\text{ref}}].$$

The function  $Q_{\text{DPWM}}$  rounds  $d_c$  to the closest value of the form  $j q_{\text{DPWM}}$ , where  $q_{\text{DPWM}}$  is the quantization step of the DPWM and  $j$  is a positive integer, subject to the condition that  $d \in (0, 1)$ , and the function  $Q_{A/D}$  rounds the value of  $v_e$  to the closest value of the form  $l q_{A/D}$ , where  $q_{A/D}$  is the quantization step of the A/D converter and  $l$  is a positive or negative integer. When  $v_q(n) = l q_{A/D}$ , we say that the voltage  $v(n)$  lies in the  $l$ -th error bin.

We thus obtain the autonomous three-dimensional discrete-time piece-wise linear discontinuous dynamical system given by:

$$W(n+1) = e^{T_s A} (W(n) - W_j^*) + W_j^*, \quad (5)$$

$$d_c(n+1) = d_c(n) - K_p (v_q(n+1) - v_q(n)) - K_i v_q(n), \quad (6)$$

with the quantized quantities  $d(n)$  and  $v_q(n)$  given by (4) and where

$$W_j^* = (I - e^{T_s A})^{-1} N(d_j) V_{in}, \quad (7)$$

We see from (5) that for  $d = d_j$  a trajectory in  $W$  is simply a logarithmic spiral winding clockwise in towards  $W_j^*$  and thus any trajectory in  $W$  consists of consecutive spiral segments winding in towards a value  $W_j^*$  as  $d_c$  changes from one

quantization level to another. Considering the effect of the voltage value  $v$  on  $d_c$ , we see that from the proportional part, when  $v_q(n)$  changes from quantization level  $l q_{A/D}$  to  $(l+m) q_{A/D}$ , there is a jump in the value of  $d_c(n)$  of magnitude  $-K_p m q_{A/D}$ . For the integral part, we see that a value of  $v_q(n) = l q_{A/D}$  will cause the value of  $d_c(n+1)$  to change by a value  $-K_i l q_{A/D}$ . Thus, for any  $W_j^*$  for which  $v_j^*$  lies in the zero-error bin, i.e.  $v_q = 0$ , and we have that  $d_c \in \left[ d_j - \frac{q_{\text{DPWM}} V_{in}}{2}, d_j + \frac{q_{\text{DPWM}} V_{in}}{2} \right)$ , then  $[v_j^*, u_j^*, d_c]$  represents a fixed point of the system. As long as a trajectory remains at a particular duty cycle level  $d_j$ , we have that  $\tilde{W}(n+p) = e^{pT_s A} \tilde{W}(n)$ , where  $\tilde{W}(n) = W(n) - W_j^*$ . If we assume that the relation  $\sigma \ll \omega \ll \frac{1}{T_s}$  holds, we have that  $W_{j+1}^* - W_j^* \approx [1, \delta_u]^T \tilde{q}$ , where we denote  $\delta_u = \frac{\sigma}{\omega} - \frac{\sigma^2 + \omega^2}{\omega} r_c C$  and  $\tilde{q} = q_{\text{DPWM}} V_{in}$ .

### III. LIMIT CYCLES ON TWO DUTY CYCLE LEVELS

Limit cycles in the system occur when an oscillation happens over two or more duty cycle levels. As in the case in [7], these may be single-loop limit cycles, in which a trajectory rotates once around the fixed points in the  $(v, u)$ -plane in an almost circular fashion before returning to the point it started at, or multiple-loop limit cycles, in which a trajectory rotates several times around the fixed points in the  $(v, u)$ -plane before returning to the point it started at.

However, unlike the case in [7], the frequency of these limit cycles is not fixed, and depends on the gain coefficients  $K_p$  and  $K_i$ , as well as the position of the reference voltage with respect to the fixed points.

#### A. Possible amplitudes and frequencies of limit cycles

We will consider a single-loop limit cycle rotating around fixed points in the  $(v, u)$ -plane. If the trajectory is  $P$  iterations long, then the frequency of oscillation will be  $\omega_{\text{osc}} = \frac{2\pi}{PT_s}$ . While a single-loop limit cycle is obviously constrained to having integer values of  $P$ , in a multiple-loop limit cycle the number of iterations it takes to rotate around the fixed points may vary from loop to loop, and thus the average number of iterations may not necessarily be integer. We will therefore consider  $P$  real, rather than integer, in what follows. We consider a trajectory as in Fig. 3 starting at the switching point to the right of the zero-error bin, winding first around the left fixed point and then around the right fixed point and we recall that the distance between two adjacent fixed points is approximately  $[1, \delta_u]^T \tilde{q}$ . The trajectory takes the form

$$\tilde{W}_1 = e^{p_1 T_s A} \tilde{W}_0 \quad (8)$$

$$\tilde{W}_2 = e^{(P-p_1) T_s A} \tilde{W}_1 - e^{(P-p_1) T_s A} [1, \delta_u]^T \tilde{q} \quad (9)$$

where  $\tilde{W}_n$  are switching points between duty-cycle levels. As  $\tilde{W}_2 = \tilde{W}_0 - [1, \delta_u]^T \tilde{q}$ , we have that

$$\tilde{W}_0 = [I - e^{PT_s A}]^{-1} [I - e^{(P-p_1) T_s A}] [1, \delta_u]^T \tilde{q} \quad (10)$$

As  $\tilde{v}(p) = e^{-p\sigma T_s} (\cos(p\omega T_s) \tilde{v}_0 + \sin(p\omega T_s) \tilde{u}_0)$ , we see that the peak voltage of this trajectory will occur when  $\frac{d\tilde{v}(p)}{dp} = 0$ . Solving this equation, we find that

$$p_{\text{pk}} = \frac{1}{\omega T_s} \tan^{-1} \left[ \frac{1 - \frac{\sigma}{\omega} \frac{\tilde{v}_0}{\tilde{u}_0}}{\frac{\tilde{v}_0}{\tilde{u}_0} + \frac{\sigma}{\omega}} \right] \quad (11)$$

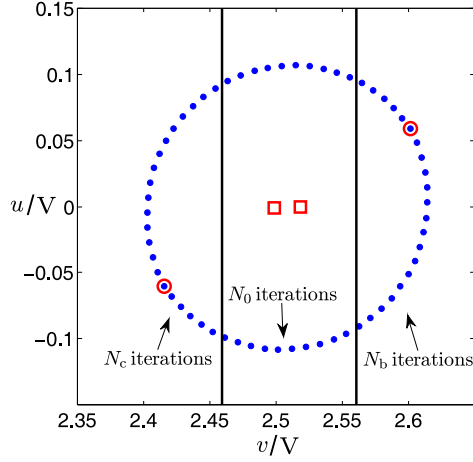


Fig. 3. Limit cycle in the  $(v, u)$ -plane. Trajectory marked in blue dots, switching points marked in red circles, zero-error bin boundaries marked in vertical black lines. Equilibrium points in red squares.

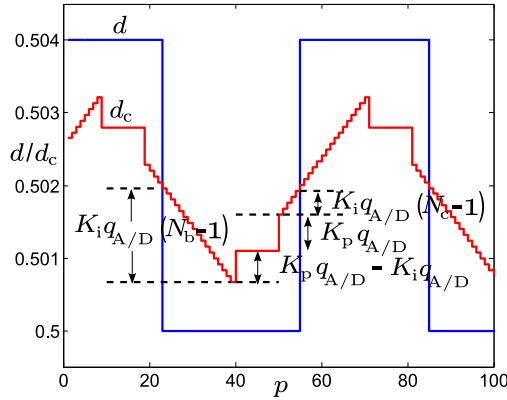


Fig. 4.  $d$  (in blue) and  $d_c$  (in red) versus  $p$  for limit cycle in Fig. 3.

So, by specifying a number of iterations  $P$ , which determines the frequency of oscillation of a limit cycle, we may find the switching point to the right of the zero-error bin from (10) by varying  $p_1$ . Using  $(\tilde{v}_0, \tilde{u}_0)$  from (10) in (11), we find the amplitude of a limit cycle at frequency  $\omega_{osc}$  as

$$r = e^{-p_{pk}\sigma T_s} (\cos(p_{pk}\omega T_s)\tilde{v}_0 + \sin(p_{pk}\omega T_s)\tilde{u}_0) - \frac{\tilde{q}}{2} \quad (12)$$

If  $V_{ref}$  is placed such that the fixed points are symmetrical about  $V_{ref}$ , then we see that the amplitude of a limit cycle at a certain frequency is at its largest. As  $V_{ref}$  moves away from this point, the amplitude of the limit cycle decreases, until a point is reached at which limit cycles are no longer possible. We note that as  $p_1$  increases, the switching point moves closer to the zero-error bin boundary, and the amplitude of the limit cycle decreases. If we assume that the limit cycle remains approximately symmetrical about  $V_{ref}$ , then the smallest possible limit cycle for a particular value of  $P$  will occur when we have that  $\tilde{v}_0 = \frac{q_{A/D}}{2} - \frac{q_{DPWM}V_{in}}{2}$ .

### B. Relationship of limit cycles to gain coefficients

If we consider a limit cycle on two duty cycle levels confined to the  $\pm 1$  and 0-error bins, as shown in Fig.3, then we seek to find a relation between the amplitude and frequency and the controller gains. If we have  $N_b$  iterations in the  $+1$

error bin after the right switching point, with  $N_0$  iterations in the zero-error bin, and  $N_c$  iterations in the  $-1$ -error bin before the left switching point, and we consider the excursion of this limit cycle in  $d_c$  as shown in Fig 4, we see that

$$K_i(N_b - 1)q_{A/D} = 2K_p q_{A/D} - K_i q_{A/D} + K_i(N_c - 1)q_{A/D}$$

which we rearrange to find

$$\frac{K_p}{K_i} = \frac{N_b - N_c + 1}{2} \quad (13)$$

We have that  $N_b + N_0 + N_c = p_1$ , and so we find that

$$\frac{K_p}{K_i} = \frac{2N_b + N_0 + 1 - p_1}{2} \quad (14)$$

We may approximate  $N_b$  and  $N_0$  as angles in the  $(v, u)$ -plane as follows

$$N_b = \frac{\cos^{-1} \frac{q_{A/D}}{2r} + \cos^{-1} \frac{\tilde{v}_0 - 0.5q_{DPWM}V_{in}}{r}}{\omega_{osc}T_s} \quad (15)$$

$$N_0 = \frac{\pi - 2\cos^{-1} \frac{q_{A/D}}{2r}}{\omega_{osc}T_s} \quad (16)$$

Using these relations in (14), we find

$$\frac{K_p}{K_i} = \frac{1}{2} \left[ \left( 2\cos^{-1} \frac{\tilde{v}_0 - \frac{\tilde{q}}{2}}{r} + \pi \right) \frac{P}{2\pi} + 1 - p_1 \right] \quad (17)$$

So, we see that it is the ratio of  $\frac{K_p}{K_i}$  which is important in determining the amplitude and frequency of the limit cycles seen in the system, rather than the absolute values, provided of course, that the excursion in  $d_c$  does not overlap to another DPWM quantization bin. We note that as we are continuing the approximation that  $P$  and  $p_1$  are real, we are considering real values of  $N_b$ ,  $N_c$  and  $N_0$  here, whereas in reality these values will all be integer. Therefore rather than having a single value of  $\frac{K_p}{K_i}$  at which a particular limit cycle is possible, the same limit cycle will be possible over a limited range of values.

However, if the first points once the trajectory leaves the zero-error bin are the points at which switching occurs then the switching in the limit cycle occurs only due to the proportional gain, as shown in Fig. 5. We have that the distance between the two values of  $d_c$  just before the duty cycle level changes is  $K_i N_1 q_{A/D}$ , where  $N_1$  is the number of iterations the trajectory spends on one side of the zero-error bin. Provided that the two values of  $d_c$  are symmetrical about the quantization boundary, then the value of  $K_i$  can be made arbitrarily small and it will still be possible for this limit cycle to exist, provided the necessary symmetry exists in the system. Thus, we cannot guarantee that limit cycle oscillations on two duty cycle levels will not occur simply by adjusting the gain coefficients in the system.

We plot in Fig. 6 the predicted amplitude versus frequency range from (10), (11) and (12) and we plot in Fig. 7 the corresponding predicted value of the amplitude versus  $\frac{K_p}{K_i}$  from (17). In both plots the top black lines are for the maximum output amplitude, which will happen when  $V_{ref}$  is close to being halfway between two fixed points, and the bottom black lines are for the smallest amplitude limit cycles possible, which are found by letting the switching point  $\tilde{v}_0$  lie on the edge of the zero-error bin, i.e.  $\tilde{v}_0 = \frac{q_{A/D}}{2} + \frac{\tilde{q}}{2}$ . We

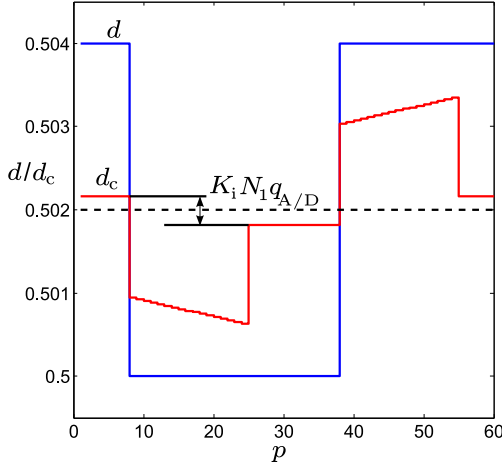


Fig. 5. Representative plot of  $d$  (in blue) and  $d_c$  (in red) versus  $p$  for a limit cycle where switching occurs only due to the proportional term. Quantization boundary shown in dashed black line.

see, therefore, that a range of amplitudes are possible at a particular frequency, and the smallest amplitude possible at that frequency is dependent on  $q_{A/D}$ . Values from simulation show a relatively good match with the possible amplitudes and frequencies of limit cycles, as well as the possible range of  $\frac{K_p}{K_i}$  at which these can occur. In general, we see that increasing the value of the ratio  $\frac{K_p}{K_i}$  leads to a decrease in the amplitude and frequency of the limit cycles which may exist. We note that even with large values of  $\frac{K_p}{K_i}$ , limit cycles may still exist, owing to switching occurring as in Fig. 5.

In order to prevent a limit cycle on two duty cycle levels from being possible, therefore a sufficient condition is that the largest amplitude limit cycle is confined to being within the zero-error bin, as was found in [7]. The peak-to-peak largest amplitude limit cycle is approximately given by  $\frac{1+e^{-\frac{\pi\sigma}{\omega}}}{1-e^{-\frac{\pi\sigma}{\omega}}} q_{DPWM} V_{in}$  (which is found by letting  $P = 2p_1 = \frac{2\pi}{\omega T_s}$  in (10) which yields  $p_{pk} \approx 0$ ) and thus the condition

$$q_{A/D} > \frac{1 + e^{-\frac{\pi\sigma}{\omega}}}{1 - e^{-\frac{\pi\sigma}{\omega}}} q_{DPWM} V_{in} \quad (18)$$

must be satisfied in order to prevent limit cycles on two duty cycle levels occurring.

#### IV. CONCLUSION

We have developed an analytical model of a digitally controlled buck converter in order to predict the possible frequency and amplitude of limit cycles on two duty cycle levels which occur in the system. We have also related this frequency and amplitude to the controller gains  $K_p$  and  $K_i$ , and shown that it is the ratio of these values which is important in determining whether or not a limit cycle may occur in the system. We have then verified our predictions through simulation. We have also shown that it is not possible to guarantee that limit cycles on two duty cycle levels will not occur by only adjusting the gain coefficients, and we have given a bound in terms of the system parameters which will prevent limit cycles on two duty cycle levels from occurring.

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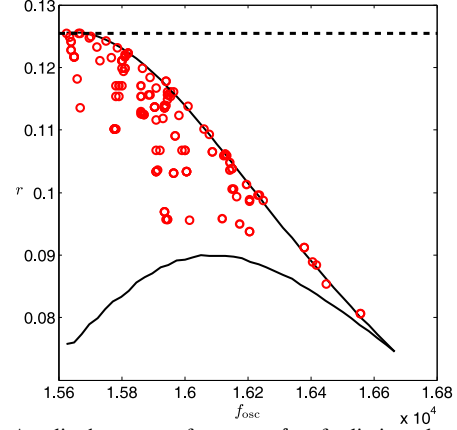


Fig. 6. Amplitude  $r$  versus frequency  $f_{osc}$  for limit cycles on two duty cycle levels. Predicted bounds are given by black lines. Values from simulation are given in red circles. Parameters are  $V_{in} = 5$  V,  $T_s = 1\mu s$ ,  $q_{A/D} = 0.101$  V,  $q_{DPWM} = 0.004$ ,  $r_c = 0.02\Omega$ ,  $C = 13.52\mu F$ ,  $L = 7.62\mu H$ ,  $R = 10\Omega$ , which yields  $\sigma = 5000$  s $^{-1}$  and  $\omega = 98.3$  krad s $^{-1}$ .  $V_{ref}$  and  $K_p/K_i$  are varied in order to find a range of amplitudes and frequencies of limit cycles. Bound from (18) in dashed black line.

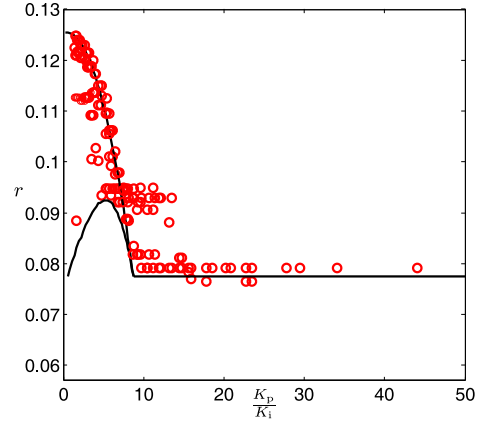


Fig. 7.  $r$  versus  $\frac{K_p}{K_i}$  corresponding to Fig. 4. Predicted bounds from (17) are given by curved black lines, while horizontal black line indicates the predicted amplitude of oscillations when switching occurs only from the proportional action of the controller, as in Fig. 5. Values from simulation in red circles.

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