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<td>Nikandish, Gholamreza, Staszewski, Robert Bogdan, Zhu, Anding</td>
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A Fully Integrated Reconfigurable Multi-Mode Class-F$_{2,3}$ GaN Power Amplifier

G. Reza Nikandish, Member, IEEE, R. Bogdan Staszewski, Fellow, IEEE, and Anding Zhu, Senior Member, IEEE

Abstract—In this paper, we propose a reconfigurable multi-mode fully integrated power amplifier (PA) in GaN technology. The PA is composed of one main transistor, biased in class-AB, and three auxiliary transistors which can be switched between class-AB and deep class-C, to improve efficiency and linearity of the PA. Furthermore, a harmonic termination network is proposed to enable operation of the PA in class-F$_{2,3}$. A proof-of-concept PA, fabricated using a 250-nm GaN-on-SiC process, provides 33.8 dBm output power and 42% peak drain efficiency (DE) at 4.8 GHz. Modulated-signal measurements using a 200-MHz 256-QAM 7.2-dB peak-to-average power ratio (PAPR) signal indicate that rms error vector magnitude (EVM$_{\text{rms}}$) $< 5\%$ (−26 dB) can be achieved with 27.7–28.5 dBm average output power, 26–30% average DE, and −38.1 to −33.5 dBc adjacent channel leakage ratio (ACLR), in the four operation modes. It is shown that ACLR can be improved by 6 dB at lower output power levels through reconfiguring the mode of PA operation.

Index Terms—5G, class-F, GaN, multi-mode, power amplifier (PA), reconfigurable PA, wideband modulation.

I. INTRODUCTION

MULTI-MODE power amplifiers (PAs) can enhance their performance through reconfigurable active devices and matching networks [1]–[4]. This enables efficient operation of the PA in variable working conditions, e.g., changing distance between a user equipment and access point, where a wide range of output power should be delivered with high efficiency and linearity. In the 5G communications, complex-modulated signals with high peak-to-average power ratio (PAPR) and wide modulation bandwidth, e.g., 100–200 MHz in sub-6 GHz bands, are used and that imposes stringent linearity requirements on the PA in all operational modes.

In this paper, we propose a multi-mode PA architecture with reconfigurable active cells and a harmonic termination network enabling operation in class-F$_{2,3}$. A fully integrated GaN PA is implemented as a proof-of-concept. It can be used in a more complex architecture, e.g., a digital transmitter, to control the structure based on operating conditions or input signal power.

II. RECONFIGURABLE MULTI-MODE PA

A. PA Architecture

The circuit schematic of the proposed reconfigurable multi-mode class-F$_{2,3}$ PA is shown in Fig. 1. The PA is composed of a main transistor $M_1$ and three auxiliary transistors $M_{2,3,4}$.

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B. Class-\(F_{2,3}\) Operation

Efficiency of the PA can be improved by the proper harmonic terminations to shape the drain current and voltage waveforms. In the class-\(F_{2,3}\) mode used in this design, the drain current is shaped towards a square-wave with faster transitions and lower overlap with the drain voltage waveform. The output matching network shown in Fig. 1 can provide the required load impedances for the class-\(F_{2,3}\) operation. By choosing the resonant frequency of the network \(L_{1a}||C_1\) to be smaller than \(2f_0\), it appears as a capacitance at \(2f_0\) which along with \(L_{1a}\) can provide a short-circuit at this frequency. The network composed of \(L_1\) and \(C_1\) operates as an inductance at \(3f_0\) which can resonate with the output-referred capacitance of the power cell \(C_{out}\). Considering that the network \(L_{2a}||C_2\) resonates at \(3f_0\), an open-circuit impedance is achieved at this frequency. The circuit appears as an inductive \(\pi\) network at \(f_0\), which can transform \(R_L\) to \(R_{opt}\) (in both cases of \(R_{opt} > R_L\) and \(R_{opt} < R_L\)) and compensate \(C_{out}\).

A major concern in this reconfigurable PA structure is whether the described conditions can be maintained in all the operational modes, or if violated, whether the acceptable PA performance can still be obtained. The two parameters \(R_{opt}\) and \(C_{out}\) should be checked in the four operational modes. It is noted that the short-circuit condition at \(2f_0\) is controlled by \(L_1\) and \(C_1\) which is independent of the operational mode.

C. Mode Reconfiguration

The relative size of the main and auxiliary transistors \((W_m/W_a)\) and the number of operational modes \((N)\) are determined based on the target range of output power and the number of steps. Ratio of the lowest output power level (when only the main transistor is active) to the highest output power level (when all the transistors are active) is roughly given by

\[
P_{out,min} \approx \frac{W_m}{W_m + (N-1)W_a}. \tag{1}
\]

In this design with \(N = 4\) operational modes, we choose the size of transistors as \(W_m = 6 \times 125 \mu m\) and \(W_a = 2 \times 125 \mu m\), to achieve an output power ratio of 2, while \(P_{out,m} = 34.2\) dBm and \(P_{out,a} = 28.5\) dBm. A 250-nm GaN-on-SiC process used for the implementation.

The optimum load resistance that should be synthesized by the output matching network is given by

\[
R_{opt} = R_{opt,m} \left| \frac{R_{opt,a}}{N - 1} \right. \tag{2}
\]

where \(R_{opt,m}\) and \(R_{opt,a}\) respectively denote the optimum load resistance of the main and auxiliary transistors. In this design, \(R_{opt} = 92\Omega\) is derived using (2) with \(R_{opt,m} = 207\Omega\) and \(R_{opt,a} = 500\Omega\). Thus, the resonant frequency of the network \(L_{1a}||C_1\) is set at \(f_0\) so that the inductive \(\pi\) network be simplified to an L-section network which scales up the 50-\(\Omega\) load impedance to 92-\(\Omega\) optimum load resistance. It should be mentioned that the transmission lines used in the output power combiner of Fig. 1 introduce parasitic inductances which can alter the optimum load impedance presented to the transistors, thus leading to asymmetric power combining (e.g., between \(M_{2,4}\) and \(M_3\)). These effects are considered in simulations, indicating that (2) can still provide a good rough estimation (within 10% error).

Parasitic capacitances of the transistors can change with the operational mode. The gates-source capacitance can be approximated by a hyperbolic function of gate-source voltage, increasing from \(C_{gs,l}\) in class-C to \(C_{gs,h}\) in class-AB. Therefore, the input capacitance of the combined transistors in the mode \(k\) is given by

\[
C_{in}(k) = C_{gs,h,m} + (k-1)C_{gs,h,a} + (N-k)C_{gs,l,a}. \tag{3}
\]

In this GaN process \(C_{gs,l} \approx 0.56C_{gs,h}\), therefore, the input capacitance can change by a factor of \(C_{in,max}/C_{in,min} = 1.28\). This should be considered in the design of input matching network. It is noted that in mode 1 where all auxiliary transistors are biased in deep class-C, the main (class-AB) and auxiliary transistors appear as parallel devices with expansive and compressive nonlinearity characteristics, a feature which can reduce AM-PM distortion of the PA [5].

Furthermore, drain-source capacitance of the transistors slightly changes with their gate-source voltages, decreasing from \(C_{ds,h}\) in class-C to \(C_{ds,l}\) in class-AB. e.g., in this process \(C_{ds,l} \approx 0.91C_{ds,h}\). The output capacitance of the combined transistors is given by

\[
C_{out}(k) = C_{ds,l,m} + (k-1)C_{ds,l,a} + (N-k)C_{ds,h,a}. \tag{4}
\]

leading to \(C_{out,max}/C_{out,min} = 1.05\). The change in the center frequency is only 2% (here, \(\approx 100\) MHz) which is negligible. In high output power levels, average drain-source capacitance should be considered in the analysis which approaches the same value in all the modes. The output capacitance remains thus almost constant (for any \(k\)) when the auxiliary transistors change their state,

\[
C_{out} \approx C_{ds,m} + (N-1)C_{ds,a}. \tag{5}
\]

Therefore, the two conditions \(Z_L(2f_0) = 0\) and \(Z_L(3f_0) = \infty\) for class-\(F_{2,3}\) operation are substantially satisfied in all operational modes. Using (4) with \(C_{gs,m} = 0.35\) pF and \(C_{ds,a} = 0.1\) pF, \(C_{out} = 0.65\) pF is derived (Fig. 1). It should be mentioned that the output combiner effects neglected in this discussion are considered in circuit simulations.

D. Efficiency and Linearity Enhancement

The proposed reconfigurable structure can improve the PA performance, e.g., efficiency and linearity, by enabling control of the auxiliary transistors. How this reconfiguration can be used to improve the performance is dependent on the relative size and bias of transistors. A size ratio of \(W_a/W_m = 1/3\) is chosen, as discussed above. The effect of bias current is illustrated in Figs. 2 and 3, where drain efficiency (DE), gain, AM-AM, and AM-PM versus output power in the four operational modes are shown in three cases of low, moderate, and high bias currents (13, 66, and 233 mA). The bias current is reported in mode 4 where all transistors are active. The frequency of operation is 4.8 GHz. A close investigation of these plots reveals some special features of this structure.

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1Derived design equations for the circuit components cannot be included here due to limited space.
In Fig. 2, it is noted that DE is reduced at the high bias current (class-A bias). In this case, DE can be improved in back-off (e.g., by 1.6×) by turning off the auxiliary transistors to reduce the DC current [Fig. 2(c)]. However, such efficiency improvement cannot be achieved in lower bias currents as the DC current is mainly determined by the signal amplitude (class-B bias). Another feature of the high bias current condition is a higher and more linear gain. A fairly linear gain can also be achieved in the low bias current [Fig. 2(a)], but the gain is too low, which degrades power-added efficiency (PAE) (not shown here). Therefore, the high bias current can provide the best performance in the applications where gain linearity is the primary requirement.

In Fig. 3, AM-AM and AM-PM characteristics are shown in the three bias conditions. The low bias current condition leads to the lowest AM-AM but very large AM-PM. The moderate bias provides the lowest AM-PM, while its AM-AM is only 0.5 dB larger than in the high bias. Furthermore, in Fig. 3(b) it is noted that AM-PM can be improved by reconfiguring from mode 4 to 1 (as a result of nonlinearity cancellation of the main and auxiliary transistors). Therefore, the moderate bias current can lead to the optimized amplitude and phase linearity.

Simulated $S$ parameters and µ stability factor of the PA in the four modes of operation are shown in Fig. 4 (moderate bias current). We note that $S_{21}$ can be controlled within 10.7–14.3 dB, while $S_{11}$ changes from $-8$ dB (mode 1) to $-12$ dB (mode 4), which relaxes the aforementioned concern of the input capacitance varying due to the mode switch-overs. The stability factor is higher than 1 in all the modes.

The proposed PA is fabricated in a 250-nm GaN-on-SiC process from WIN Semiconductors. The chip micrograph is shown in Fig. 5. The chip die is wire-bonded to the test PCB for measurements. The PA is supplied at 28 V and draws 62 mA quiescent current.

Measured output-input power characteristic, gain, and DE versus output power are shown in Fig. 6. The saturated output power is 33.8 dBm. Gain is within 7.6–12.1 dB in low output power and 5.6–9.6 dB at 33 dBm output power, corresponding to $\sim$2–4 dB gain compression. Measured peak DE reads 37–42% in the four modes.

Modulated-signal measurements are performed using a 256-QAM signal with wide bandwidth of 200 MHz to evaluate the PA performance for high data-rate 5G applications. Achieving a good linearity under such a wide bandwidth is challenging due to increased dynamic nonlinearity and charge-trapping effects in GaN HEMT devices. In Fig. 7,
We propose a reconfigurable multi-mode power amplifier (PA) architecture. The operational mode can be changed through switching of the gate biasing of three auxiliary transistors between deep class-C and class-AB, which are working in parallel with a main transistor biased in class-AB. Using this architecture, gain, output power, efficiency, and linearity can be controlled to improve the PA performance.

### IV. Conclusion

Table I compares the proposed PA to relevant state-of-the-art fully integrated GaN PAs. Performance of the other PAs is reported at the closest frequency to that of our design, which to the best of authors’ knowledge has not yet been disclosed in the literature. For a wideband 200-MHz 256-QAM signal, our PA achieves 30% average DE and < 5% $EVM_{\text{rms}}$.

#### REFERENCES


#### TABLE I

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<tr>
<th>Oper. Mode</th>
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