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Authors(s)	Nikandish, Gholamreza, Staszewski, Robert Bogdan, Zhu, Anding
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The (R)evolution of Distributed Amplifiers: From Vacuum Tubes to Modern CMOS and GaN ICs

Gholamreza Nikandish, *Member, IEEE,* Robert Bogdan Staszewski, *Fellow, IEEE,* and Anding Zhu, *Senior Member, IEEE*

I. Introduction

BROADBAND amplification of signals is desirable in many applications such as high-speed data communications, high-resolution imaging systems, optoelectronics and instrumentation systems. Wide bandwidth is one of the prominent factors to be considered in designing such a system since it determines ability of the system for transferring high-data-rate information, transmitting/receiving short pulses, or processing wideband signals. Designing broadband amplifiers has always been challenging. The ever-increasing demand for higher data-rates and low energy consumption in next generation communication systems further complicates the design of broadband amplifiers.

Distributed amplifiers (DA), also known as travelling-wave amplifiers (TWA), are one of the most popular broadband amplifier architectures. The DA architecture was originally patented by Percival in 1936 [1] and later elaborated by Ginzton in 1948 [2]. The early DAs were implemented using vacuum tube technology. One of the first vacuum tube DAs fabricated in 1950 is shown in Fig. 1. The amplifier included three type 807 tubes and 482-Ω plate and grid lines. The amplifier achieved a gain of 11 dB, bandwidth of 100 Hz to 300 MHz, and a typical output power of 15 W [3].

The first Monolithic Microwave Integrated Circuit (MMIC) DA was demonstrated by Ayasli in 1982 [4] using a Gallium Arsenide (GaAs) MESFET technology. The amplifier, shown in Fig. 2, included four transistors with 1-μm gate length and 50-Ω input and output lines. It achieved 9-dB gain and 1–13 GHz bandwidth. GaAs remained the main technology for design of DAs until the inception of the first Indium Phosphide (InP) DA in 1990 [5] with an impressive bandwidth of 5–100 GHz. GaAs and InP semiconductor technologies have been predominantly employed in implementation of DAs. These technologies provide superior performance resulting from their high electron mobility, high saturated electron velocity, high breakdown voltage, and high-resistivity substrate. The later contributes to availability of low-loss integrated passive elements.

The market demands for low cost, small size, and low power consumption of electronic systems has motivated researchers to develop techniques to implement distributed amplifiers using mainstream CMOS technologies. The first integrated CMOS DA was presented by Kleveland in 1999 [6]. Recently,

The authors are with the School of Electrical and Electronic Engineering, University College Dublin, Ireland (nikandish@ucd.ie, robert.staszewski@ucd.ie, anding.zhu@ucd.ie).

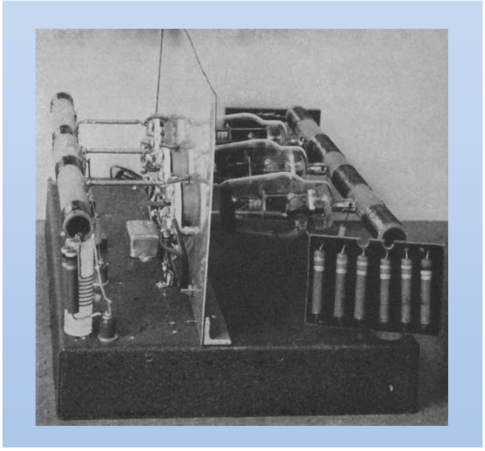

Fig. 1. A vacuum tube DA fabricated in 1950. It achieved 11-dB gain and 100 Hz to 300 MHz bandwidth [3].

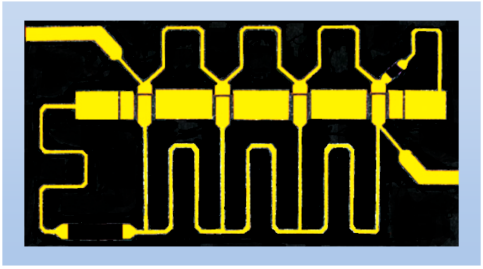

Fig. 2. The first MMIC DA implemented in a 1-μm GaAs MESFET technology, with 9-dB gain, 1–13 GHz bandwidth, and 2.5 mm × 1.65 mm chip size [4].

DA chips designed using Gallium Nitride (GaN) technologies have been developed to provide high output power over a wide bandwidth.

It is noteworthy that the distributed architecture can also be adopted in other circuits to achieve broad bandwidth [7]. Examples include oscillators [8], power amplifiers [9], [10], mixers [11], phase shifters [12], as well as power combiners and splitters [13], [14]. Transversal filters are another important circuit type that has been implemented using distributed architectures for application in broadband optical communications [15], [16].

Through the years, many circuit techniques have been developed to improve performance of DAs in different technologies. A review of the most important circuit developments and state-of-the-art performance achieved in each process will be presented in this paper.

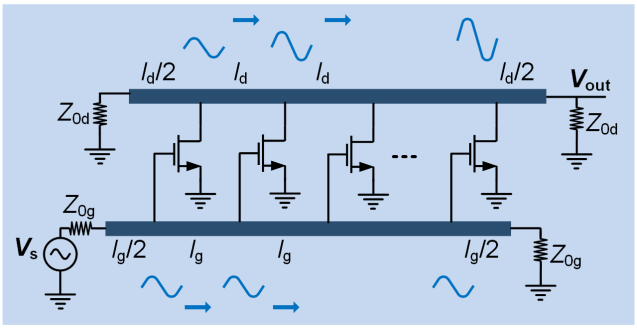

Fig. 3. The basic architecture of a distributed amplifier.

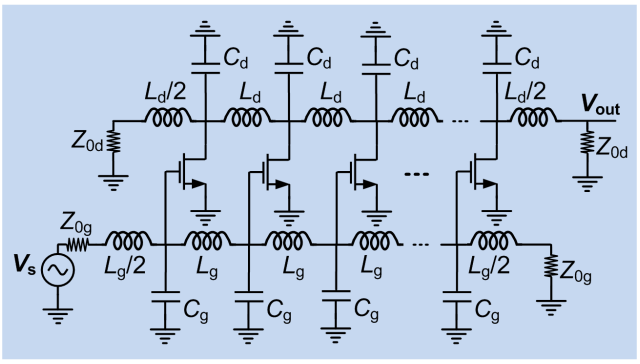

Fig. 4. The DA architecture based on lumped-element artificial transmission lines.

II. Operation Principles

The basic architecture of a distributed amplifier is shown in Fig. 3 where a cascade of identical transistors have their gates connected to a transmission line with a characteristic impedance Z_{0g} and a length l_g, while the drains are connected to a transmission line having a characteristic impedance Z_{0d}, with a length l_d. The key idea of this architecture is to operate multiple transistors in cascade to increase the gain and simultaneously absorb their parasitic capacitances into the gate and drain transmission lines to achieve a wide bandwidth. The input voltage wave propagates through the gate line and reaches the gate of the transistors with phase shifts. Each transistor amplifies its gate voltage and generates a drain current propagating through the drain line. If the gate and drain line sections provide same phase shifts, i.e.,

$$\beta_g l_g = \beta_d l_d, \tag{1}$$

where β_g and β_d is the propagation constant of the gate and drain line, respectively, the drain current waves reach the load impedance and constructively add. The gate and drain lines are terminated in their loaded characteristic impedance at the other end to absorb waves traveling in the reverse directions.

Assuming the transconductance gain of each device is G_m and the output impedance seen by each transistor is half the characteristic impedance of the transmission line, the voltage gain of the DA is thus derived as

$$A_v = \frac{1}{2} n G_m Z_{0d} \tag{2}$$

where n is the number of stages and Z_{0d} is characteristic impedance of the drain line [2]. The gain of the DA can be increased by using more gain stages n or higher transconductance G_m. Z_{0d} is set by the output impedance matching condition. It should be noted that (2) is derived assuming lossless transmission lines. Considering loss of transmission lines, the voltage wave amplitude attenuates when passing through the gate and drain lines. This effect tends to degrade the voltage gain when using more gain stages. Thus, there is an optimum number of gain stages that maximizes the voltage gain [17].

The circuit model of Fig. 3 is based on the assumption that parasitic capacitances of the transistors are uniformly distributed along the transmission lines. Although fairly accurate to describe the DA operation and derive its voltage gain for practical number of gain stages, this model cannot provide a realistic estimation of the DA bandwidth. The DA can also be modeled by lumped-element artificial transmission lines as shown in Fig. 4. The DA analysis based on this model has been presented in literature [17], [18]. The condition (1) is modified as

$$L_g C_g = L_d C_d, \tag{3}$$

where C_g and C_d are capacitances at the gate and drain of each transistor, while L_g and L_d denote the inductance of the gate and drain line sections, respectively. The bandwidth of the DA is limited by the cut-off frequency of the gate and drain lines. It is shown that the cut-off frequency is given by

$$\omega_c = \frac{2}{\sqrt{LC}} \tag{4}$$

where L and C are the inductance and capacitance of the lumped-element line, assuming that gate and drain lines have the same cut-off frequencies. The wave propagating through the lumped-element line experiences significant attenuation beyond the cut-off frequency. In order to achieve a high bandwidth, small transistors should be used, but, this lowers the gain of the DA. As the ratio L/C determines the characteristic impedance of the lines, inductance L cannot be made arbitrarily small to achieve higher bandwidth. Thus, there is a trade-off between gain and bandwidth of the DA.

III. Circuit Developments

A. DA Using Improved Gain Stages

The input capacitance of transistors is the largest parasitic capacitance that limits bandwidth of the DA. Capacitive coupling is a solution proposed in [21] to mitigate the loading effect of the gate-source capacitance on the gate line. A capacitor is placed in series with the gate of transistors to reduce the effective capacitance to $C_{gs}/(1 + C_{gs}/C_c)$ [Fig. 5(a)]. A large resistor in parallel with C_c provides a path for the gate bias. It is noted that voltage gain is also reduced by the factor $1 + C_{gs}/C_c$ due to voltage division at input of transistors. This technique is usually adopted in distributed power amplifiers where the gate-source capacitance of large transistors can limit bandwidth and gain is not the primary design concern [22]-[24].

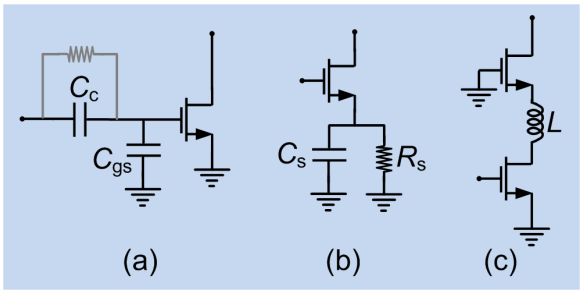

Fig. 5. The most conventional circuit architectures used as gain stage of DAs. (a) Capacitive coupling to reduce input capacitance of the transistors, (b) Source RC degeneration to reduce input capacitance of the transistors and compensate losses arising from input resistance of the transistors as well as transmission lines, (c) Bandwidth-enhanced cascode amplifier to improve reverse isolation.

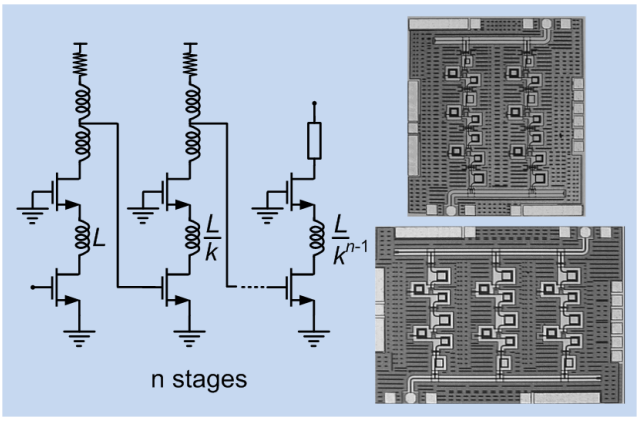

Fig. 6. The DA architecture using multi-stage amplifier with bandwidth enhancement and stagger-tuning technique proposed by [36]. Two DA versions are designed in a 0.18-μm CMOS process.

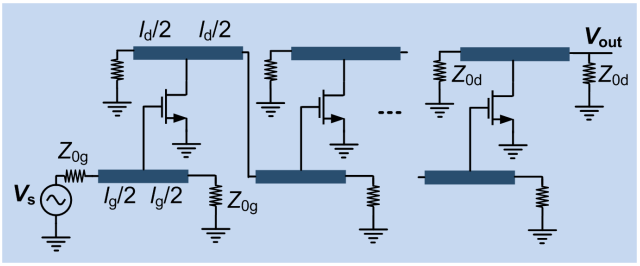

Fig. 7. The cascaded single-stage DA architecture.

Another technique developed to reduce the loading effect of the transistors input impedance is using a common-source amplifier with RC degeneration [Fig. 5(b)] as the gain stage [25]-[31]. The input impedance of the amplifier is derived as a series resistance and capacitance. i.e. $Z_{in} = R_{in} + 1/j\omega C_{in}$. By proper setting of the circuit elements, the amplifier parameters are derived as $R_{in} = 0$, $C_{in} = C_{gs}/(1 + g_m R_s)$, and $G_m = g_m/(1 + g_m R_s)$. Thus, the input capacitance is reduced, at the cost of degraded transconductance. In practice, the circuit elements are set to achieve negative input resistance. It can be used to compensate loss of the gate transmission line and input parasitic resistance of the transistor. The Darlington amplifier can also provide a similar input impedance [32].

The cascode amplifier shown in Fig. 5(c) is a popular architecture used to provide high isolation between input and output of the DA. The inter-stage inductance moves the pole associated with the inter-stage parasitic capacitance to higher frequencies, and hence, improves bandwidth. Other techniques to compensate the effects of loss and parasitic capacitance of transistors are presented in [33]-[35].

In order to improve the gain of the DA, multi-stage amplifiers are adopted as the gain stage [27], [36]-[39]. Bandwidth enhancement techniques [40], [41] can be employed to avoid bandwidth limitation by inter-stage parasitic capacitances. The multi-stage amplifier proposed by [36] is shown in Fig. 6. The stagger-tuning technique is used in the multi-stage amplifier to improve gain flatness of the DA. The amplifier stages have slightly different 3-dB bandwidths and gain peaking near the cut-off frequency. The amplifier stages are properly adjusted to provide an overall flat gain response. To this end, the inter-stage inductance is scaled down by the factor $k = 1.3$ from the first toward the last stage. Using this technique, two DAs are designed in a 0.18-μm CMOS process (Fig. 6). The first DA comprises three gain stages using three cascaded amplifiers, achieving 16.2 dB gain and 33.4 GHz bandwidth. The second DA comprising two gain stages using four cascaded amplifiers achieves 20 dB gain and 39.4 GHz bandwidth.

B. Cascaded DAs

Similar to other amplifier architectures, multiple DAs can be cascaded to achieve higher gain. The cascaded single-stage DA (CSSDA) is an architecture developed to achieve high gain and wide bandwidth (Fig. 7) [42]-[44]. The parasitic capacitances of the transistors are absorbed in the transmission lines to achieve wide bandwidth, while gain stages are cascaded to increase overall gain. The inter-stage impedances can be chosen higher than the input and output impedances to achieve higher gain. In practice, as the number of transmission line sections is limited, this architecture does not inherit all features of a conventional DA such as wideband impedance matching and flat gain response.

A technique based on using internal feedback to improve the gain of the DA is proposed in [45]. A simplified amplifier architecture based on this technique is shown in Fig. 8. The signal amplified from port 1 to port 3 experiences the same gain as the signal going from port 4 to port 2. Thus, by providing a feedback between ports 3 and 4, the input signal is amplified twice to reach port 2. The input and output DA blocks are connected to this core DA block to provide impedance matching. The undesired gain from port 4 to port 3 is the reverse gain of the DA [2] which is low for the typical number of gain stages. This ensures stability of the DA with feedback. This technique is adopted to design a broadband DA with 74-GHz bandwidth and 19-dB gain in a 90-nm CMOS technology.

C. Matrix DAs

The matrix DA is a structure developed to achieve higher gain [46], [47]. A matrix DA with two rows is shown in Fig. 9. The matrix DA offers both additive and multiplicative

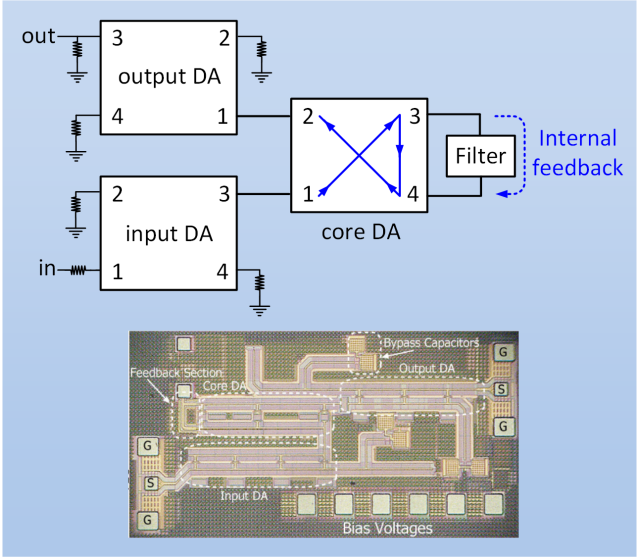

Fig. 8. The internal feedback technique proposed to improve gain of the multi-stage DA and chip photograph of the DA implemented in a 90-nm CMOS technology [45].

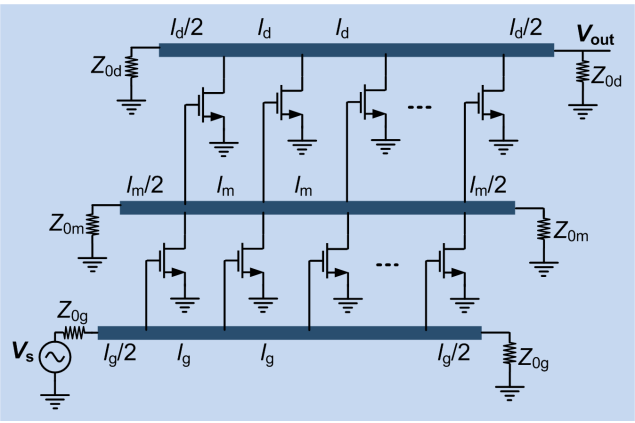

Fig. 9. The matrix DA architecture comprising two rows.

amplification to achieve wideband and high-gain operation. The gain of the matrix DA is higher than that of two cascaded DAs because both the forward and reverse waves in the middle line are amplified by the second row, while the reverse wave is absorbed by the drain line termination in a conventional DA. The characteristic impedance of the middle line Z_{0m} can be chosen higher than Z_{0g} and Z_{0d}, which are determined by impedance matching conditions, to improve gain of the matrix DA. More rows can be added to further improve the gain of matrix DAs.

D. DAs with Transformer Coupling

Using inductive coupling between inductors of the gate or drain line can improve the bandwidth of the DA (Fig. 10) [2], [49]. The negative inductive coupling between adjacent inductors of the line is used to modify its features. It is shown that characteristic impedance and cut-off frequency of the line are derived as $Z_0 = \sqrt{(1+k)L/C}$ and $\omega_c = 2/\sqrt{(1-k)LC}$, indicating that both features are improved

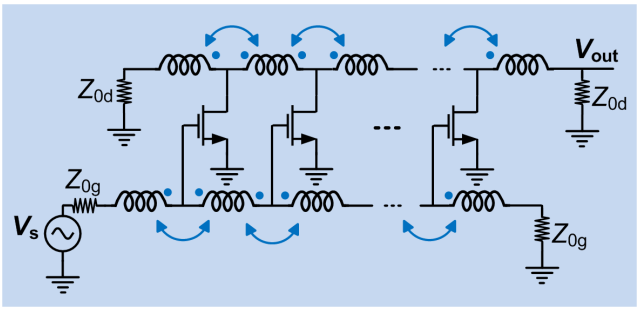

Fig. 10. The DA architecture with inductive coupling between inductors of the gate and drain line.

[2]. This allows using a smaller value of inductance to achieve the same characteristic impedance, while extending the cut-off frequency of the line.

The gate-drain capacitance of transistors is usually neglected in the DA analysis. In a DA, gate-to-drain voltage gain of the transistors increases from the first toward the last stage. As a result, the gate-drain capacitances experience nonuniform Miller multiplication. This lowers the characteristic impedance of the lines, decreases bandwidth, and leads to inter-symbol interference (ISI) in random data [50]. The gate-drain capacitance also degrades impedance matching and stability of the DA [17]. In advanced technologies with shorter gate length, the gate-drain capacitance exhibits other detrimental effects. The capacitance effects can be mitigated by using cascode amplifier as the gain stage. But, this entails its own issues such as reduced output voltage swing and noise contribution of the common-gate device at high frequencies. In [51], a technique is proposed to cancel the gate-drain capacitance over entire bandwidth of the DA. This technique is based on using transformer coupling between the gate and drain lines of the DA (Fig. 11). It is shown that the phase synchronization condition $L_g C_g = L_d C_d$ should be modified as

$$L_g(C_g + C_{gd}) = L_d(C_d + C_{gd}), \tag{5}$$

where C_{gd} is the gate-drain capacitance of each transistor. The optimum inductive coupling coefficient is derived as

$$k_{opt} = \frac{1}{\sqrt{\left(1+\frac{C_g}{C_{gd}}\right)\left(1+\frac{C_d}{C_{gd}}\right)}}. \tag{6}$$

The required coupling coefficient is low. Thus, it can be easily obtained over a wide bandwidth using edge-coupled microstrip lines or partially-overlapped loop inductors.

In [51], two DAs are designed using this technique and implemented in a 0.1-μm GaAs pHEMT process (Fig. 11). The first DA has an average gain of 10 dB and 3-dB bandwidth of 2–41 GHz. The DA layout is folded to save chip area. Spacing of the coupled line sections (50 μm) is determined based on the required coupling coefficient ($k_{opt} = 0.22$) derived using (6). Length and width of the gate and drain lines are tapered to improve DA performance. The second DA comprises cascade of two four-stage DAs and provides 19.2 dB average gain over 3-dB bandwidth of 2–39.5 GHz. As the gate-drain capacitance is neutralized, a common-source amplifier is used as the gain

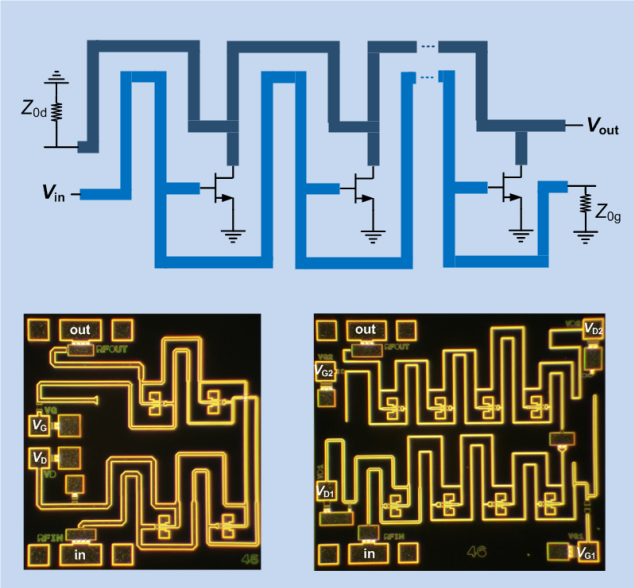

Fig. 11. Unilateralization of DA using transformer coupling between the gate and drain lines and the chips implemented in a 0.1-μm GaAs pHEMT technology [51].

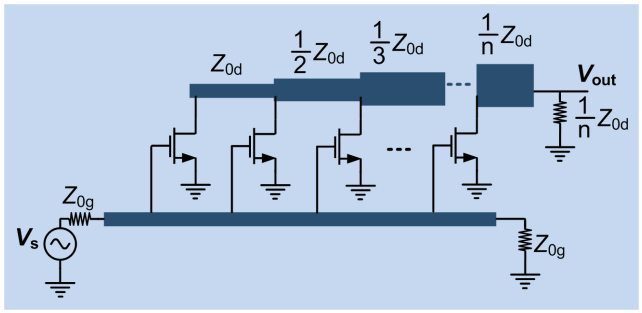

Fig. 12. The DA architecture with tapered width of the drain line sections. The tapered characteristic impedance of the drain line sections directs higher part of the drain currents toward the load impedance and improves output power and efficiency of the DA.

stage instead of the cascode amplifier. As a result, the DA can operate with supply voltages as low as 0.5 V to reduce power consumption, while its gain, bandwidth, and noise figure (NF) are maintained.

The transformer coupling between gate and drain lines has also been used to extend bandwidth of a DA using cascode gain stages [52]. Two DAs are designed using this technique in 0.18-μm and 90-nm CMOS technologies. The 0.18-μm CMOS DA provides a gain of 9.5 dB and 3-dB bandwidth of 32 GHz, while consuming 71 mW DC power. The 90-nm CMOS DA achieves gain of 7 dB, 3-dB bandwidth of 61.3 GHz, and consumes 60 mW DC power.

E. Nonuniform DAs

Nonuniform DA architectures can provide superior performance compared to a conventional uniform DA. Several nonuniform design techniques have been proposed including tapering the width of the drain line sections, tapering the length of the gate and drain line sections, and using unequal width of transistors.

The DA with tapered width of the drain line sections, or equivalently scaled characteristic impedance of the drain line, was first introduced in 1948 [2]. As shown in Fig. 12, the characteristic impedance of the drain line sections is scaled from Z_0 at the first section to Z_0/n at the last section. The drain line termination resistance is eliminated. In the conventional DA, the drain current wave of the transistors equally propagates toward the forward and reverse paths as the two paths exhibit the same impedance. However, in this DA structure, a larger part of the drain current wave propagates toward the forward path, improving forward gain and reducing reverse gain of the DA. This technique has been widely adopted in distributed power amplifiers to improve output power [22], [24], [53]-[56]. There are some issues, however, in implementation of this DA structure. For a large number of gain stages n, lines with very high characteristic impedance may be needed which may not be realizable. The output impedance matching may also be degraded due to reflections at the drain of transistors in absence of the drain termination resistance.

Tapering the length of the gate line sections is another technique to improve input impedance matching of the DA [57]. It is shown by gradually decreasing the length of the gate line sections, input impedance matching is improved while ripple in the gain of the DA is reduced. In [58], the length of the gate and drain line section are tapered to improve gain and bandwidth of the DA. In [59], a design technique for nonuniform DAs using filtering structures is proposed. The gate and drain lines are synthesized as low-pass filters. This technique allows better control over pass-band and stop-band frequency response of the DA.

Transistor width optimization is another nonuniform design technique that was first proposed in [48] to lower NF and power consumption of the DA. For a given total bias current, the optimally weighted DA can achieve lower NF compared to a conventional DA. A simplified architecture of the weighted DA is shown in Fig. 13. The width of the transistors gradually reduces from that of the first stage, reaching a minimum at the third stage, and then increases approaching the final stage. The inter-stage inductance is used to mitigate the effect of the interstage parasitic capacitance on bandwidth of the cascode amplifier. As the parasitic capacitances of the transistors are scaled proportional with their width, inductance values are scaled proportional to the inverse of the width to maintain constant bandwidth in all gain stages. The inductive coupling between inductors is used to improve the effective inductance of the gate and drain lines.

In [28], a design technique for distributed power amplifiers is proposed that adopts drain line impedance tapering and transistor width scaling to improve output power and efficiency. In a conventional DA, amplified signals at the drain line are add up constructively as they travel toward the load impedance [Fig.14(a)]. The largest voltage swing occurs at the last stage. By increasing the input power, the last stage saturates while preceding stages never reach this limit. Thus, the preceding stages contribute less to the output power while consuming the same bias currents. This degrades

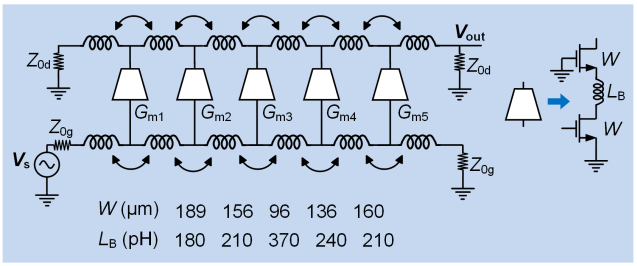

Fig. 13. The weighted DA architecture proposed to lower NF and power consumption of the DA [48].

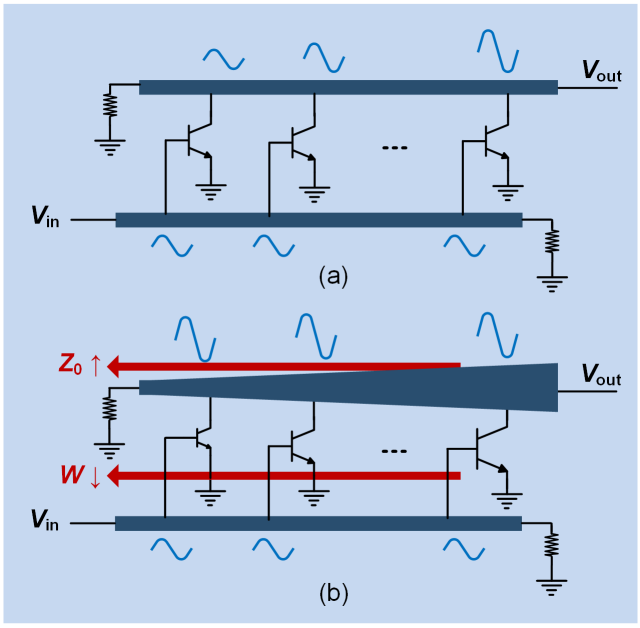

Fig. 14. Large-signal operation of (a) conventional DA and (b) nonuniform DA with scaled width of transistors and collector line.

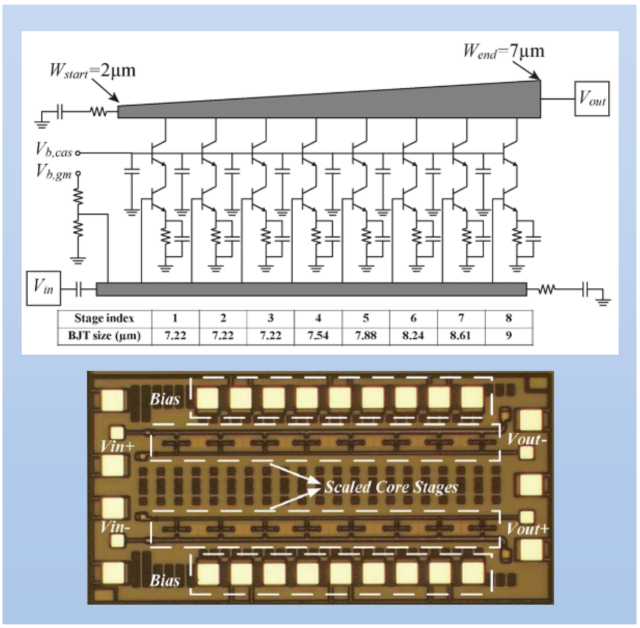

Fig. 15. The stage-scaled distributed power amplifier implemented in a 0.13-μm SiGe BiCMOS technology [28].

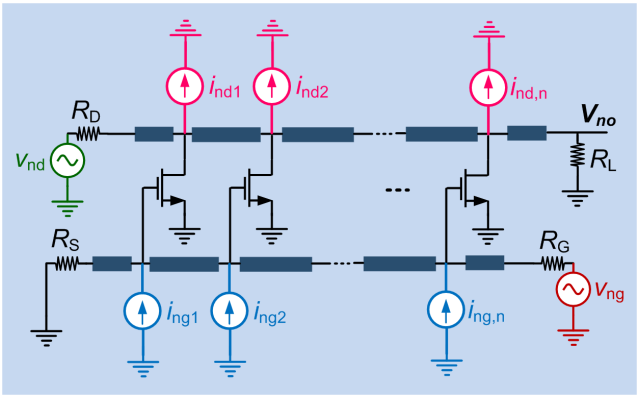

Fig. 16. Main noise sources in the DA, including termination resistances of the gate and drain lines as well as input and output noise current sources of the transistors.

efficiency of the power amplifier. A solution is to scale up the impedance of the drain line from the last stage toward the first stage, while bias and width of transistors are scaled down in the same direction [Fig.14(b)]. A DA is fabricated in a 0.13-μm SiGe (Silicon Germanium) BiCMOS process using this technique. An RC emitter degeneration technique is adopted to compensate base resistance of the transistors (Fig.15). The DA achieves 10 dB small-signal gain, 110 GHz bandwidth, mid-band saturated output power of 17.5 dBm and peak power-added efficiency (PAE) of 13.2%. Another technique for efficiency enhancement of the DA based on supply voltage scaling is proposed in [29]. Instead of tapering the transmission lines, the supply voltage of the transistors can be scaled from the last stage toward the first stage to improve power efficiency of the DA. An eight-stage DA with four supply voltages of 2.7, 3.2, 3.6, and 4 V is fabricated using a 90-nm SiGe BiCMOS technology. The DA achieves a gain of 12 dB over a 3-dB bandwidth of 14–105 GHz, the peak output power of 17 dBm, and the peak PAE of 12.6%. Other design techniques for nonuniform distributed power amplifiers are presented in [55] and [60].

F. Low-Noise DAs

The DA can be designed as a broadband low-noise amplifier. The main noise sources in a DA are shown in Fig. 16. A comprehensive noise analysis developed by Aitchison in 1985 [19] indicates that noise factor of the DA is given by

$$F = 1 + F_{R_G} + F_{R_D} + F_{i_{nd}} + F_{i_{ng}} \tag{7}$$

where F_{R_G} and F_{R_D} denote contributions of the gate and drain termination resistances, while $F_{i_{nd}}$ and $F_{i_{ng}}$ denote contributions of the transistors drain and gate current thermal noise sources in the DA noise factor. Analytical expressions for these noise factor terms are presented in [19]. In Fig. 17, the four terms of the noise factor defined in (7) are plotted in terms of normalized frequency (ω/ω_c). The DA is composed of 8 gain stages, with transconductance of 80 mS and cut-off frequency of f_T =130 GHz. The power density of the drain and gate current thermal noise sources are defined as $\overline{i_{nd}^2} = 4kT\gamma g_m$ and $\overline{i_{ng}^2} = 4kT\delta\omega^2 C_{gs}^2/g_m$, with $\gamma = 2/3$

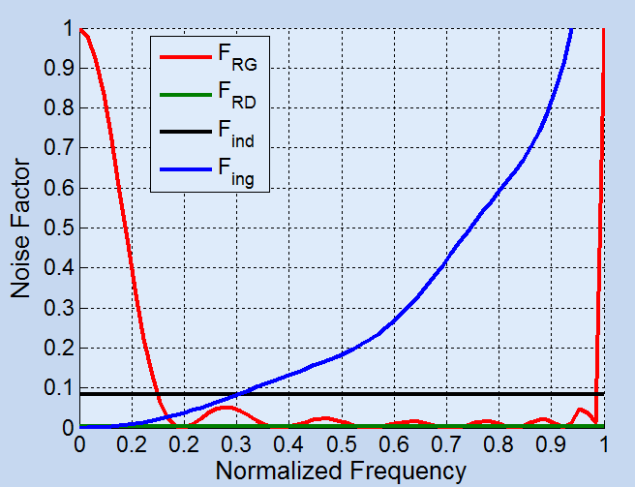

Fig. 17. The four terms of DA noise factor. Low-frequency noise factor is dominated by noise of the gate termination resistance, while high-frequency noise factor is mainly determined by the gate current noise of transistors.

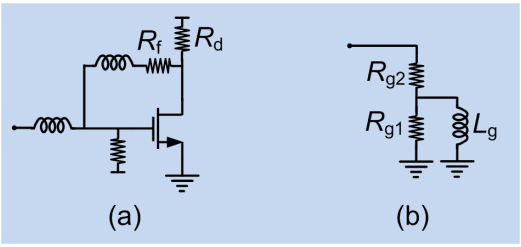

Fig. 18. Modified termination of the gate line using (a) active network, (b) passive network.

and $\delta = 4/15$, which are the values derived for long-channel devices [20]. The transmission lines have a characteristic impedance of 50 Ω and cut-off frequency of $f_c = 65$ GHz. The noise factor is dominated by noise of the gate termination resistance at low frequencies, while at high frequencies is mainly determined by the gate current noise of transistors.

Some techniques have been proposed to improve noise performance of the DA [34], [61]-[65]. As previously mentioned, the NF of the DA at low frequencies is limited by the noise contribution of the gate resistance. The gate termination resistor can be replaced by an active circuit as shown in Fig. 18(a), providing a 50-Ω impedance while contributing less thermal noise [61], [62]. The parasitic gate-source capacitance of the transistor can limit bandwidth of this circuit. Extra inductors are added to compensate the parasitic capacitance effect and improve matching at high frequencies. A passive network shown in Fig. 18(b) can also replace the gate termination resistor [34]. The network exhibits the resistance R_{g1} at low frequencies, which is smaller than Z_{0g}, to lower NF at these frequencies, while its impedance increases to $R_{g1}+R_{g2}$ at high frequencies to maintain impedance matching. The improved NF at low frequencies is obtained at the cost of degraded input impedance matching.

In the DA architecture proposed in [63], the gate termination resistor is eliminated and the last gain stage is modified as a wideband matched feedback amplifier (Fig. 19). It is

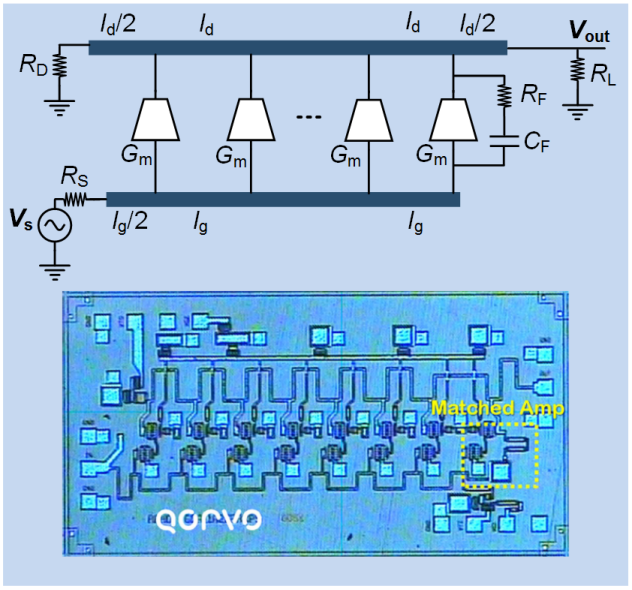

Fig. 19. The DA architecture with gate resistance termination replaced by a wideband matched feedback amplifier and chip photograph of the DA implemented in a 0.15-μm GaN HEMT technology [63].

shown that compared to the active gate termination previously presented, this DA architecture achieves superior linearity. The DA provides lower NF as a result of improved matching of transistors to their optimum noise impedance. A 0.1–45 GHz DA is designed using a 0.15-μm GaN HEMT technology. The DA provides over 10 dB gain, average mid-band NF of 2.5–3 dB, and saturated output power of 1 W.

A design technique for tapered distributed low-noise amplifiers is presented in [65]. The gate and drain lines are considered as a cascade of lumped-element T sections with their inductance and capacitance tapered by constant factors (Fig. 20). The gate and drain termination resistances are modified based on the tapering factors. The optimal tapering factors for inductances of the gate line K_g, inductances of the drain line K_d, and transconductances of the gain stages K_m can be determined based on gain, bandwidth, and NF contours. Using this technique, a low-noise tapered DA is designed and implemented in a 0.1-μm GaAs pHEMT process (Fig. 20). The chosen optimal design point is marked by an asterisk. The DA achieves average gain of 15.2 dB and 3-dB bandwidth of 43.3 GHz. The average NF is 2.3 dB over the frequency band 2–40 GHz.

IV. State-of-The-Art Processes

A. GaAs DAs

The first MMIC DA designed using a 1-μm GaAs MESFET process was reported in 1982 [4]. It achieved 9-dB gain over 1–13 GHz. Later in 1985, a GaAs DA with 2–40 GHz bandwidth and 4-dB gain was presented [66]. Since then, GaAs has been the dominant technology for implementation of commercial DAs. Several GaAs designs have been reported in the literature [26], [51], [62], [65], [67]-[72]. GaAs technology provides several advantages for DA implementation. It offers low-loss transmission lines and passive elements resulting

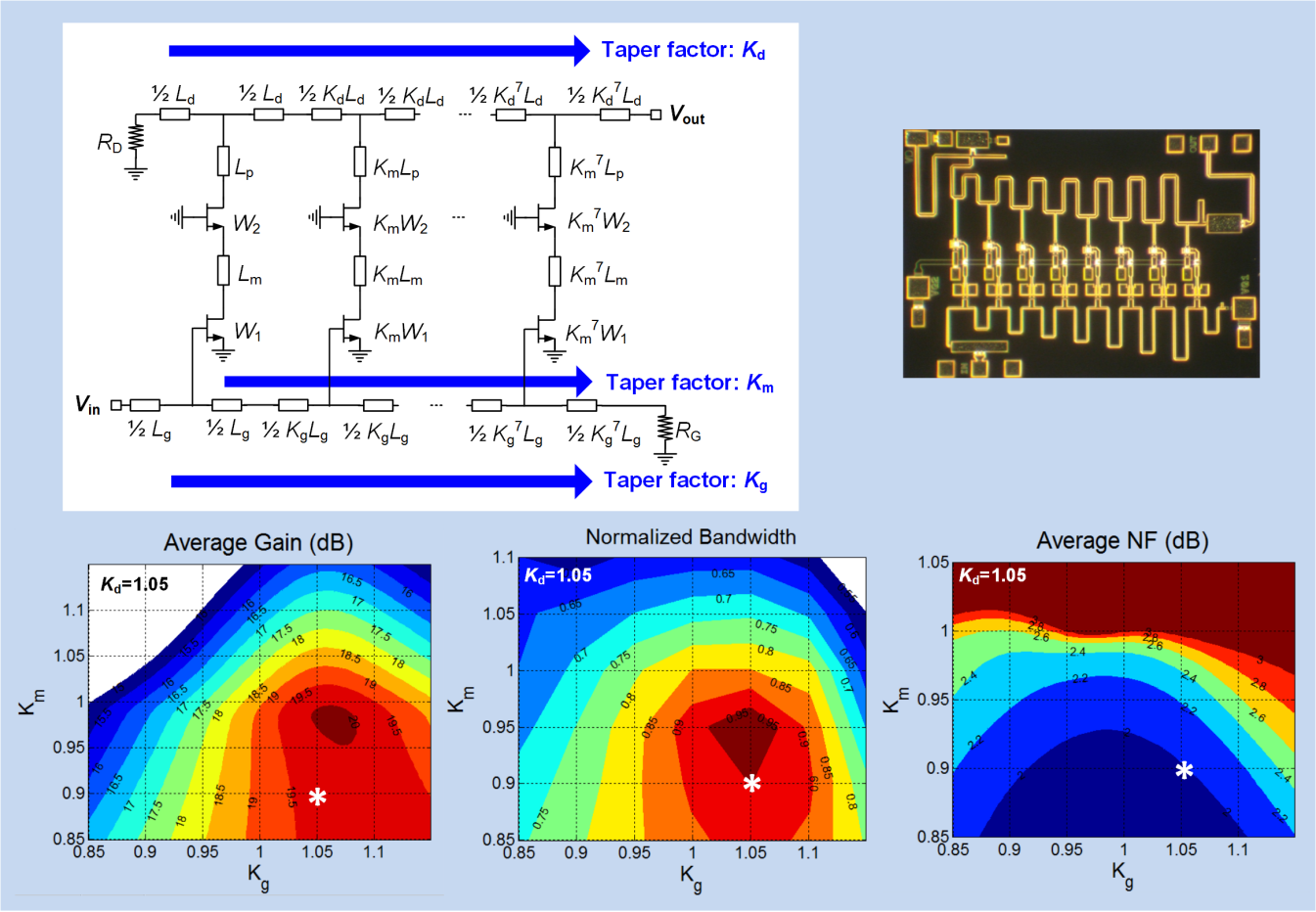

Fig. 20. The tapered distributed low-noise amplifier design technique using contours of gain, bandwidth, and NF. The chosen optimal design point is marked by an asterisk. A tapered low-noise DA with over 40-GHz bandwidth is implemented in a 0.1-μm GaAs pHEMT technology [65].

from semi-insulating GaAs substrate and thick metal layers. Moreover, accurate process design kits (PDKs) are available from GaAs foundries which are essential in design of high-frequency integrated DAs. A performance summary of state-of-the-art GaAs DAs is given in Table I. The minimum NF and maximum output 1-dB compression point (P_{1dB}) are reported in the table. The GaAs DAs provide low NF and good linearity, while their power consumption is relatively high. The maximum bandwidth of 65 GHz and GBW of 500 GHz are achieved using GaAs technologies.

B. InP DAs

The first demonstration of an InP-based MMIC DA was reported in 1990 [5]. An impressive bandwidth of 5–100 GHz with 5.5 dB average gain was achieved using a 0.1-μm InP HEMT process. InP has been a popular process in implementation of extremely wideband DAs [5], [27], [74]-[82]. A performance summary of state-of-the-art InP DAs is presented in Table II. The table indicates bandwidths over 100 GHz can be readily achieved using InP technologies.

In [77], an amplifier with 45-GHz bandwidth and 30-dB gain is reported using an InP double heterojunction bipolar transistor (DHBT) technology. InP DHBTs offer higher bandwidth compared to a transistor with the same feature size in Si and SiGe technologies.The amplifier comprises a lumped input stage followed by a distributed output stage (Fig. 21). The input stage consists of a differential current-mode logic (CML) inverter preceded by two cascaded emitter followers to reduce input parasitic capacitance. The output distributed stage consists of six differential amplifier cells and employs coplanar wave-guide (CPW) transmission lines. The gain cells, shown in Fig. 21, use multiple bandwidth enhancement techniques including use of a double emitter follower, emitter RL degeneration in the cascode stage, series inductive peaking at the inter-stage of common-emitter and common-base devices, as well as shunt inductive peaking at the output of the cascode stage. The design approach can be considered a solution to mitigate the low gain issue of conventional DAs.

In [82], DAs with record bandwidth are reported using an InP DHBT technology (Fig. 22). A cascode amplifier with inter-stage and output bandwidth enhancement is used as the gain cell. The single-stage DA achieves 7.5-dB gain and 192-GHz bandwidth, while consuming 40 mW DC power. The two-cascaded single-stage DA achieves an average gain of 16 dB with a bandwidth of 235 GHz and thus a GBW of 1480 GHz. The chip DC power consumption is 117 mW.

TABLE I
PERFORMANCE SUMMARY OF STATE-OF-THE-ART GAAS DAS.

Ref.	BW (GHz)	Gain (dB)	GBW (GHz)	NF (dB)	P_{1dB} (dBm)	P_{dc} (mW)	Technology
[26]	27.5	12.7	119	4.0	–	650	HBT
[51]	37.5	19.2	342	2.3	12.6	131	0.1-μm pHEMT
[62]	44	9	124	5.4	–	1000	0.2-μm MESFET
[65]	43.3	15.2	249	2.0	9.5	110	0.1-μm pHEMT
[67]	65	13.4	304	2.0	11.0	105	0.15-μm mHEMT
[68]	39.9	22	503	–	10	484	0.15-μm pHEMT
[69]	54	15	304	–	20	1100	0.15-μm pHEMT
[70]	50	12.5	211	2.5	–	400	0.1-μm mHEMT
[71]	34.5	20.1	349	–	25.1	1300	0.15-μm pHEMT
[71]	41	13.2	187	–	24.6	1860	0.15-μm pHEMT
[72]	43.5	8.5	116	4.2	8	225	0.5/0.2-μm HEMT/HBT

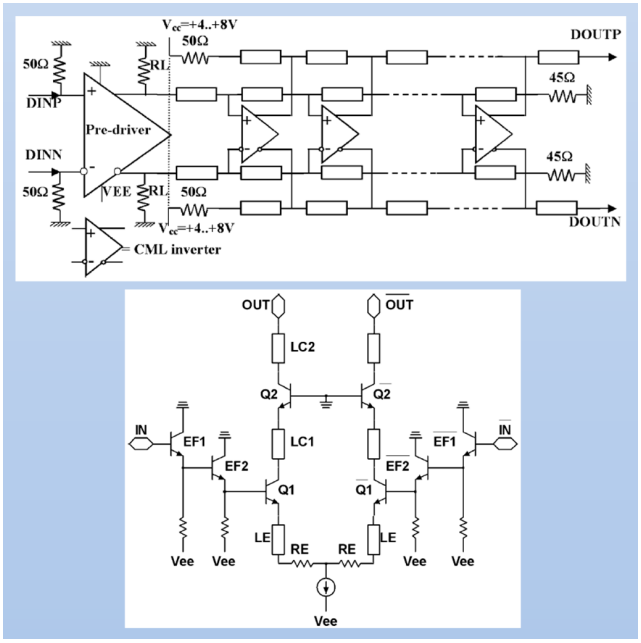

Fig. 21. The broadband amplifier architecture comprising a lumped driver amplifier followed by a distributed output stage, providing 30-dB gain and 45-GHz bandwidth in an InP DHBT technology [77].

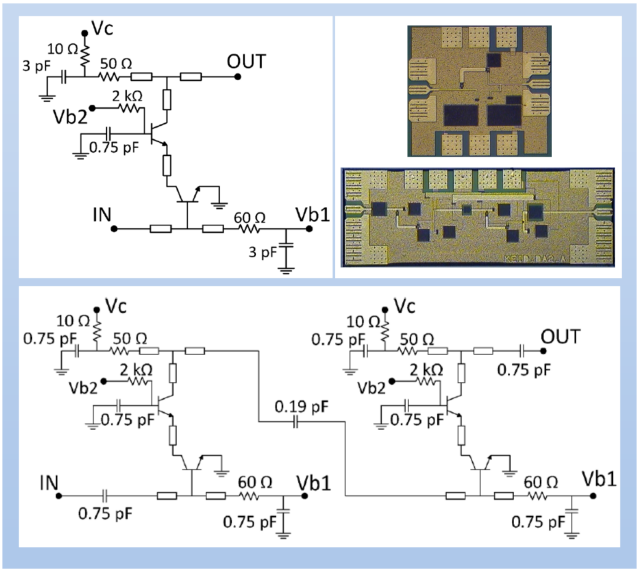

Fig. 22. The single-stage DA with 192-GHz bandwidth and the two-cascaded single-stage DA featuring 235-GHz bandwidth [82]. These InP DHBT DAs achieve widest bandwidths reported in any technology.

C. CMOS DAs

In recent years, CMOS has been the most attractive technology to implement high-frequency integrated circuits because of its low cost, low power consumption, and potential for integration with baseband circuits. The first CMOS DA reported in 1999 [6] was implemented in a 0.18-μm process. Gain was 5 dB at low frequencies and bandwidth was quite limited. DAs have since been reported in more advanced CMOS technologies, achieving superior performance. The main challenge in implementation of CMOS DAs is the high loss of transmission lines arising from lossy Si substrate and thin metal layers. This results in lower gain and higher NF compared to GaAs DAs. Also, lower breakdown voltage of CMOS transistors limits output power and linearity of the DA. The main advantages of CMOS DAs are lower power consumption and wider bandwidth resulting from high-speed transistors in advanced nano-scale CMOS technologies. A summary of state-of-the-art CMOS DAs is presented in Table III. A bandwidth of 80 GHz using a 90-nm CMOS process [83] and a bandwidth of 92 GHz using a 45-nm silicon-on-insulator (SOI) CMOS process [92] are achieved. The SOI CMOS technologies can offer lower NF arising from lower loss of the insulator substrate. In [90], a DA with average gain of 9.7 dB over 10–59 GHz is designed using a 90-nm SOI CMOS process. The DA exhibits an impressive noise performance, achieving NF below 3.8 dB from 0.1 to 40 GHz. In [86], a low-power design approach for the DA is presented, leading to a 0.18-μm CMOS DA with 7-GHz bandwidth and 8-dB gain, consuming only 9 mW DC power.

In [58], a cascaded three-stage DA with 14-dB gain and

TABLE II
PERFORMANCE SUMMARY OF STATE-OF-THE-ART INP DAS.

Ref.	BW (GHz)	Gain (dB)	GBW (GHz)	P_{dc} (mW)	Technology
[5]	95	5.5	179	–	0.1-μm HEMT
[27]	102	10	323	150	DHBT
[27]	94	12	374	460	DHBT
[27]	80	11	28	224	DHBT
[74]	111	7	248	–	0.1-μm HEMT
[74]	156	5	277	–	0.1-μm HEMT
[74]	180	5	320	–	0.1-μm HEMT
[75]	89.2	10	282	860	0.1-μm HEMT
[76]	92	13	411	800	0.1-μm HEMT
[77]	50	25	889	1700	1.2-μm DHBT
[77]	45	30	1423	3000	1.2-μm DHBT
[77]	60	17	425	2500	1.2-μm DHBT
[78]	120	21	1346	610	0.7-μm DHBT
[79]	70	12.8	306	105	TS HBT
[80]	90	15	506	–	0.7-μm DHBT
[80]	110	13	491	–	0.7-μm DHBT
[81]	182	10	576	105	0.25-μm HBT
[82]	192	7.5	455	40	0.25-μm DHBT
[82]	235	16	1483	117	0.25-μm DHBT
[82]	180	12.8	786	110	0.25-μm DHBT

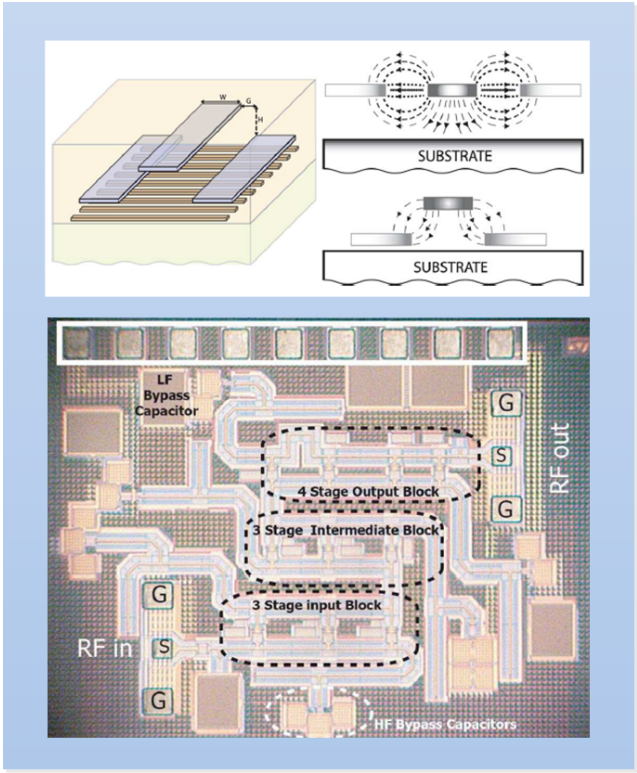

Fig. 23. The cascaded three-stage DA using elevated CPW lines to provide higher impedance and lower loss. The DA is implemented in a 90-nm CMOS technology [58].

73.5-GHz bandwidth is designed using a 90-nm CMOS process (Fig. 23). An elevated CPW (E-CPW) transmission line structure is used to increase characteristic impedance and lower loss of the lines. The length of the gate and drain line segments are tapered to improve gain and bandwidth of the DA.

D. SiGe BiCMOS DAs

The DAs implemented in SiGe BiCMOS technologies can provide much higher bandwidth compared to CMOS processes. The SiGe technologies offer transistors with higher cut-off frequency and low-loss transmission lines and passive elements. In Table IV, performance of state-of-the-art SiGe BiCMOS DAs is summarized. It is noticed DAs with bandwidth exceeding 100 GHz and GBW of 1500 GHz are reported. The achieved bandwidth values are comparable with that obtained using InP technologies, while DC power consumption is lower.

In [31], a DA with 170-GHz bandwidth and 10-dB gain is presented using a 130-nm SiGe BiCMOS technology. The frequency behavior of gain stage transconductance G_m is shaped to compensate for loss of the input line at high frequencies. The schematic of the gain cell is shown in Fig. 24, where a triple cascode amplifier is used to provide high isolation between input and output. Emitter RC degeneration is used to compensate for loss of the input line, while capacitive coupling is used to reduce parasitic capacitance loading on the input line. The boosting of G_m at high frequencies is achieved by resonance of the two inter-stage inductances with inter-stage parasitic capacitances. This leads to a peak in G_m at high frequencies that is used to compensate for the increase in loss

TABLE III
PERFORMANCE SUMMARY OF STATE-OF-THE-ART CMOS DAS.

Ref.	BW (GHz)	Gain (dB)	GBW (GHz)	NF (dB)	P_{1dB} (dBm)	P_{dc} (mW)	Technology
[33]	43.9	9.8	136	–	–	103	130 nm
[36]	33.4	16.2	216	–	–	260	180 nm
[36]	39.4	20	394	–	–	250	180 nm
[39]	65	22	818	6.9	10	97	65 nm
[45]	74	19	660	5.2	3.7	84	90 nm
[48]	12	15	67	2.3	8	26	130 nm
[52]	61.3	7	137	–	–	60	90 nm
[58]	73.5	14	368	–	3.2	84	90 nm
[83]	80	7.4	188	–	8	120	90 nm
[84]	70	7	157	–	10	122	90 nm
[85]	44	19	392	–	–	57	90 nm
[86]	7	8	18	4.2	–	9	180 nm
[87]	33	24	523	6.5	7.5	238	180 nm
[88]	30	7	67	4	2	34	40 nm
[89]	87	5	155	–	–	90	120 nm SOI
[89]	81	9	228	5.5	10	130	120 nm SOI
[90]	59	8	148	3.2	12.5	132	90 nm SOI
[92]	92	9	259	–	–	73.5	45 nm SOI

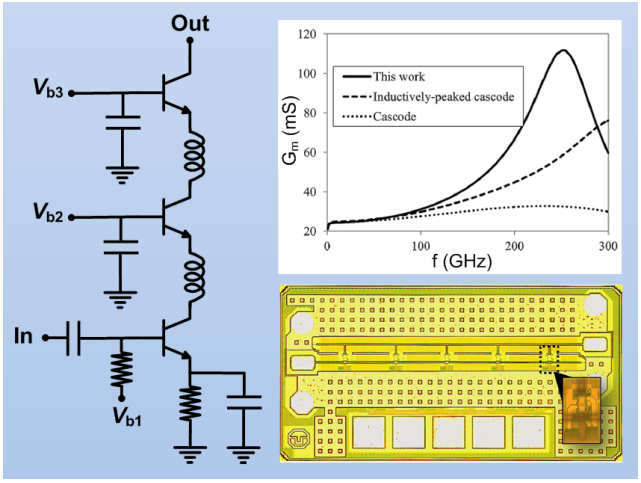

Fig. 24. The triple cascode amplifier architecture used as the gain stage in a 170-GHz bandwidth DA implemented using a 0.13-μm SiGe BiCMOS technology [31].

TABLE IV
PERFORMANCE SUMMARY OF STATE-OF-THE-ART SIGE BICMOS DAS.

Ref.	BW (GHz)	Gain (dB)	GBW (GHz)	P_{dc} (mW)	Technology
[28]	110	10	348	119	130 nm
[29]	91	12	362	297	90 nm
[30]	95	24	1506	247.5	130 nm
[31]	170	10	538	108	130 nm
[35]	29.4	13.2	134	136	130 nm
[55]	11	12	44	400	250 nm
[93]	13	26	259	82	120 nm
[94]	170	13	759	74	130 nm
[95]	180	18.7	1550	86	130 nm
[96]	135	8.5	360	99	55 nm

of the lines, and thus, extend the bandwidth of the DA.

E. GaN DAs

The high power capability of GaN technology has made it an attractive solution for power amplifier design. A relatively small GaN transistor can provide an output power level that is not feasible using other high-power processes, making it a good candidate for implementation of wideband DAs with high output power. A performance summary of state-of-the-art GaN DAs is presented in Table V. The GaN DAs are primarily targeted to provide high output power and efficiency. Output power and PAE approaching 20 W and 35% can be achieved using GaN DAs.

In [22], a distributed power amplifier comprising ten stages is implemented using a 0.25-μm GaN on SiC HEMT technology with 30 V supply voltage (Fig. 25). The DA adopts tapered width of the drain line sections to improve output power and also uses the input capacitive coupling technique to reduce input parasitic capacitance of the transistors. The amplifier achieves 10 dB small-signal gain, 9–15 W saturated output power, and 20–38% PAE over 1.5–17 GHz bandwidth.

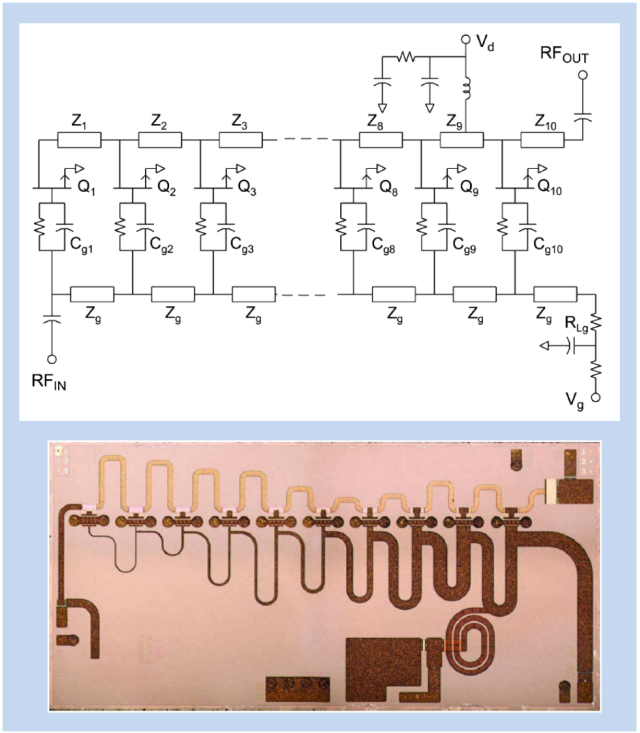

Fig. 25. The nonuniform distributed power amplifier with 9–15 W output power implemented using a 0.25-μm GaN HEMT technology [22].

In [23], a two-stage distributed power amplifier is designed using a 0.2-μm dual-gate GaN HEMT technology (Fig. 26). A low inter-stage impedance of 25 Ω is chosen for two reasons: The lower impedance leads to larger width of the transistors in the output stage, increasing output power without reducing bandwidth. The lower impedance also keeps the inter-stage transmission lines short, saving chip area. A capacitive division technique is used in the second stage to further enhance the output power. The DA achieves small-signal gain of 20 dB over 2–18 GHz, saturated output power of 0.8–2 W, and PAE of 5–15%.

In [54], a balanced power amplifier using two DAs with tapered width of the drain line and scaled size of transistors is implemented in a 0.25-μm GaN process with 40 V supply voltage (Fig. 27). The balanced amplifier exhibits small-signal gain of 8–10 dB, average output power of 12.9 W, and average PAE of 18% over 6–18 GHz. The maximum measured output power is 13.5 W.

V. CONCLUSION AND FUTURE TRENDS

Bandwidth and gain are usually used as the main performance metrics for DAs. The performance trends of DAs designed using various technologies are illustrated in Figs. 28 and 29. Fig. 28 indicates that bandwidths over 100 GHz have been achieved by using InP and SiGe processes. GBWs over 500 GHz can also be obtained by using these two processes with a few others in CMOS. Fig. 29 indicates that before the year 2000, DAs had been mainly implemented in GaAs and InP technologies. CMOS, SiGe and GaN technologies

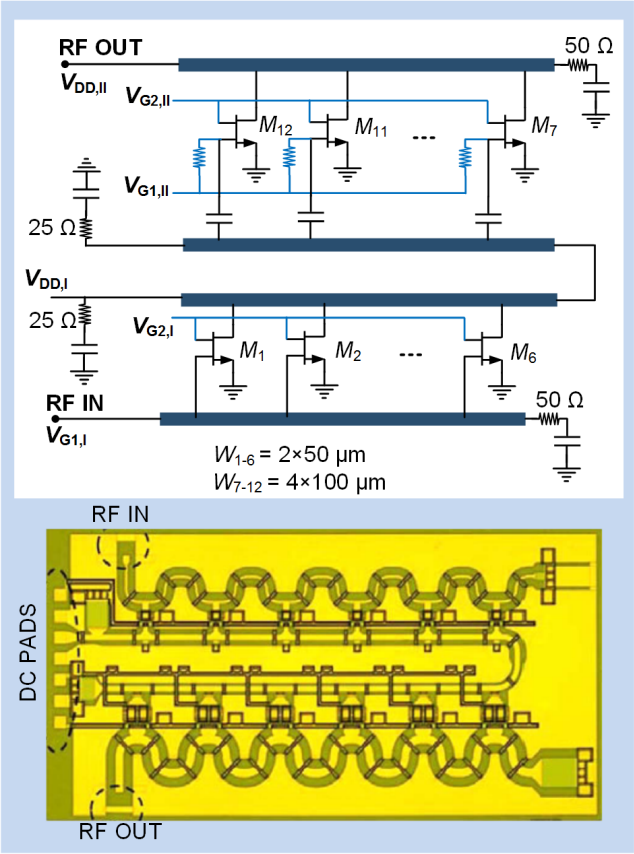

Fig. 26. The two-stage distributed power amplifier implemented using a 0.2-μm dual-gate GaN HEMT technology [23].

TABLE V
PERFORMANCE SUMMARY OF STATE-OF-THE-ART GAN HEMT DAS.

Ref.	BW (GHz)	Gain (dB)	GBW (GHz)	P_{sat} (W)	PAE (%)	Technology
[22]	15.5	10	49	9–15	20–38	0.25 μm
[23]	16	20	160	0.8–2	5–15	0.2 μm
[24]	34	14	170	0.5	5	0.1 μm
[53]	13	11.5	49	5.5	25	0.25 μm
[54]	12	10.4	40	12.9	18	0.25 μm
[63]	44.9	10	142	1–2	–	0.15 μm
[73]	14	10	44	4.4	16	0.2 μm
[97]	49	5.2	89	–	–	0.2 μm
[97]	30	12	119	1	16	0.2 μm
[98]	18	12	72	10–20.6	25–36	0.2 μm
[99]	16	12	64	11–16	25–38	0.25 μm
[100]	25	15	140	2.5	12	0.14 μm

have become popular in recent years for designing DAs. In particular, CMOS technologies with continuous gate-length scaling have offered high-speed transistors with cut-off frequencies approaching several hundreds of gigahertz. SiGe has also proven itself as a promising solution to achieve bandwidths comparable and even larger than what in the past was only feasible using InP. In the future, it is expected

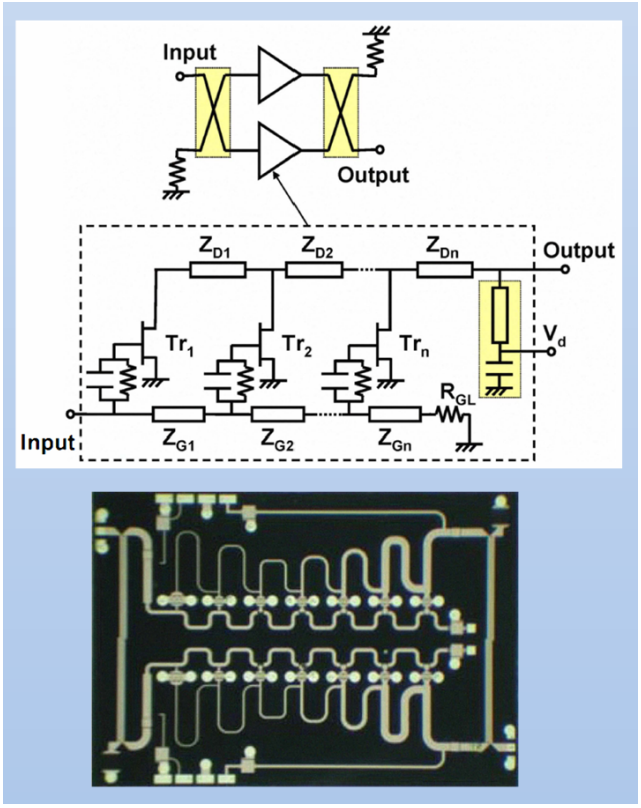

Fig. 27. The balanced distributed power amplifier with 12.9 W average output power implemented using a 0.25-μm GaN technology [54].

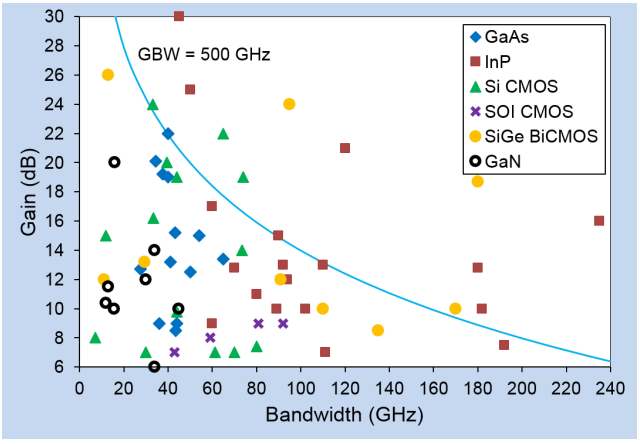

Fig. 28. Gain and bandwidth performance of integrated DAs in various technologies.

that further wider bandwidths can be achieved, specifically by using CMOS and SiGe technologies. GaN is also experiencing rapid advancements, paving the way for realization of high-power broadband DAs. These advancements will open up new opportunities for future broadband communication systems.

VI. ACKNOWLEDGMENT

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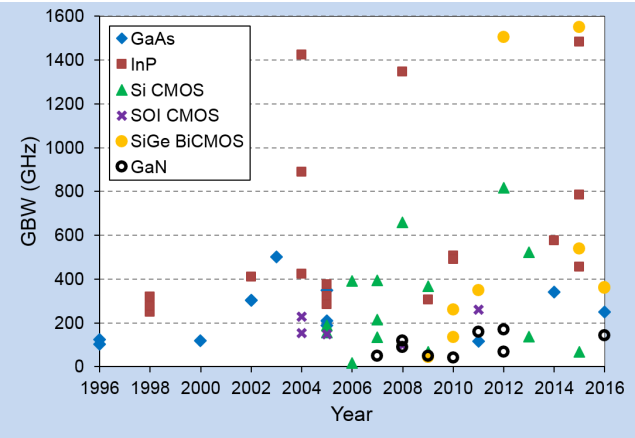

Fig. 29. Gain-Bandwidth performance trend of DAs in the past decades.

13/RC/2077 and 12/IA/1267.

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