A 28-GHz Switched-Filter Phase Shifter with Fine Phase-Tuning Capability Using Back-Gate Biasing in 22-nm FD-SOI CMOS

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***Abstract*— This paper introduces a phase shifter based on switched filters for mm-wave 5G MIMO transmitters. It is realized in 22 nm FD-SOI CMOS and exploits the use of back-gate biasing. The new approach features strong tolerance to process, voltage and temperature (PVT) variations and thus can maintain low phase error with fine phase tuning capability supporting a large bandwidth. Measurement results show that the 4-bit phase shifter achieves 3.5° rms phase error at 28 GHz. The proposed phase shifter can maintain <5° of the worst-case rms phase error when operating across 24 to 29.5 GHz resulting in 20.56% fractional bandwidth which is the largest among the published switched-filter phase shifters to date.**

***Keywords*— 5G, CMOS, MIMO, millimeter wave, phase shifters, phased arrays, silicon-on-insulator (SOI).**

I. Introduction

Recent developments in 5G wireless aim to support increasing demand for ever higher data rate by exploiting the large available bandwidth in mm-wave phased array systems. As one of the key components in such systems, phase shifters are responsible for electronic beam steering. There are many types of phase shifters, mainly categorized as active and passive. The active ones use vector-modulator based structures [1], [2], whereas the passive ones utilize reflective loads [3]–[5], switched-line [6], [7] or switched-filter structures [8]–[11]. The passive phase shifters typically require a stage for each bit, which means a larger area and higher signal loss, while the active phase shifters require additional dc power which in turn worsens the power efficiency of the overall system. Despite their different natures, both active and passive phase shifters share a common concern of maintaining their performance across the wide mm-wave frequency range to support 5G systems in order to maintain the quality of the generated beams. Additionally, important key parameters, such as phase error, can be further deteriorated in face of process, voltage and temperature (PVT) variations. Therefore, it is important to have a fine phase-tuning adjustment capability which will allow the possibility to maintain the performance of the wideband phase shifting over PVT variations.

From a circuit perspective, the insertion loss and phase shift of a signal passing through a transistor switch can be controlled by means of the transistor's channel resistance, $R_{\rm on}$. This hints at a new solution for reducing the effects of PVT variations: to use a back-gate for adjusting $R_{\rm on}$, provided it is available in the used technology. The fully depleted silicon-on-insulator (FD-SOI) process is one of the available CMOS technologies that offer an individual and dynamic control of the threshold voltage, V_{th}, of each transistor through body biasing applied on a back-gate terminal, and without channel doping. The idea of controlling the insertion loss and phase shift through the back-gate voltage for the purpose of adjusting $R_{\rm on}$ is illustrated in Fig. 1 for a representative NMOS transistor switch.

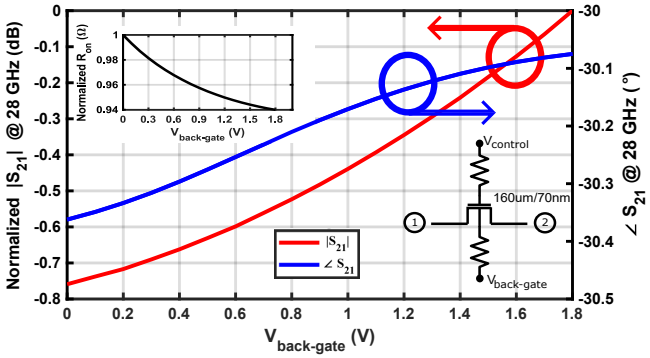
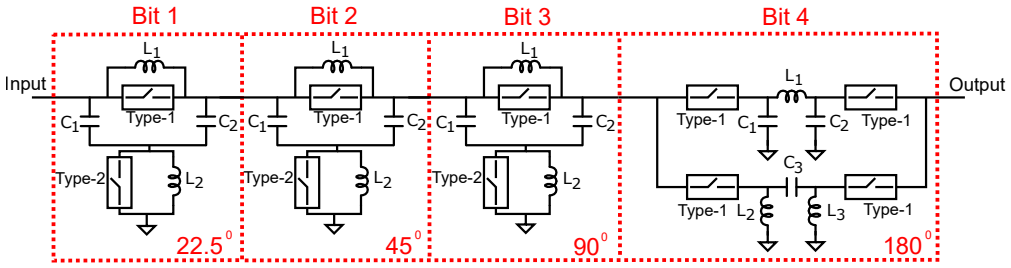


Fig. 1. Simulated effect of the back-gate voltage on S_{21} of the transistor switch.

In this paper, we show how the individual $R_{\rm on}$ control can be used for calibrating the effects of PVT variations and achieving large bandwidth in a 4-bit switched-filter phase shifter. The main advantage of the proposed structure is that the phase error, which is affected by PVT variations, can be maintained low within a large frequency range. Measurement results confirm the largest bandwidth achieved among published switched-filter phase shifters. Furthermore, this is the first published design that uses body biasing via a back-gate terminal for fine phase tuning.

II. Proposed Switched-Filter Phase Shifter

Fig. 2 presents the overall schematic of the proposed phase shifter. The first three bits of the 4-bit phase shifter include only one low-pass filter, similar to the bit configurations presented in [8]–[10]. They are different from the typical switched-filter designs, which are usually composed of cascaded units that include two branches with low-pass or high-pass filters selected by a single bit by means of single-pole-double-throw (SPDT) switches. The reason behind this modification is to attain a smaller chip area by reducing the number of inductors. Moreover, thanks to this topology, the SPDT switch can be eliminated, which in turn further reduces the chip area and signal loss. For the customary MSB bit, which is responsible for the 180° phase shift, the modified



	Bit 1	Bit 2	Bit 3	Bit 4
C_1	7.48 fF	21.1 fF	57.7 fF	178.92 fF
L_1	155.2 pH	199.62 pH	193.29 pH	241.43 pH
C_2	7.48 fF	21.1 fF	57.7 fF	178.92 fF
L_2	1.54 nH	412.26 pH	180.57 pH	577.9 pH
C_3	——	——	——	1.45 pF
L_3	——	——	——	577.9 pH

Fig. 2. Overall schematic of the implemented 4-bit switched-filter phase shifter.

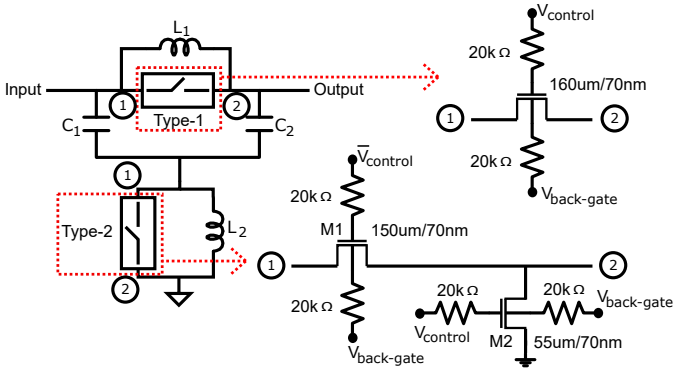


Fig. 3. Schematic representation of the first three bits.

version cannot be used since it is impossible to obtain the required capacitance and inductor values with the technology used. The conventional design is used instead.

The main difference between the proposed phase shifter and the ones presented in [8]–[10] is in the switch design: here, the switches have an extra control pin through the back-gate terminal which enables the R_{on} control by body biasing.

A. Switch Design

Fig. 3 illustrates the schematic view of the first three bits. For the switch located in the series branch, which is labelled as "type-1", R_{on} and C_{off} values should be very small. On the other hand, for the switch located in the parallel branch, which is labelled as "type-2", R_{on} value should also be small while C_{off} value should be very large in order to have a smaller inductor at the parallel branch. To optimise the performance of a single bit, two different types of switches are implemented. For the "type-1" switches, a single transistor switch is employed. This switch is also used for all the switches in the 180° bit. For the "type-2" switches, a one-stage series-shunt switch, also known as a ladder-type switch, is implemented. One of the most important features of this topology is that large C_{off} can be obtained with small R_{on}. The common feature of these switches is that they have an additional control pin which enables the individual body biasing via the back-gate terminal for all the transistors, and also enables the individual R_{on} control. This feature can be used for introducing the fine phase-tuning capability to the phase shifter design.

B. Phase Shifter Design Procedure

For the case of $V_{\text{back-gate}} = 0\,\text{V}$, $V_{\text{control}} = 1.2\,\text{V}$ and $\overline{V}_{\text{control}} = 0\,\text{V}$, the equivalent circuit models of the switches shown in Fig. 3 are investigated. The initial values of the inductors and capacitors are obtained separately for each bit by using the previously discussed bit configurations and the circuit models of the switches in Keysight ADS. Then, these values are used as a reference point for the optimization toolbox of Cadence and the final values are calculated with this toolbox.

To estimate the PVT variation effect on the phase shifting performance, additional simulations are performed. The maximum expected phase variations for each state are obtained by a local process-variation Monte Carlo simulation, temperature sweep from 0°C to 50°C, and 10% voltage variation. Based on these simulations, the maximum expected phase variation due to PVT variation is approximately 1.3°.

III. Measurement Results

The proposed phase shifter was fabricated in GlobalFoundries 22 nm FD-SOI process. The chip micrograph is shown in Fig. 4. For the measurement results presented in this paper, S-parameters were measured with Cascade Microtech Summit 9000 Analytical Probe Station and MPI T40A GSG-100 wafer probes connected to Agilent E8361A PNA directly. On-wafer calibration was done with AC-2 calibration substrate. The measurements were performed with the back-gate voltage changing from 0 V to 1.8 V in steps of 0.1 V.

Fig. 5 shows the RF measurement results in terms of phase shift and insertion loss vs. frequency. Fig. 6 illustrates the

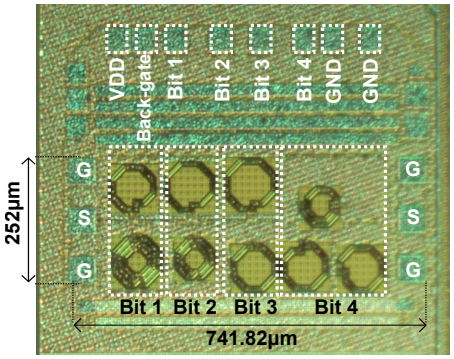
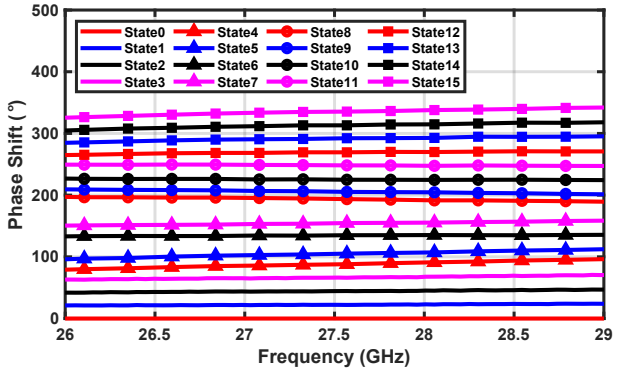
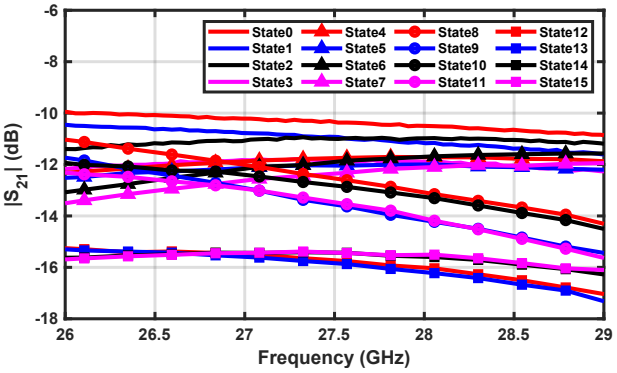


Fig. 4. Chip micrograph of the fabricated 4-bit switched-filter phase shifter.

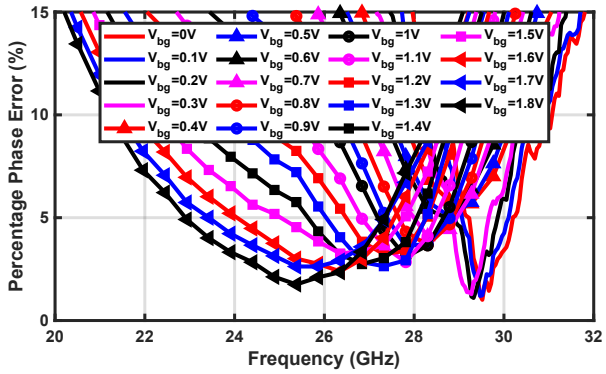


(a)

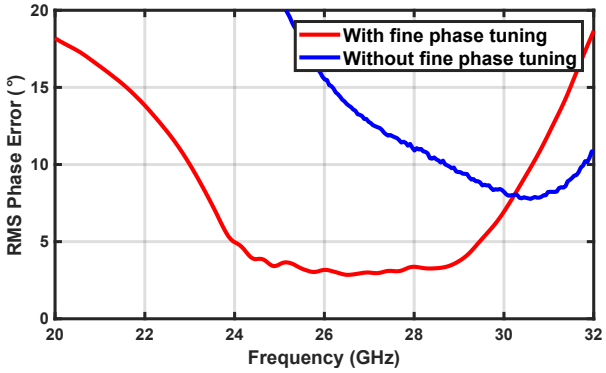


(b)

Fig. 5. Measured (a) phase shift and (b) insertion loss of the phase shifter with proper back-gate biasing for attaining low rms phase error at 28 GHz.



(a)



(b)

Fig. 7. Measured phase error vs. frequency: (a) percentage phase error in State 1 example across different back-gate voltages, and (b) rms phase error across all the 16 states with/without the fine phase tuning.

percentage phase error at 28 GHz for each state with and without the fine phase-tuning, which proves the effectiveness of the technique. For these measurement results, the back-gate voltages were set for attaining the lowest rms phase error at 28 GHz. At 28 GHz, the measured rms phase error is 3.5° with an insertion loss of 13.5 ±2.5 dB, including the GSG pads, and a return loss lower than 7 dB. As it can be seen in Fig. 6, State 8 has the maximum percentage phase error which increases the overall rms phase error. Nevertheless, the designed phase shifter offers percentage phase error lower than 15% for all states between 26 GHz and 29 GHz. It should be noted that the back-gate voltage applied to each state is not expected to be the same. Each state may attain its lowest phase error and insertion loss at a different calibration point.

Fig. 7(a) shows the measured percentage phase error of

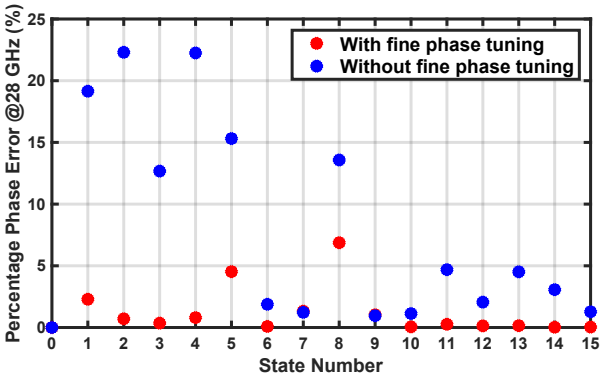


Fig. 6. Measured percentage phase error at 28 GHz across all states of the 4-bit phase shifter.

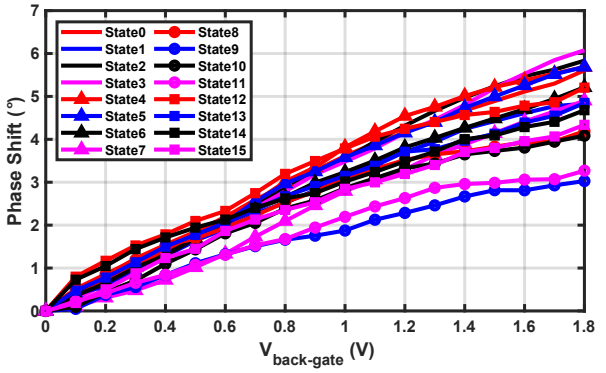


Fig. 8. Additional phase shift achieved with increasing back-gate voltage in all states.

TABLE I. PERFORMANCE COMPARISON OF THE FABRICATED PHASE SHIFTER WITH THE STATE-OF-THE-ART IN PASSIVE PHASE SHIFTERS.

	This Work	**[5] TCAS-I '20**	**[8] TMTT '18**	**[9] RFIC '16**	**[10] MWCL '16**	**[11] IMS '16**
Technology	22-nm FD-SOI CMOS	65-nm CMOS	40-nm (1P7M)	45-nm FD-SOI CMOS	65-nm CMOS	90-nm CMOS
Frequency Range (GHz)	24-29.5	28	22-36	26-28	27.5-28.35	57-66
Frac. Bandwidth (%) (rms phase error <5°)	20.56	Not available	13.8*	14.81	6.78*	14.63
Topology	Switched-filter	Reflective type	Switched-filter	Switched-filter	Switched-filter	Switched-filter
Phase Shift Range (°)	360	180	360	360	360	360
Number of Bits	4	5	3	5	4	4
RMS Phase Error (°)	< 5	2.8	< 12.8	< 5	< 8.98	< 5
Phase Tune Range (°)	≥ 3	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
Loss (dB)	13.5±2.5	16.5±1.5	5.6±0.5	7±1	6.6±1	17±0.5
Active Area (mm^2)	0.15	0.17	0.132	3.3 (All receiver)	0.23	0.168

* Estimated from plot.

State 1 at different back-gate voltages. It implies that each of the back-gate voltages applied to the design results in a different bandwidth around a different center frequency. That means one can divide the frequency band into the sub-ranges and apply the back-gate voltages to them accordingly. When these ranges are cascaded, the bandwidth of State 1 will become larger. This is also valid for other states. Therefore, by applying different back-gate voltages to each of sub-ranges in the frequency band can lead to a larger bandwidth. As Fig. 7(b) implies, the presented phase shifter can maintain the rms phase error <5° between 24 and 29.5 GHz with the fine phase-tuning.

Fig. 8 presents the effect of the back-gate voltage on the phase shift for all states. As discussed above, the phase shift due to the local process variation as well as 10% variations in both voltage and temperature is expected to be at a maximum of 1.3°. Fig. 8 points out that this design is robust to PVT variations since for for all states the minimum fine phase tuning range is at least 3° whereas the maximum expected phase shift due to PVT variations is 1.3°.

Table I summarizes the performance of the proposed phase shifter and compares it with the published state-of-the-art. The novelty of the proposed structure lies in the fine phase-tuning capability. This brings about several advantages. First, it can decrease the phase error as shown in Fig. 6. Second, it can extend the operational frequency range with supported low rms phase error. Ultimately, this structure can offer robustness to the PVT variations and their ill effects on the phase error.

IV. CONCLUSION

This paper presents a wideband mm-wave 4-bit switched-filter phase shifter which has the capability of fine phase-tuning by virtue of body biasing with the back-gate terminal. The technique allows to achieve low overall rms phase error without being effected by PVT variations in a large bandwidth. Some additional advantages are discussed and supported by measurements. This design is the first ever switched-filter phase shifter reported which has fine phase-tuning capability. Based on the measurement results, the rms phase error is lower than 5° between 24 and 29.5 GHz, which is the largest reported bandwidth in the literature for switched-filter phase shifters. The presented technique can be used with other phase shifter topologies and it could be considered for complex phase modulation.

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