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BJT Based Precision Voltage¹ Reference in FinFET Technology

Umanath Ramachandra Kamath



¹The Tempio Voltiano at Como dedicated to Alessandro Volta who invented battery, a constant voltage source (Image Source: wikipedia.org)

BJT Based Precision Voltage Reference in FinFET Technology

by

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Master of Science in Microelectronics

Delft University of Technology, The Netherlands, 2012

This thesis is submitted to University College Dublin
in fulfilment of the requirements for the degree of

Doctor of Philosophy

School of Electrical and Electronic Engineering



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To my Mother, who is the clearest vision of God to me and to whom I owe everything I am.

To my late Father, who inspired and encouraged me to dream big.

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Abstract

Real world is analog. Hence, precision analog circuits are an essential part of systems that interface with the outside world. Data converters are a clear example of this, among many others. Analog or mixed-signal circuits are based on voltage, current, or time-domain signal processing. In most of these cases, they require a stable reference generation, which is a bandgap voltage/current. In addition, power generation and management for analog or mixed-signal circuits, as well as digital circuits, requires a stable reference.

Typically, it is expected that these references are precise, high-performing in terms of drive strength, possess a fast response time, and are insensitive to process, supply voltage and temperature variations. Moreover, the accuracy of the reference is a key source of error and can degrade the overall effective resolution of the measurement, thus affecting the system performance. Some of the blocks which require such voltage references are data converters (A/D, D/A), opamps, low-dropout (LDO) regulators, SERDES, oscillators etc. Bipolar junction transistor (BJT) devices are usually the key components of such benchmark analog circuitry, thanks to their linear dependence on temperature as well as robustness to manufacturing process variability.

Vertical fin-shaped field-effect transistors (FinFET) in CMOS fabrication processes have emerged as a strong contender to the planar CMOS technology for sub-28nm nodes due to the cost (area scaling) as well as improved performance (higher speed transistors, lower off-state device leakage). This has led state-of-the-art devices used by the semiconductor industry to transition to the FinFET devices at around the 16-nm CMOS node, especially

for Field Programmable Gate Array (FPGA) and large System-on-Chip (SoC). These devices are characterized by the gate covering the channel along the vertical dimension, thus having a better control of the channel current [3]. FinFET technology has been widely adopted for high-performance computing chips and large mixed-signal System-on-Chip (SoC). This work addresses the problem of realizing high-precision voltage references in deep nanoscale FinFET process technology. Such a problem requires consideration both at the device and circuit levels as well as their co-optimization. Hence, this thesis begins with a BJT device and its characterization in 7-nm FinFET process followed subsequently by utilizing these constructed device models for circuit realization.

This work highlights the BJT device SPICE modeling and characterization results in 7-nm FinFET CMOS technology, giving special emphasis to the BJT's variability and process spread in order to provide insights into key device-circuit interactions. This guides the optimization choices for the designer, which is crucial for analog design in deep nanoscale CMOS.

BJT device characterization in 7-nm FinFET process is essential to enable not only precision voltage references, but also for other circuits such as temperature sensors, current references which use BJT at its core. Besides, the key parameters characterized helps predict the limit of achievable precision due to the underlying device inaccuracy. Subsequently, this achieves the aim of quantifying the system application performance. Measurement results of two test-chip device arrays are presented to demonstrate the feasibility of using BJTs in FinFET CMOS and the associated operating conditions (bias current density) optimal for achieving high-precision circuits. Instead of using the standard BJT layout structure available from the foundry, a merged layout structure was implemented which further saves 20% of the silicon area. This area saving layout of the BJT device could be useful for certain applications such as distributed reference or thermal sensors in large SoC. In the next part of the work, we present a 1-V precision voltage reference with a programmable temperature coefficient (*'temp-co'*).

The voltage reference is based on a parasitic BJT realized within the process steps available in the chosen 7-nm FinFET technology and characterized in the earlier part of this thesis. The targeted precision for this work was achieved by employing trimming techniques to

manage the process spread and using two curvature compensation methods. The architecture together with these techniques ensured that the circuit was capable of handling any *variation* in the device models since the process technology was not mature at the time of design. In addition, the proposed architecture also is capable to *program* the ‘*temp-co*’ which is shown to be beneficial in certain applications, to compensate for any system-level thermal degradation.

The reference circuit was implemented in a 7-nm TSMC FinFET technology and achieves a maximum inaccuracy of $\pm 0.2\%$ and a minimum *temp-co* of 6ppm/ $^{\circ}\text{C}$ from -45°C to 125°C , which is favourable in comparison to state-of-the-art voltage references. Furthermore, its *temp-co* is digitally programmable between $-7\text{ mV}/100^{\circ}\text{C}$ to $+8\text{ mV}/100^{\circ}\text{C}$ using a 7-bit *flat-trim* control code, which is an additional feature of architecture to cope with thermal gradients across large SoC by compensating system-level performance across temperature. The proposed voltage reference has a line regulation of $0.1\%/V$, and occupies area of 0.078 mm^2 .

CHAPTER

1

Introduction

Voltage references are the key analog circuits required for almost all analog, digital and mixed-signal circuits and systems. They are typically embedded in system-on-chip (SoC) and Field Programmable Gate Arrays (FPGA), where they are indispensable for functional blocks, such as A/D and D/A converters, low-dropout (LDO) regulators, filters, oscillators and serializer-deserializer (SerDes). For instance, A/D converters require precise voltage or current references to determine the unknown input signal. The key requirements of voltage/current references are high precision [4] [5], low temperature drift and long-term stability and high rejection to power supply noise [6] [7]. It should be noted that the high precision requirements are application-dependent, since in some cases absolute accuracy is required while, in others, only relative accuracy is significant and any absolute shift in magnitude is benign. Additional sources of error include electrical device noise (flicker, thermal) as well as line/load variation, aging, and package stress. In addition, certain applications, such as Internet-of-Things (IoT), operate in an energy-constrained environment and hence this leads to the need for analog circuits being able to work with a low-voltage supply.

There has been a trend in the semiconductor industry towards more integration on a single chip leading to SoC solutions. Typically, an SoC consists of fabricating digital, RF and analog circuits on a single chip. Such an SoC has two requirements:

1. satisfy conflicting requirements, such as high-speed and low supply for digital circuits, while requiring precision for analog circuits.
2. Need to be compact since off-chip component use must be minimized and different chips are now integrated in a single SoC on the printed circuit board (PCB). This reduces the bill of materials (BOM) and subsequently the cost and area consumed for the system realization.

Since the majority of the area in such SoCs is consumed by digital logic, it is implemented in advanced process technology. This is usually cost-effective for applications such as mobile phones and processors, where the volume justifies the cost of moving to the next process node. Additionally, it poses additional challenges for the implementation of general analog circuits. Therefore, realizing bandgap references and temperature sensors with high precision is an important problem to solve. These circuits enable power delivery as well as power and thermal management, which are essential for these types of SoC.

One of the main specifications of a voltage reference is its initial accuracy, which quantifies the effect of process variation, mismatch, and package stresses on its accuracy. While the systematic component can be calibrated, the random component affects each sample uniquely. Therefore, a statistical measure is required using a large number of samples. The initial accuracy (A) is defined as the ratio of three times the standard deviation (3σ) over its mean (μ) for a large number of samples as given by Eq. (1.1)

$$A = \pm \frac{3 \cdot \sigma(V_{\text{ref}})}{\mu(V_{\text{ref}})} \quad (1.1)$$

The circuit designer uses models of the components, such as BJTs, MOS transistors, and passives for implementing the reference circuitry. These models are used to arrive at the overall spread of the reference by simulating across the process, voltage, and temperature range combinations. This gives the maximum and minimum spread of the output reference. Monte Carlo models for achieving a certain confidence interval are used to calculate the standard deviation. Typically, the specification is quoted post-trimming. The simulation

models also give guidance to the designer on the expected accuracy and the required amount of trimming bits, which are like “knobs” to bring a sample from “*out of range*” to “*within specification*” by adjusting the component value. During the measurement phase, trimming is employed over a large number of samples, ideally across different wafers and lots, before the final accuracy specifications are arrived at.

Another key parameter which determines the temperature sensitivity or temperature drift of the voltage reference is temperature co-efficient (‘*temp-co*’ or TC), in ppm/°C, is defined as :

$$TC = 2 \frac{V_+ - V_-}{V_+ + V_-} \cdot \frac{1}{T_{hi} - T_{lo}} \cdot 10^6 \quad (1.2)$$

where T_{hi} and T_{lo} are the maximum and minimum of the die temperature range, respectively, while V_+ and V_- are the maximum and minimum values of the reference, respectively, in the same range of temperature. This method is known as a “box method” to determine the ‘*temp-co*’.

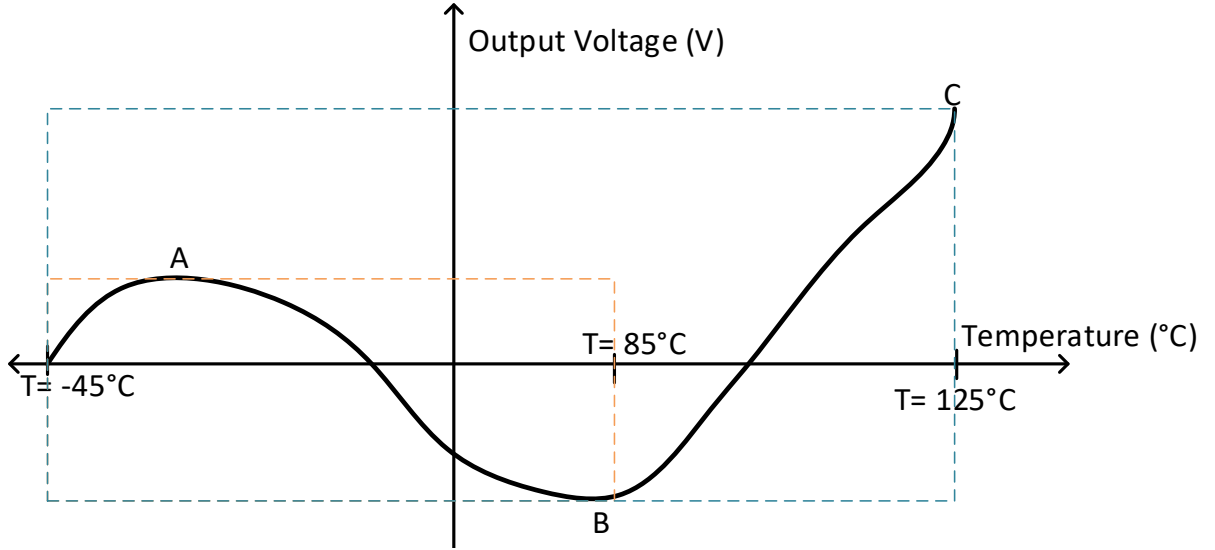


Figure 1.1: Box method to determine the ‘*temp-co*’ of a voltage reference.

Figure 1.1 shows representative figures for the two temperature ranges. Equations (1.3) and (1.4) summarize the ‘*temp-co*’s’.

$$TC_1 = 2 \cdot \frac{A - B}{A + B} \cdot \frac{1}{85^\circ\text{C} - 45^\circ\text{C}} \cdot 10^6 \quad (\text{ppm}/^\circ\text{C}) \quad (1.3)$$

$$\text{TC}_2 = 2 \cdot \frac{C - B}{C + B} \cdot \frac{1}{125^\circ\text{C} - 45^\circ\text{C}} \cdot 10^6 \quad (\text{ppm}/^\circ\text{C}) \quad (1.4)$$

The allowable reference drift (*'drift'* or TD in ppm/ $^\circ\text{C}$) is shown in Fig. 1.2. The various graphs in Fig. 1.2 are for a certain system accuracy (A/D or D/A conversion resolution of N bits) requirement together with the total temperature range (T_r in $^\circ\text{C}$) based on Eq. (1.5).

$$\text{TD} = \frac{10^6}{2^N} \cdot \frac{1}{T_r} \quad (1.5)$$

The demand on precision reference becomes stringent for achieving a higher resolution across a larger temperature range. [8] and [9] are some of the best commercially available reference which provides approximately 1–1.5 ppm/ $^\circ\text{C}$). For example, this does not meet the demands of a stable precision reference for greater than 15 bits ADC. Therefore, in such situations, a continuous self-calibration scheme should be employed. Continuous self-calibration will ensure the reference drift will be periodically brought into the limit, together with a good heat sink to ensure the temperature range is within specified limits.

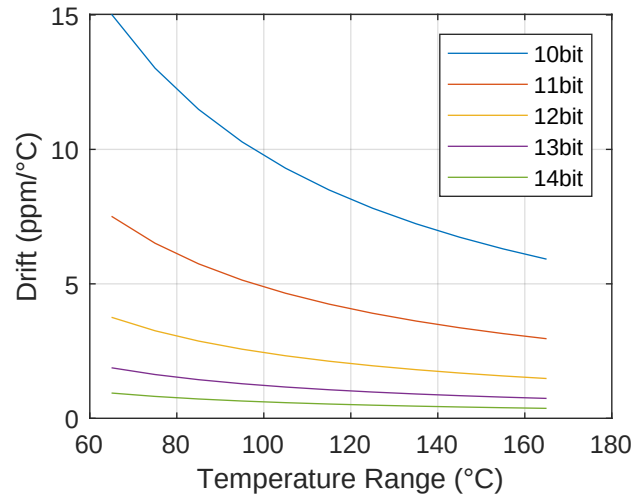


Figure 1.2: Bandgap *'temp-co'* performance required for various system accuracy across different temperature range.

Usually, the temperature drift or drift due to aging is a very challenging problem in bandgap references [10]. The initial error in the bandgap reference can be trimmed, but the

long-term drift is difficult to compensate. When choosing a reference for an A/D converter or any system, care must be taken to ensure that the drift due to temperature and aging over the total life-time of operation of the system is taken into consideration in the system error budget for the reference.

A long-term stable reference ensures repeatability. It is not common to find the long-term stability of the references specified, but in some critical applications where this is needed (such as automotive grade, medical industry) it is typically specified in ppm/1000 hrs. Long-term drift in precision analog circuits is a “random-walk” phenomenon since it is due to the microscopic effects [10]. In order to calculate its equivalent for the period of life-time (hrs), the resulting long-term drift (ppm) is given by the product of drift (ppm/1000 hrs) and square root of the ratio of the life-time operation (hrs) per 1000 hrs. Since drift is a “random-walk” phenomenon, a square root of the ratio of the life-time operation (hrs) per 1000 hrs is used instead of the life-time per 1000 hrs by itself as it gives a pessimistic estimate [10].

Buried Zener diodes offer excellent long-term stability as they are at the lowest level in the vertical cross-section of silicon and hence are less susceptible to contamination at the surface [10].

Robustness of the voltage reference against supply voltage disturbance can be quantified using line regulation (LR), which provides the output voltage variation against the shift in supply voltage, and the power supply rejection ratio (PSRR), which quantifies the reference swing against AC supply disturbance swing.

$$\text{LR} = \frac{\Delta V_{ref}}{\Delta V_{supply}} \quad (1.6)$$

$$\text{PSRR} = 20 \cdot \log \frac{\Delta V_{ref}}{\Delta V_{supply}} \quad (1.7)$$

While the ability of the voltage reference to remain constant despite changes in the reference’s load is termed load regulation (LDR) given by (1.8).

$$\text{LDR} = \frac{\Delta V_{ref}}{\Delta I_{out}} \quad (1.8)$$

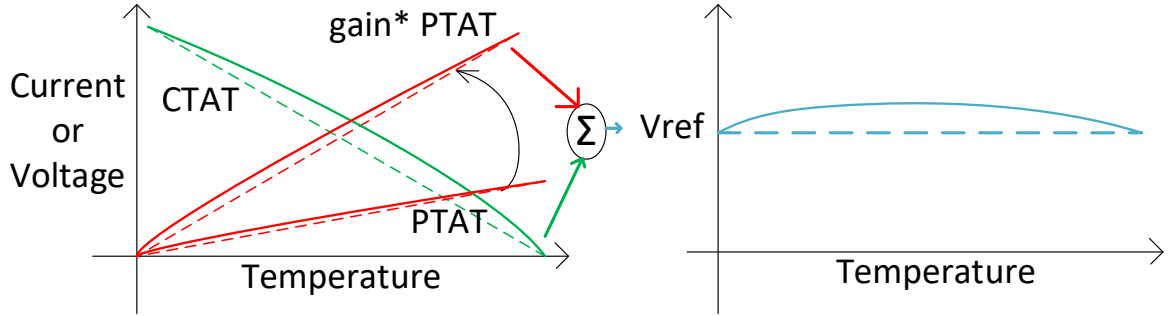


Figure 1.3: Basic constituents of reference circuits.

1.1 Overview of Voltage Reference Circuits

Semiconductor technology does not provide any electrical quantity which is, by itself, independent of ambient temperature. Generally, such a quantity is derived by combining two available quantities, which have an opposite dependence on the ambient temperature. This is more clear for a resistance, a series of positive ‘*temp-co*’ resistors together with resistors of different materials which have negative ‘*temp-co*’ will provide a temperature independent resistance. This is not so easily applicable for voltages. Generally, voltage reference circuits utilize two contributing components with opposite temperature coefficients (e.g., positive/negative ‘*temp-co*’s of current/voltage), which can provide a flat characteristic when proportionately summed using a scaling factor (gain). These ‘*temp-co*’ components are typically derived from a BJT, where the emitter-base voltage is complementary to the absolute temperature (CTAT) while the difference between a pair of BJTs with different current density is proportional to the absolute temperature (PTAT). BJT is used at the core of the voltage reference because the emitter-base voltage, V_{eb} , of BJT is better behaved as it is linear and varies less compared to a threshold voltage or mobility of MOS transistors [11]. Thus, the majority of voltage references used in industry still place BJT’s PN junction at the heart of the architecture.

Figure 1.3 shows a conceptual diagram illustrating the above principle. The output voltage would be perfectly flat if the two individual components, i.e., PTAT and CTAT, were perfectly linear (shown by dotted lines). In reality, both of these constituents exhibit

some (although in practice well-characterized) non-linearity (shown by solid lines). A basic bandgap circuit involves compensation of the first-order temperature coefficient, thus leaving the second and higher-order non-linearities (shown by the solid line around V_{ref}). In the quest for better flatness, techniques have been developed [12] to cancel the higher-order nonlinear dependence.

1.1.1 Theoretical Analysis of BJT-based Voltage References

One of the key components used to generate the temperature-dependent voltage/current in most bandgap topologies is based on the base-emitter voltage of a diode-connected BJT. The collector current I_c of a BJT as a function of the emitter-base voltage V_{eb} in the forward-active region is given by Eq. (1.9).

$$I_c(T) = I_s(T) \exp \frac{qV_{eb}}{\eta kT} \quad (1.9)$$

where: T = absolute temperature,

k = Boltzmann constant,

q = electron charge,

η = non-ideality factor,

I_s = saturation current.

I_s is the saturation current, which is proportional to the base-emitter area and given by:

$$I_s(T) = \frac{qAn_i^2 D(T)}{N_B} \quad (1.10)$$

A = emitter area

$n_i(T)$ = intrinsic carrier concentration

$D(T)$ = effective minority carrier diffusion constant in the base

N_B = total impurities per unit area in the base. It can be shown from Einstein relation that the diffusion constant D relates to carrier's drift mobility μ as:

$$D(T) = \frac{kT}{q} \mu(T) \quad (1.11)$$

The mean mobility of minority carriers (μ) in the base has a temperature dependency:

$$\mu(T) = BT^{-n} \quad (1.12)$$

where B and n are constants. Using the above equations, we can arrive at the bandgap voltage at a given temperature T :

$$V_{eb}(T) = V_G(T) + \frac{kT}{q} \ln \frac{I_c(T)}{CT^n} \quad (1.13)$$

where: $V_G(T)$ = bandgap voltage of silicon as a function of temperature, and C = constant. It can be seen from (1.13) that V_{eb} has a CTAT characteristic due to strong dominance of the term T^n in the denominator. Finally, a more generic form of the above equation at any arbitrary temperature T as a function of a specified reference temperature T_r is given by Tsividis [13] as:

$$V_{eb}(T) = V_G(T) - \frac{T}{T_r} V_G(T_r) + \frac{T}{T_r} V_{eb}(T_r) - (n - \delta) \frac{kT}{q} \ln \frac{T}{T_r} \quad (1.14)$$

where: n = a constant less than 4 [11], depending on the doping level,

δ = order of temperature dependence of collector current shown by Eq. (1.15). The cause of non-linearity is due to the term $T \ln(T)$ in Eq. (1.14).

$$\delta = \theta_r \frac{dI_c/dT}{I_c/T} \quad (1.15)$$

In (1.14), the value of δ depends on the ‘temp-co’ of the collector current [13]. If the collector current is PTAT : $\delta = 1$, if the collector current is ZTAT : $\delta = 0$. This has been exploited [12] to correct for the curvature of the bandgap reference. It can be shown [14] that an approximate expression for the ‘temp-co’ of emitter-base voltage is given by:

$$\frac{\partial V_{eb}}{\partial T} = \frac{V_{eb} - (4 + m)V_T - E_g/q}{T} \quad (1.16)$$

where: $m = -3/2$,

E_g = bandgap energy.

The above expression shows the source of the CTAT part of Fig. 1.3, which is nothing but the emitter-base voltage of the BJT. We now proceed to determine the PTAT part.

$$V_{eb} = \eta \frac{kT}{q} \ln \left(\frac{I_c}{I_s} \right) = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_e - I_b}{I_s} \right) \quad (1.17)$$

The relation between emitter-base voltage (V_{eb}) to the collector current (I_c) and the saturation current (I_s) of the BJT is given by Eq. (1.17), where:

η = non-ideality factor,

k = Boltzmann constant,

q = charge,

T = absolute temperature.

Since the silicon substrate is commonly tied to ground, PNP BJT is biased via the emitter terminal. The emitter current (I_e) is related to the base current (I_b) by the finite current gain (β) of the BJT:

$$I_e = I_{bias} = (1 + \beta)I_b \quad (1.18)$$

While the collector current (I_c) is related to the emitter current (I_e) by Eq. (1.19).

$$I_c = \beta I_b = \beta \frac{I_{bias}}{1 + \beta} \quad (1.19)$$

Substituting Eq. (1.19) in Eq. (1.17) gives:

$$V_{eb} = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_{bias}}{I_s} \frac{\beta}{\beta + 1} \right) \quad (1.20)$$

In the above expression, non-ideality factor η depends on the current density used for biasing the BJT, the saturation current depends on the process as well as temperature. In the fine-geometry technologies, h_{21} or β -factor of the BJT is very low and the process variation is observed to be larger. This can be explained because of the base-emitter junction being squeezed inside the fin [15]. The difference in voltage between two BJTs of emitter area ratio

1:N is given below:

$$V_{eb1} = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_{bias}}{I_s} \frac{\beta_1}{\beta_1 + 1} \right) \quad (1.21)$$

$$V_{ebn} = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_{bias}}{I_s/N} \frac{\beta_n}{\beta_n + 1} \right) \quad (1.22)$$

$$\Delta V_{eb} = V_{ebn} - V_{eb1} = \eta \left(\frac{kT}{q} \right) \ln \left(N \frac{\beta_n}{\beta_1} \frac{\beta_1 + 1}{\beta_n + 1} \right) \quad (1.23)$$

We see from Eq. (1.23) that the difference in emitter-base voltage is PTAT. This is because the saturation current, which has a temperature dependency, is cancelled due to the difference, while in the emitter-base voltage it results in a CTAT voltage. It is assumed for simplicity in the analysis that the biasing of the BJT pair is done such that η is constant for both devices (size 1 and N).

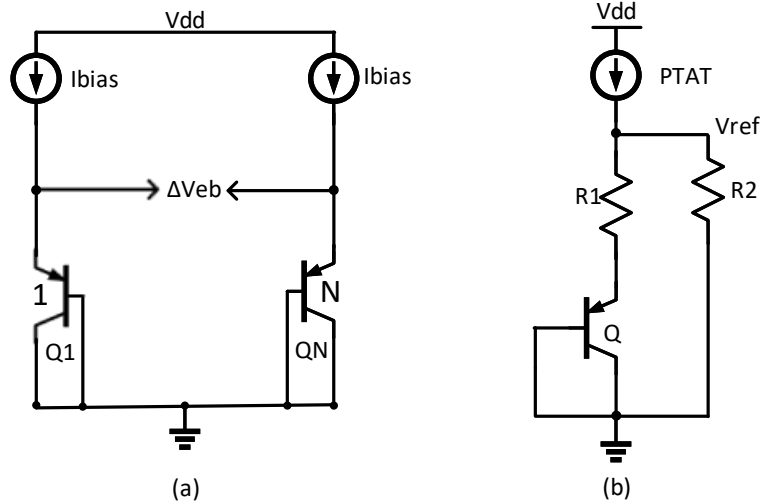


Figure 1.4: Conceptual diagram of the reference circuit.

A conceptual diagram [14] for generating a reference is shown in Fig. 1.4, which consists of two parts. The first part, shown in Fig. 1.4(a), is a generation of the PTAT current source based on the difference between emitter-base voltage of BJTs Q_1 and Q_N . The second part, shown in Fig. 1.4(b), consists of BJT Q which is biased using the PTAT current source. The emitter-base voltage of Q has a CTAT characteristic and hence, if an additional voltage is stacked on top of the CTAT voltage which has PTAT characteristic and with the right

multiplying factor, we can generate a temperature-independent voltage reference. This can be simply implemented using R_1 which provides a voltage drop proportional to PTAT current times the resistance. The final temperature-independent voltage generated can be further divided by shunting with resistor R_2 .

The BJTs shown in Fig. 1.4 are typically parasitic vertical BJT available in Complementary Metal Oxide Semiconductor (CMOS) processes which will be dealt in detail in the second chapter. BJT can be considered in following important aspects, namely: 1) base resistance, 2) current gain, 3) early effect, 4) package stress [16]. The equivalent network for the BJT is shown in Fig. 1.5. It is observed that the base resistance can be modeled as a function of base current [17]. Conventionally, upper and lower case distinguishes between extrinsic and intrinsic voltages for the analysis, as shown below :

$$V_b = V(b), v_b = V(b_i) - V(e_i),$$

$$V_c = V(c), v_c = V(c_i) - V(e_i).$$

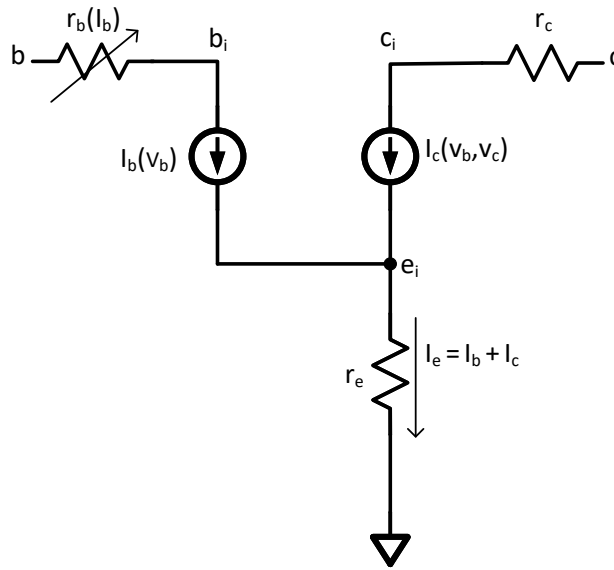


Figure 1.5: BJT equivalent network [17].

The intrinsic base resistance of a parasitic vertical BJT is large [18], [17]. This, together with the associated low current gain, will result in a large intrinsic voltage (v_b) at the base of the BJT versus the ground. Therefore, care should be taken to ensure the bias current is small, so that $V_{eb} \gg v_b$, for all the BJT used in the circuit. This is generally true for

currents below 1 mA. Another drawback is the inherently lower current gain of BJT (which is decreasing further in finer technology nodes). This is because in a PNP BJT device, the bias current can be controlled at its emitter terminal. The emitter-base voltage depends on the collector current. Therefore, there is an additional dependence on β , especially for low values of β . This is because the approximation of the emitter current being equal to the collector current is no longer valid. Therefore, one circuit technique to circumvent this problem is shown in Fig. 1.6.

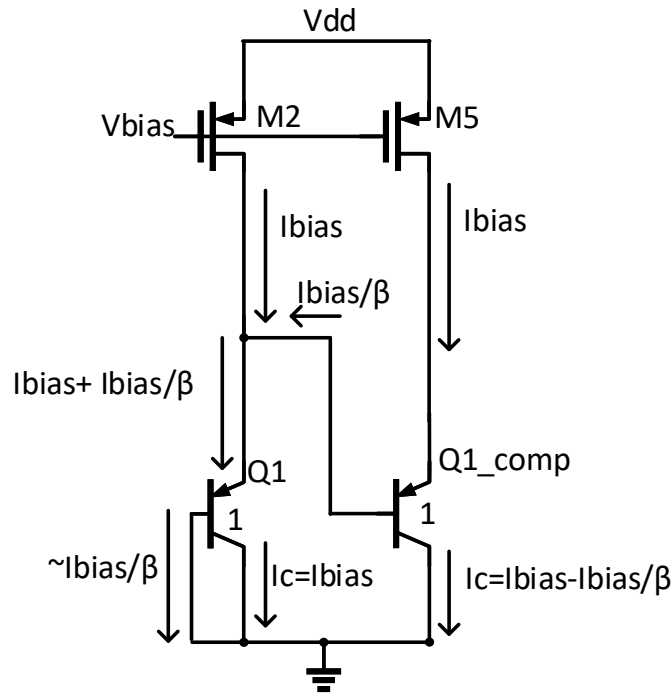


Figure 1.6: Base-current compensation circuit.

In this circuit, Q_1 is the actual BJT used in the main reference circuit while $Q_{1,comp}$ is an auxiliary device used to compensate for the additional base current. $Q_{1,comp}$ provides the additional current I_{bias}/β which ensures that the actual collector current is the same as I_{bias} . In a non-compensated device, the collector current is $I_{bias} - I_{bias}/\beta$. One drawback of this technique is that it requires a higher supply voltage since it needs to accommodate an additional emitter base voltage at the base of $Q_{1,comp}$.

Conventional bandgap references which employ the temperature dependence of BJT junction to create PTAT and CTAT components, provide first-order temperature compensated

references. These are limited by the emitter-base non-linearity and can provide the best ‘*temp-co*’ of ~ 20 ppm/ $^{\circ}\text{C}$ across the range of 100°C . Higher accuracy can be achieved by canceling some of the non-linearity of emitter-base junction voltage. This leads to an approximate second-order curvature corrected bandgap reference for applications which require precision. It is at the cost of additional power and area consumed by the auxiliary circuit which either adds a compensating voltage or current to the reference. The two main techniques employed in the literature for correcting the curvature of a first-order temperature compensated reference are:

1. Use of an additional pair of BJTs whose curvature is used to cancel the non-linearity of the main voltage reference [6] [12].
2. Use of a piecewise-linear method, whereby a nonlinear current/voltage is added together with the first-order bandgap to compensate for the non-linearity [19].

1.2 Bandgap Reference Architectures

It was not until 1964 that Hilbiber [20] showed a possible implementation of a reference voltage circuit. Hilbiber showed that as the junction doping increased, there is an increase in V_{eb} and $d(V_{eb})/dT$ becomes less negative. An increase in current density also has the same effect. Two sets of stacked diodes (m, n such that $m - n = 1$) are used which are biased at two different currents. The difference between these stacked diode voltages is shown to be independent of temperature. Subsequently, in 1965, Widlar [21] showed the first representation of the proportional-to-absolute-temperature (PTAT) voltage difference between the emitter-base voltages of diodes biased with different current densities. In 1971, Widlar [22] subsequently published the first bandgap circuit followed by another architecture proposed by Brokaw [23] in 1974. These are shown in Fig. 1.7.

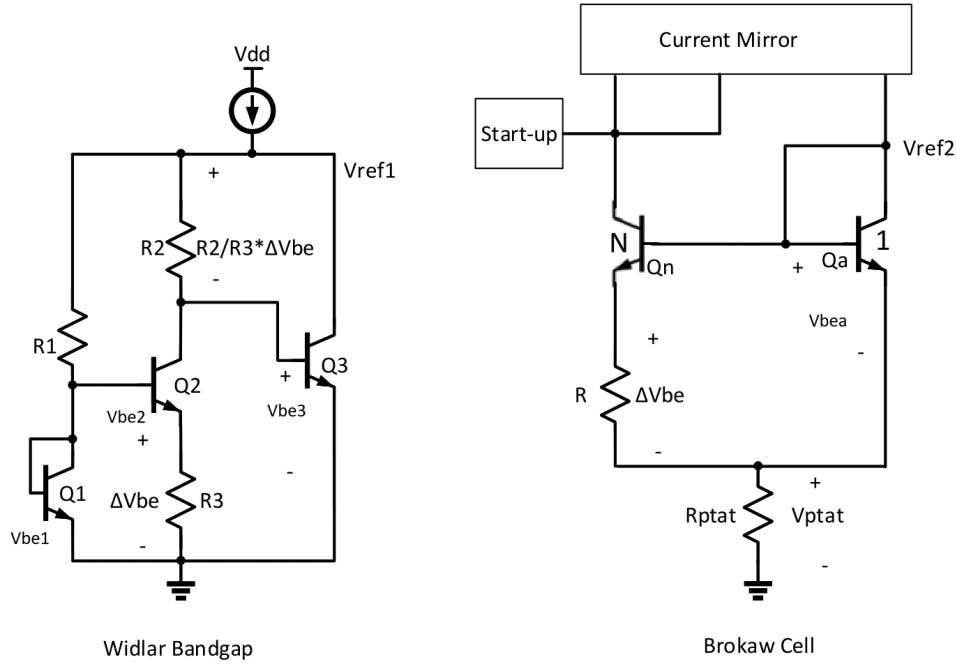


Figure 1.7: Widlar's bandgap [22] and Brokaw cell [23].

In the Widlar's bandgap, the base-emitter voltage across Q_1 is given by Eq. (1.24) while the voltage across R_3 is given by Eq. (1.25)

$$V_{be1} = \left(\frac{kT}{q} \right) \ln \left(\frac{I_c}{I_s} \right) \quad (1.24)$$

$$\Delta V_{be} = V_{be1} - V_{be2} = \left(\frac{kT}{q} \right) \ln \left(\frac{I_{c1} I_{s2}}{I_{c2} I_{s1}} \right) \Delta V_{be} = \left(\frac{kT}{q} \right) \ln \left(\frac{R_2}{R_1} \right) \quad (1.25)$$

For a high β factor, it can be assumed that $I_c \approx I_e$ which implies that the current through R_2 is the same as that through R_3 . This is given by Eq. (1.26)

$$\frac{\Delta V_{be}}{R_3} = \frac{\Delta V_{R_2}}{R_2} \quad (1.26)$$

Therefore, the voltage across resistor R_2 , i.e. ΔV_{R_2} , is given by Eq. (1.27).

$$\Delta V_{R_2} = \frac{R_2}{R_3} \Delta V_{be} \quad (1.27)$$

The overall output reference voltage is given by Eq. (1.28)

$$V_{ref1} = V_{be3} + \frac{R_2}{R_3} \Delta V_{be} = V_{be3} + \frac{R_2}{R_3} \left(\frac{kT}{q} \right) \ln \left(\frac{R_2}{R_1} \right) \quad (1.28)$$

Brokaw cell forms the core for many state-of-the-art bandgap circuits [24], [25], [26]. Fig. 1.7 shows the Brokaw cell where the current mirror forces equal currents into unequal diodes Q_a , Q_n which have a ratio of emitters as N . The difference between the two BJT base-emitter voltages is applied across the resistor R , producing a PTAT current and subsequently a PTAT voltage across R_{ptat} .

$$V_{bea} = \left(\frac{kT}{q} \right) \ln \left(\frac{I_c}{J_s \cdot A} \right) \quad (1.29)$$

$$I_{ptat} = I_{cQ_a} = I_{cQ_n} = \frac{\frac{kT}{q} \ln(N)}{R} \quad (1.30)$$

$$V_{ptat} = 2 \cdot I_{ptat} \cdot R_{ptat} \quad (1.31)$$

$$V_{ref2} = V_{bea} + 2 \cdot I_{ptat} \cdot R_{ptat} = V_{bea} + 2 \cdot \frac{\frac{kT}{q} \ln(N)}{R} \cdot R_{ptat} \quad (1.32)$$

Note that one other possible solution for Eq. (1.30) is the condition $I_{ptat} = I_{cQ_a} = I_{cQ_n} = 0$ which is a stable but undesired state. Therefore, bandgap references typically involve an additional, usually a low-area circuit, called start-up which injects enough current into the main loop such that the bandgap reference is pulled out of this undesired stable state to the desired operation stable state. Typically, in Brokaw cell shown in Fig. 1.7, the start-up circuit draws current from the low impedance node when the circuit is in the zero state. It mirrors and injects this current into Q_a until the desired current in the loop, given by Eq. (1.30), is reached.

The conceptual description of Fig. 1.3 shows the various components of a simple bandgap reference. The related circuit blocks used to implement them individually, as shown in Fig. 1.4, can be combined in a simple bandgap reference circuit implementation (in this instance, the core is based on PNP BJT) represented in Fig. 1.8.

a flatter voltage reference is to use a highly resistive polysilicon (i.e. lightly doped polysilicon) since it has a negative '*temp-co*'. The drawback of using these resistors is that they increase power consumption at high temperatures.

One of the main drawbacks of voltage mode bandgap architecture such as Brokaw cell, Widlar cell is that the intrinsic bandgap reference voltage of 1.205 V severely limits the adoption of this architecture for low supply voltages. Besides, the current mirror error, as well as the error from non-ideal clamp devices, especially at low supply voltages, limit the architecture. It should also be noted that an absolute '*temp-co*' of 30–50 ppm/°C is not significant for a 3.3 V or 5 V system, while it can be an important factor for lower supply voltages, for example below 1.5 V.

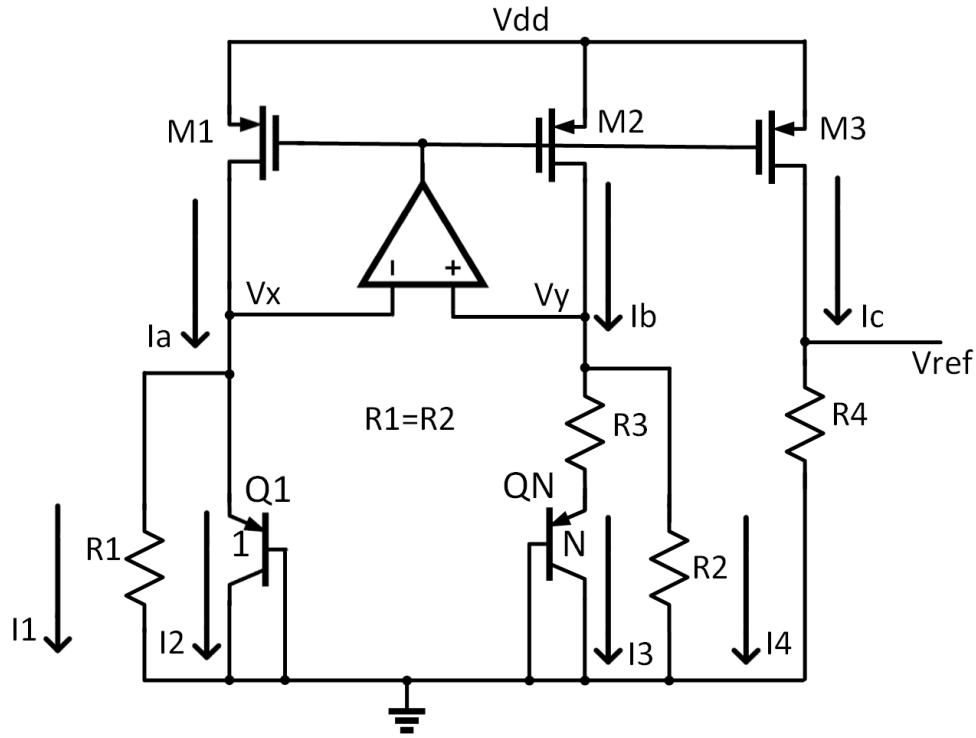


Figure 1.9: A first-order curvature-compensated low-voltage single op-amp based reference [26].

An alternative approach to overcome the supply voltage limitation is to move to the current domain summation of the constituents. One of the most popular bandgap architecture is that proposed by Banba et al., drawn in Fig. 1.9. The core of the bandgap is based on the feedback loop formed by the amplifier together with the BJT pair (whose area ratio is 1:*N*), which ensures V_x and V_y nodes are at the same voltage, which is the emitter-base voltage of

Q_1 . The individual current in each branch is given by I_1 , I_2 , I_3 , I_4 below:

$$I_1 = \frac{V_{eb}}{R_1} \quad (1.35)$$

$$I_3 = \frac{\Delta V_{eb}}{R_3} \quad (1.36)$$

$$I_4 = \frac{V_{eb}}{R_2} = \frac{V_{eb}}{R_1} = I_1 \quad (1.37)$$

$$I_2 = I_a - I_1 = I_b - I_4 = I_3 = \frac{\Delta V_{eb}}{R_3} \quad (1.38)$$

The overall output voltage is given by the mirroring of currents $I_a = I_b = I_c$ together with the load resistance R_4 . The first term in Eq. (1.39) represents the CTAT component while the second term represents the PTAT part. By choosing the correct ratio between R_1/R_4 and R_3/R_4 , a temperature-independent reference of a certain magnitude can be obtained.

$$V_{ref} = \left(\frac{V_{eb}}{R_1} + \frac{\Delta V_{eb}}{R_3} \right) \cdot R_4 \quad (1.39)$$

Therefore, a single loop generates both the CTAT and PTAT currents. The PTAT current is useful to bias the BJT while the CTAT current flows through the identical shunt resistors. This architecture has many benefits; namely, it provides good performance at low supply voltages, while trimming can be done using resistors. However, this architecture does not compensate for any V_{be} non-linearities.

1.2.1 Bandgap References at Low Supply Voltage

The current-mode bandgap reference proposed in [26], [12] has overcome the limitation of voltage-mode bandgap reference, which requires a supply $>1.4\text{ V}$. They still require a supply voltage $>0.9\text{ V}$ because of the 0.7 V for the PN-diode turn-ON voltage and 0.2 V for the PTAT current source. They also rely on the accurate summation of constituent currents which are generated by another feedback loop in the core. This architecture therefore falls short in tight accuracy performance.

There have been several attempts in the literature to overcome the supply limitation. MOS-based references are an alternative to overcome the 0.7 V headroom required by the PN-diode in BJT based references. In general, a MOS based reference exploits the negative temperature dependence of the MOS device threshold voltage and combines it with a PTAT characteristic obtained from MOS device in weak inversion. Another approach is the use of dynamic threshold MOS transistor, which is nothing else but an MOS device with an interconnected well and gate, instead of BJT. This has enabled the realization of bandgap reference with supply voltages going down to 0.85 V [28]. With certain modifications (using enhancement and depletion mode devices) in a MOS/SIMOX process, a bandgap reference operating from the supply voltage down to 0.6 V has been demonstrated [29]. But such designs are not compatible with the standard digital CMOS processes.

Another alternative based on the physical properties of the material is to use the Schottky diode [30], [31] to implement a bandgap reference, which has a much lower forward diode voltage ($\sim 0.2\text{--}0.4\text{ V}$) compared to the PN-diode ($\sim 0.7\text{ V}$). A Schottky diode is realized in a standard CMOS process, by contacting directly to N-well without using N+ implants. Cross-section of such a structure is shown in Fig. 1.11.

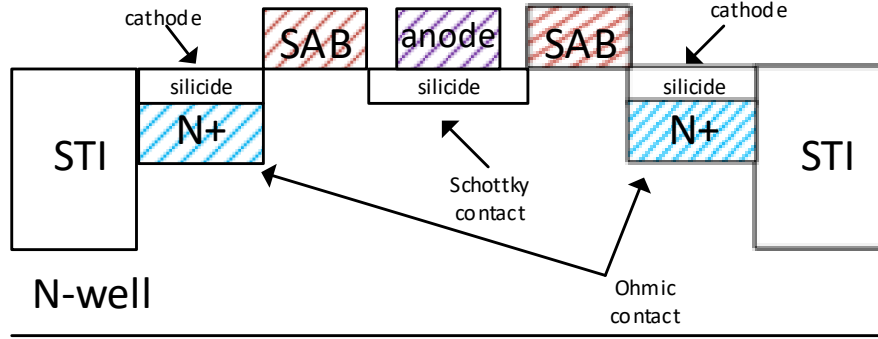


Figure 1.11: Cross section of Schottky diode in standard CMOS process [31].

Silicides are used in modern CMOS processes at silicon-metal interfaces. A Schottky barrier diode is formed where the silicide which is in contact with the metal is also in contact with the N-well. This forms the anode while the N-well is contacted via ohmic contact through N+ implants to form the cathode. A Schottky barrier voltage depends on the work-function of the metal and semiconductor and is in the range of 0.2 V to 0.4 V. Therefore, this makes the Schottky diode a candidate for the replacement of the PN-diode in the bandgap reference architecture. The difference of forward voltages between two Schottky diodes biased with different current densities has a PTAT characteristic while the forward voltage has a CTAT characteristic ($-0.4 \text{ mV}/^\circ\text{C}$). Ref. [30] has employed Schottky diodes to design voltage references operating from a 2.5 V supply but [31] showed a low-voltage version using current-summation topology similar to [32] which uses PN-diode junction at its core. Without any trimming, the temperature coefficient reported in [31] was $263 \text{ ppm}/^\circ\text{C}$ between 10 to 100°C with a supply voltage of 0.6 V. The output voltage for 18 samples was $251 \text{ mV} \pm 4 \text{ mV}$.

Another research direction towards realizing low supply voltage bandgap was to exploit MOS devices to implement the core of bandgap reference replacing the BJTs. Refs. [31], [33], [34] use the threshold voltage (V_{th}) of MOSFET to generate the absolute reference. These MOS-based references are shown to operate at a supply voltage of sub-1 V down to 0.85 V. Generally, the CTAT is obtained using the negative '*temp-co*' of the threshold voltage, while PTAT is obtained by using the difference between gate-source voltages of weakly inverted

MOS devices with different current densities [31]. Further reduction in the required supply voltage is obtained by biasing the body of a weakly inverted PMOS device as demonstrated in [28]. Ref. [31] showed an ultra-low voltage, MOS-only bandgap reference with an NMOS device with forward-biased body source connection using a deep n-well implant in a standard CMOS technology.

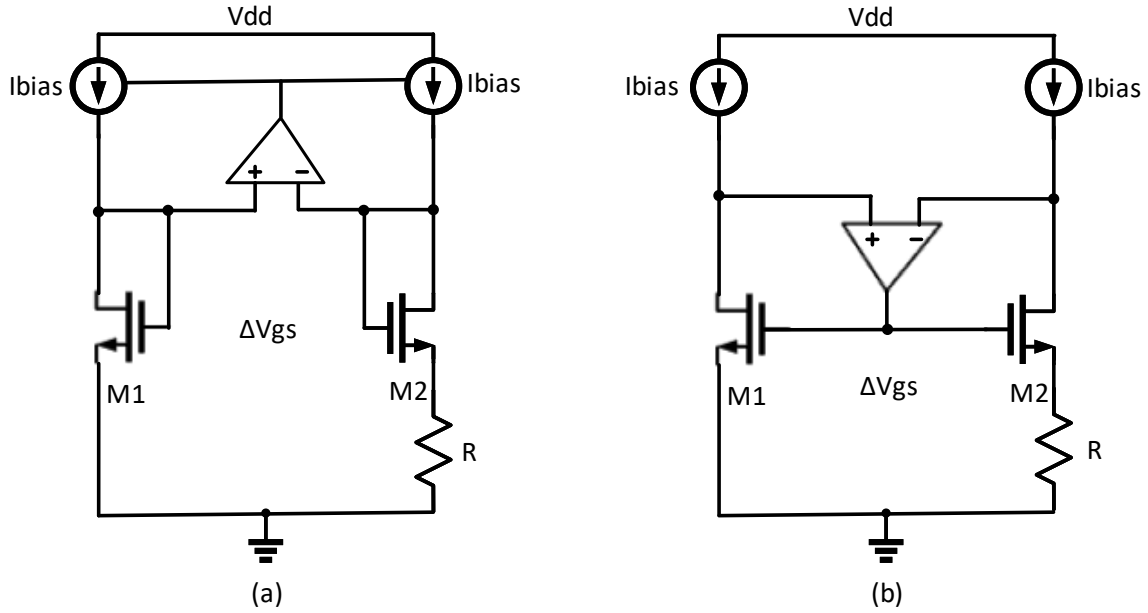


Figure 1.12: MOS PTAT cell: (a) conventional topology, (b) improved topology less susceptible to OTA offset [31].

The PTAT characteristic is obtained by exploiting I - V_{GS} relationship of a MOS operating in weak inversion. Ref. [31] employed the architecture shown in Fig. 1.12(b) which had more immunity to OTA offset compared to the conventional architecture shown in Fig. 1.12(a). In Fig. 1.12(b), the core of PTAT is based on the V_{GS} difference between M_1 and M_2 which across resistor R produces a PTAT current. M_1 , M_2 are deep-nWell NMOS devices with source and body shorted, while CTAT part can be generated using V_{GS} of a weak inversion MOSFET which is biased using PTAT current. The ‘temp-co’ of such a CTAT can be controlled using the bias current magnitude as well as the W/L ratio [31]. The resulting voltage reference [31] was shown to produce $256\text{ mV} \pm 4\text{ mV}$ for 16 samples without any trimming.

Since V_{th} is not well controlled in a manufacturing process, it becomes difficult in a high

volume production to extensively trim it to achieve an accurate reference. Although the Schottky diode and MOS based approaches showed some promise of being candidates for low-voltage references, they still had poor ‘*temp-co*’ and the (untrimmed) performance did not match those of other established architectures (based on BJT or MOS at higher supply voltages). To conclude, the Schottky diode based approach is interesting since it can be traced back to the physical parameter, i.e. Schottky barrier, which is primarily dependent on the material property. While MOS-only reference approach is interesting especially together with forward body biasing. Some works [28] have shown that the matching properties of MOS are promising in the context of ultra-low voltage reference designs.

Another approach in the literature is to use a reverse bandgap concept [35] [36]. A traditional bandgap reference is based on Eq. (1.43), where α is the gain to match the ‘*temp-co*’ between PTAT and CTAT components.

$$V_{bg} = \left(\frac{V_{eb}}{R_1} + \alpha \cdot \frac{\Delta V_{eb}}{R_3} \right) R_4 \quad (1.43)$$

An alternative approach given by Eq. (1.44) is to divide the emitter-base voltage to reduce the ‘*temp-co*’ of the CTAT component, thus balancing the PTAT and CTAT slopes, yielding a temperature-independent reference voltage.

$$V_{bg}^* = \frac{1}{\alpha} \cdot \frac{V_{eb}}{R_1} + \frac{\Delta V_{eb}}{R_3} \quad (1.44)$$

The reverse bandgap approach was proposed by [35], but the architecture depends on a large current-gain of the BJT (PNP or NPN) which is not the case in the finer CMOS technology processes. An improvement of the concept was proposed in [36], as shown in Fig. 1.13, where the reverse bandgap voltage was implemented using switched-capacitor circuitry.

In phase-1, current I_0 biases the BJT and results in V_{ref1} , while in phase-2, the N times the current is used to bias the BJT resulting in additional ΔV_{eb} . These are summarized in Eqs. (1.45) and (1.46). The minimum supply voltage for this circuit to operate is emitter-base

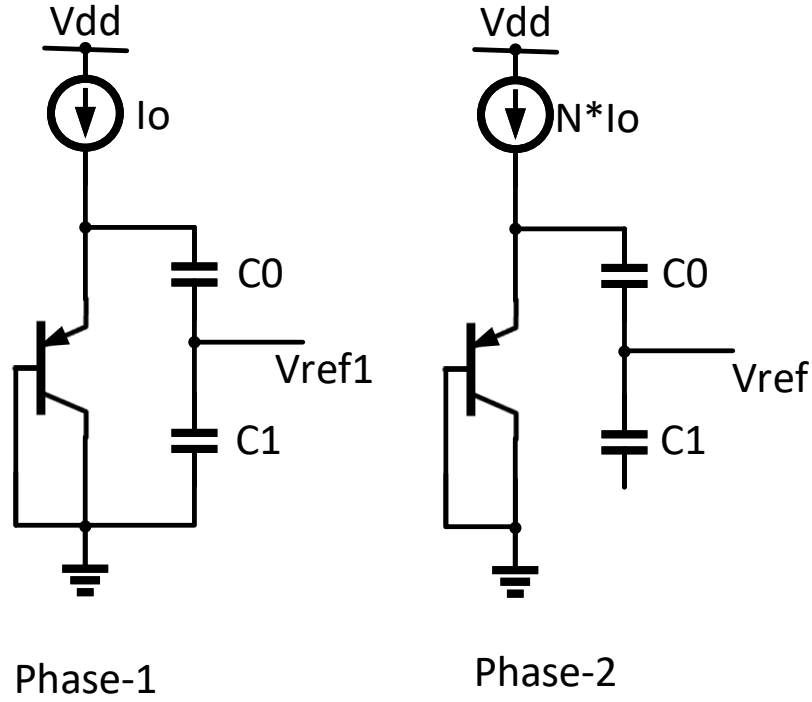


Figure 1.13: Concept of reverse bandgap [36].

voltage plus the V_{DSsat} of the bias current source.

$$V_{ref1} = \frac{C_0}{C_0 + C_1} \cdot V_{eb} \quad (1.45)$$

$$V_{ref} = V_{ref1} + \Delta V_{eb} \quad (1.46)$$

V_{ref} in Eq. (1.46) is flat across the temperature range when:

$$\frac{C_0}{C_0 + C_1} = \frac{1}{\frac{\partial V_{eb}}{\partial T}} \cdot \frac{k \cdot \ln(N)}{q} \quad (1.47)$$

This architecture is based on physical constants and hence is more favorable due to the less likely variations between wafer to wafer. On the other hand, the main drawback, as evident from Eqs. (1.45) and (1.46), is that the resulting reference magnitude is low (~ 200 mV) as well as it is not continuously available. Therefore, the core reference voltage requires to be amplified further as well as to be sampled and held in order to be useful. In [36], an

auto-zeroed amplifier is used to scale up the core reference voltage together with a buffer. Another low-voltage bandgap based on BJT core was presented in [37], where a supply voltage of 0.5 V was sufficient to power the bandgap reference. This is enabled by a switched-capacitor $2\times$ charge pump together with a BJT array. The clock required for the circuitry is generated by a current-controlled ring-oscillator operating at 0.5 V, whose frequency decreases with the input voltage, maintaining the low-power operation, and subsequently it is boosted to $2\times$ supply by the charge-pump before feeding to the switched-capacitor $2\times$ charge pump.

Previous references highlighted some of the architecture choices which achieve low-voltage (low-power) operation. Another aspect of the voltage reference is accuracy. To achieve high accuracy, trimming techniques have been employed in addition to curvature compensation techniques to achieve high precision. Ref. [5] achieved an inaccuracy of $\pm 0.15\%$, over temperature range from -40°C to 125°C , using only a single temperature trim. Higher-order curvature compensation and chopping was employed to remove non-PTAT errors, while a single room-temperature trim removed the residual PTAT errors.

Type of Error	Error Property
BJT saturation current	PTAT
BJT current gain spread	Non-PTAT
Resistor spread	PTAT
Resistor mismatch	PTAT
Opamp Offset	Non-PTAT
BJT base resistance	Non-PTAT
Curvature	Non-PTAT

Table 1.1: Error sources in bandgap references.

Table 1.1 lists the ‘*temp-co*’ of constituent errors in the bandgap from [5]. The base-emitter voltage of the BJT depends on the collector (I_c) and the saturation (I_s) currents. Any process variation results in the saturation current being affected, which is due to the spread of base doping as well as the device dimensions. Therefore, any variation resulting from the spread of I_s is PTAT. Subsection 1.4 discusses the trimming voltage references.

1.3 Error Sources in Bandgap References

The overall system accuracy performance is determined by its constituent blocks. Bandgap references are one of the key contributors and hence it is important to understand their sources of error. Overall accuracy of the bandgap reference can be determined by the key sources of error, such as process technology, circuit topology, trimming, layout pattern, and packaging. In addition, factors, such as load variation and power supply noise, also degrade the accuracy of the reference.

Process variations and mismatches are primarily reduced through careful layout followed by trimming post the manufacturing process. The cost of trimming depends on the end application for which the chip is targeted since a higher level of trimming translates to a longer “*test-time*” to accommodate a higher number of trim bits as well as to ensure thermal equilibrium (in the case of multiple temperature point trims). We consider the Brokaw cell, shown in Fig. 1.14, as an example to analyze the process-induced error sources [38].

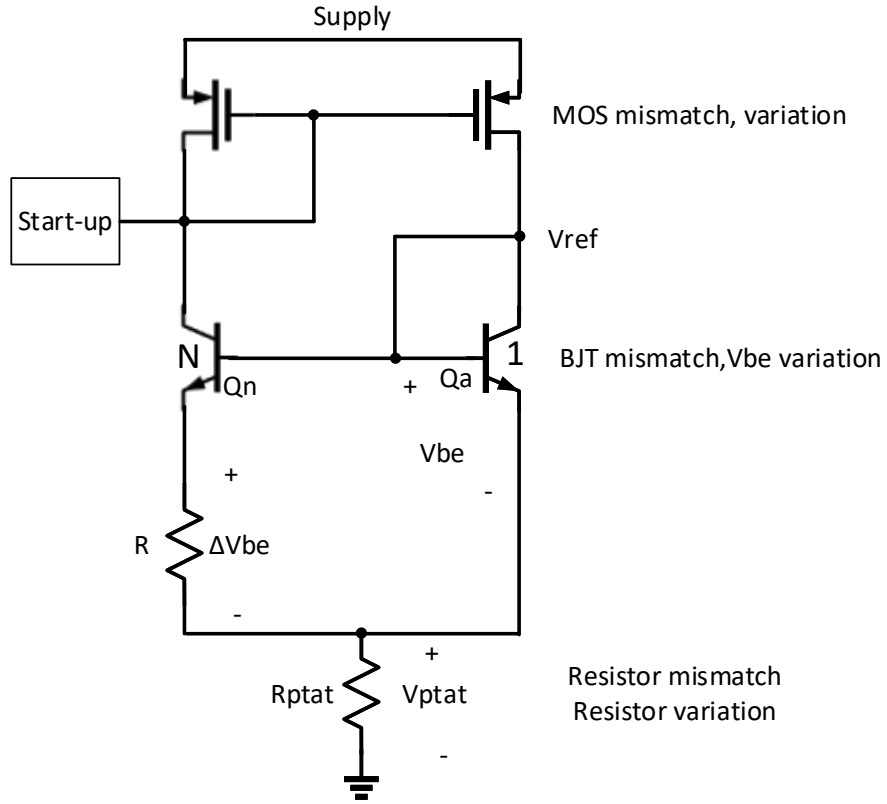


Figure 1.14: Process error sources in Brokaw cell [23] [38].

The Brokaw cell output voltage is given by Eq. (1.48), which was derived earlier in this chapter.

$$V_{ref} = V_{bea} + 2 \cdot I_{ptat} \cdot R_{ptat} = V_{bea} + 2 \cdot \left(\frac{kT}{q} \right) \frac{\ln(N)}{R} \cdot R_{ptat} \quad (1.48)$$

Due to variation in the process, the resulting difference in the reference voltage is given by Eq. (1.49) [38].

$$\Delta V_{ref} = \Delta V_{bea} + 2 \cdot \Delta I_{ptat} \cdot R_{ptat} \quad (1.49)$$

We will now investigate the sources individually as applied to Fig. 1.14. MOS device mismatch (PMOS mirror devices) and variation are one of the sources of error which leads to a deviation in the desired current mirror ratio biasing the BJT (Q_a and Q_n). It can be due to:

1. Dimension (W/L) mismatch
2. Threshold voltage (V_{th}).

It is shown in [38] that a mismatch factor of δm in the current mirroring leads to an overall error of:

$$\Delta V_{ref} = \frac{k \cdot T}{q} \times \frac{R_{ptat}}{R} (2 + \ln(N)) \times \delta m \quad (1.50)$$

For a 3σ variation of 2%, it results in variation of ± 24 mV for a 1.2 V reference, which is large. Techniques such as increasing area (WL) [39] and operating the devices with large overdrive ($V_{gs} - V_{th}$) are required to mitigate this effect. Both of this requires a large area or in other words, high parasitic capacitance, thus limiting the dynamic performance of the circuit (such as bandwidth of the circuit which affects PSRR and load regulation). Besides, it becomes more challenging at lower supply voltages, since the available headroom (V_{ds}) is limited, therefore the overdrive magnitude of the mirror devices is constrained.

Resistor mismatch is another contributor to the overall error of reference. Typically, the gain of the PTAT voltage is scaled using a ratio of resistors to match the ‘*temp-co*’ of the CTAT voltage. For a δR mismatch in resistor results in an error in reference voltage as below:

$$\Delta V_{ref} = V_{PTAT} \cdot \delta R \quad (1.51)$$

Judicious layout and using techniques such as common centroid and inter-digitation helps average errors across the silicon, thus leading to better matching. For example, a 0.5% mismatch in resistors result in approximately 3 mV error in 1.2 V reference or about 0.25% with respect to absolute reference voltage [38]. A more serious impact is due to the process variation which can be anywhere between 10–20%. In the Brokaw cell, this results in the variation of CTAT component since the PTAT generation involves the absolute value of resistors. This can be improved by using a material which has lower spread, for example, polysilicon resistors exhibit low variation across temperature and process compared to n-well resistors. Typically, design architectures (discussed later) where both CTAT and PTAT components are summed in the current domain across a load resistor shows immunity to process variation (Δ) since the resistor process variation term gets canceled for each current

component as shown by Eq. (1.52)

$$V_{ref} = \left(\frac{V_{be}}{R_1(1 + \Delta)} + \frac{\Delta V_{be}}{R_2(1 + \Delta)} \right) R_3(1 + \Delta) \quad (1.52)$$

Another key component is the BJT mismatch and variation. The BJT mismatch results in an unequal ratio of emitter area which results in an error in the PTAT voltage generated. This can be made minimal by using a larger number of unit BJT structures to form a single cell of the ratioed structure. BJT process variation has two effects, namely, the region of biasing of the BJT changes, which translates to a non-flat ideality factor (discussed more in detail in Chapter 2). It also results in a variation of V_{be} which can be a large source of error as it directly contributes to the output reference voltage. Substrate PNP available in CMOS process offer lower variation of V_{be} than the NPN variants which can be 3–6 $\times$ worse. The reason for this is that the base width of PNP is larger, which spatially averages the dopant variations, thus leading to a more uniform base-doping profile and a constant saturation current density [38]. The drawback of PNP device is that the ratio of collector currents (used to generate the ΔV_{be}) is not well controlled when the β is low for the device.

1.4 Trimming Techniques for Bandgap References

The bandgap reference is constituted of the PTAT and CTAT components. Due to the process variations, the mismatch offset affects devices across the wafer lots differently, hence every voltage reference output is unique. In order to improve the yield and ensure a predictable output voltage, typically for high precision references, the output voltage is trimmed (changed or tweaked) post fabrication to a “*golden*” value which has the least temperature drift across the entire temperature range. This process is known as trimming of bandgap reference.

Fig. 1.15 shows a conventional bandgap reference architecture. The OTA ensures that nodes V_x and V_y are equal and, as a result, M_1 and M_2 carry the PTAT current. The output of such a bandgap is given by Eq. (1.54). It should be noted that although both terminals V_{ref} and V_z are identical in terms of the output voltage magnitude, typically the output is

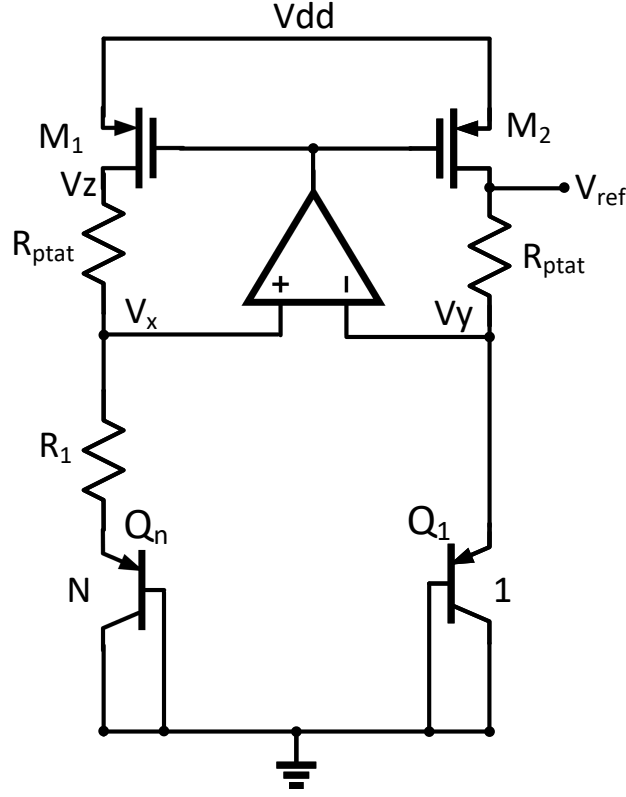


Figure 1.15: Conventional bandgap reference.

driven by V_{ref} node. This is because the OTA, together with M_1 , forms a positive feedback loop. Therefore, loading the node V_{ref} will ensure that, at higher frequencies, the positive feedback loop magnitude rolls off quicker than the negative-feedback loop (formed by OTA together with M_2) [40].

$$V_{ref} = \frac{\Delta V_{eb}}{R_1} \cdot R_{ptat} + V_{eb} \quad (1.53)$$

Considering the offset due to mismatch, the induced offset (V_{os}) at the input of the OTA as well as any mismatch in the BJT and MOS current mirror (M_{os}) results in an output voltage which is "shifted" with respect to the target "golden" value post-fabrication, which can be given by eqn. M_{os} is a fraction less than 1 and is lumped

$$V_{ref} = \frac{\Delta V_{eb} + V_{os}}{R_1} \cdot R_{ptat}(1 + M_{os}) + V_{eb} \quad (1.54)$$

The PTAT component, which is a linearly varying quantity with respect to absolute temperature (in comparison to the CTAT component V_{eb} which has additional non-linearity) is typically used to correct for the change. In Fig. 1.15, the PTAT component can be corrected by changing the value of resistor R_{ptat} . Alternatively, changing M_2 to change the mirror factor and hence the PTAT current contribution cannot be applied in this architecture (especially in deep nanoscale process) since the bias current density for the two BJT (Q_1 , Q_N) is not identical which results in different V_{eb} .

The resistor (R_{ptat}) can be varied by two different methods [38]. Firstly, a digital bus, which controls ON and OFF switches, is used to close/short or open part of the resistor ladder can be employed. The accuracy of this correction is limited by the step size (or the least resistor unit). Therefore, a higher resolution will invariably translate to a large number of steps for a given LSB and cover a dynamic range (given by the guard band together with the untrimmed spread of the bandgap). Another method is laser trimming (which resizes the resistor) is more accurate and area efficient, hence finds application in high-precision data converter applications. The drawback of this method is the inherent cost involved in the test process as well as the equipment cost.

Typically, many of the error sources in the bandgap (Table 1.1) have a linear temperature dependence (PTAT) and hence can be corrected by trimming at one temperature, which is usually room temperature. Higher order errors such as the mismatch of MOS devices (offset of OTA and current mirror devices M_1 , M_2 in Fig. 1.15) are not compensated by trimming, but their absolute value at the trim-temperature is reduced. Therefore such errors can be corrected by trimming at multiple temperatures. For a single temperature trim, the trimming is done at the wafer scale and subsequently packaged. Any stress related to the package [41], [42] on the circuit is not corrected and will add to the error budget. One way to mitigate this is to have EEPROM bits to correct for post-package shift for every device, which increases the manufacturing cost. Alternatively low-stress mechanically compliant layers are added in the packaging process before encapsulating with plastic, which again increases the associated cost [42].

In some target applications, cost is a major factor and hence time required for trimming for the industrial part might not be viable. Alternative design techniques can be employed

to reduce the effect of mismatch. One popular method is to employ a dynamic correction technique such as dynamic element matching (DEM) to correct for the mismatch. DEM employs all different combinations of unit elements which form the desired ratio. Due to this periodic rotation, the mismatch information, which is contained in low-frequency, is up-converted to a higher frequency (given by the rate at which one full rotation of each unit element is completed). Thus, the subsequent low-pass filtering of this signal helps to reduce the effect of mismatch.

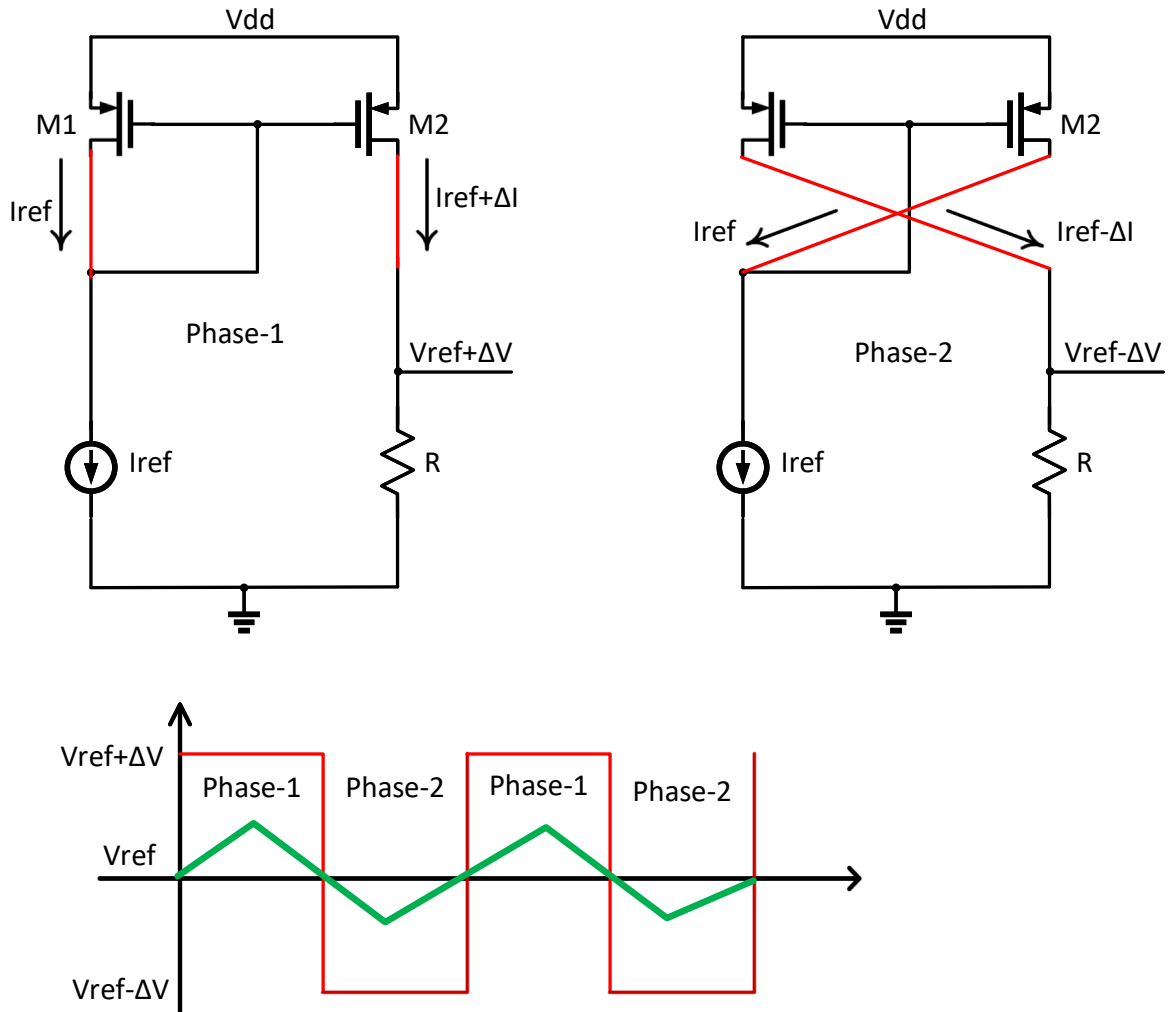


Figure 1.16: DEM to reduce mismatch and offset errors

A simple example of DEM where two elements which have a mismatch are nominally averaged by switching their contribution to the output in alternative phases is shown in Fig.

1.16. It shows a simple current mirror formed by devices M_1 , M_2 . In normal operation, due to the mismatch between M_1 , M_2 results in an output of $V_{ref} + \Delta V$. Chopping implementation for this circuit involves two pairs of switches which are swapped between two phases.

In phase-1, M_1 is diode-configured and mirrors I_{ref} to the output, but due to mismatch in M_2 ; the resulting output current is $I_{ref} + \Delta I$.

In phase-2, M_2 is diode-configured and mirrors I_{ref} , but due to the mismatch; the resulting current to output is reduced to $I_{ref} - \Delta I$.

Thus, by dynamically changing between phase-1 and phase-2, the output varies between $V_{ref} + \Delta V$ and $V_{ref} - \Delta V$, as shown by the red waveform in Fig. 1.16.

In order to remove this resulting AC signal, a low pass filter (LPF) is used subsequently to attenuate the error, thus resulting in the green waveform. Typically, DEM is done at low frequency (kHz) to minimize charge injection and clock feedthrough. This translates to LPF requirement of a low-frequency pole. The magnitude of the final noise depends on the size of the capacitor used in the low-pass filter (in order of 10-100s of pF [43]). Although a large capacitor is beneficial for filtering, it results in increased area consumption as well as limits the bandwidth of the circuit, thus degrading the transient response for any load or line changes.

1.5 Start-up Circuit for Bandgap References

Bandgap reference circuits are formed based on self-biased feedback loops. Typically, these loops have two or more stable points at which the circuit can be operational. One of these stable points is when there is no current in the loop, which is the unpowered state. Therefore, the start-up circuit is an important block accompanying a bandgap reference.

Bandgap references are key source of voltage to several other circuits across the chip and hence it is critical that they power up to the desired state of operation. In an SoC targeting power constrained applications, such as IoT sensor nodes, there are several sleep modes where the entire system consumes low current in the order of μA . This translates to start-up circuit's current budget to be minimal [44]. The impact of such system level power budgeting is that the start-up circuit becomes more sensitive to leakage currents such

as leakage of the junction capacitor or gate leakage in nano-scale processes. This leakage may be sufficient to prevent start-up [45] from functioning leading to a failure of the voltage reference. Besides, care must also be taken in both design and layout, to ensure there is no coupling or disturbance to these critical start-up blocks in a large SoC environment.

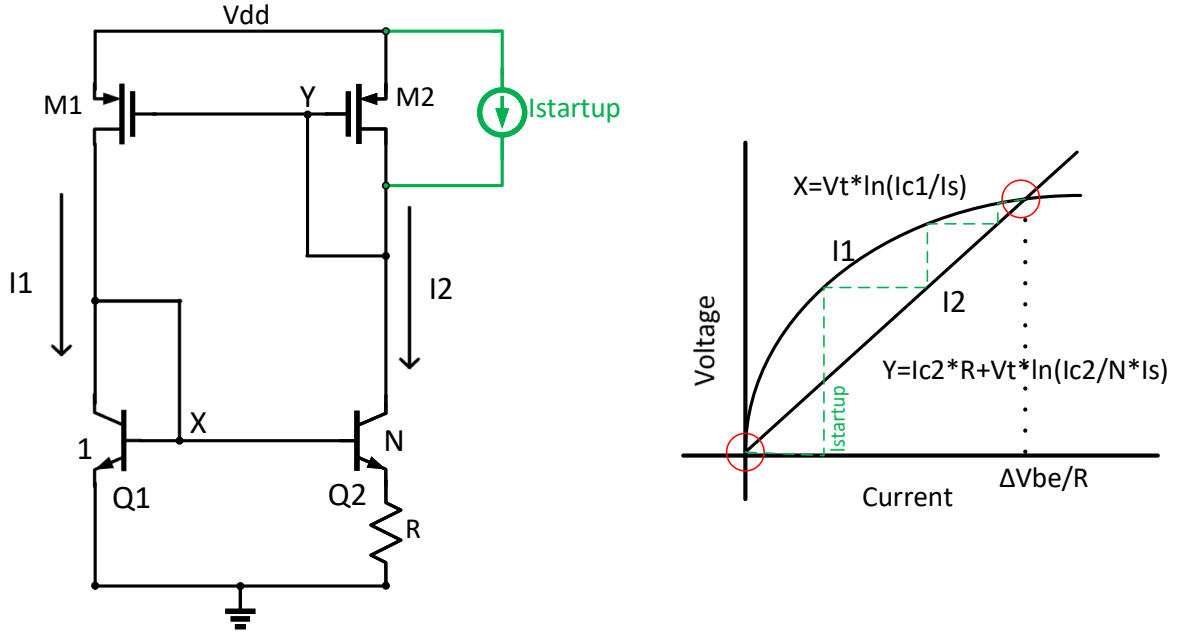


Figure 1.17: Start-up behaviour of PTAT cell [44].

Fig. 1.17 shows a conventional PTAT generator based on the NPN BJT devices together with resistor R . The circuit has two stable conditions shown in the waveform (Fig. 1.17) by red circles:

1. Zero current state ($I_1 = I_2 = 0$),
2. Actual desired current ($I_1 = I_2 = \frac{\Delta V_{be}}{R}$).

One possible method to move the circuit out of the “zero current” state is to inject a small current ($I_{startup}$) into the loop and subsequently let the loop regenerate to move towards the “desired” current state. When such *desired* state is reached, the extra injection current should be turned OFF as the circuit has reached the *correct* operation.

Since the start-up is obtained by the extra injection current, it should be noted that relying on some sort of leakage current is not a robust method of start-up. This is because:

- 1) the transistor leakage current simulation model can be incorrect, 2) at cold temperatures,

where the leakage current is small, the circuit can take a very long time to start-up, 3) in extreme cases the leakage current may not be sufficient for regeneration to occur. It should also be noted that any open-loop time-dependent current injection can always fail. Since there is a dependency on the ramp rate of the supply and can be shown to fail for slow rates [44]. But these time-dependent start-up circuits could well be used in cases where the supply rate is well defined as a use case for the chip to function. A robust start-up circuit should not depend on any predefined conditions or on leakage currents and be able to bring the circuit to a desired state whenever the reference suddenly is largely disturbed, for example due to coupling or external/internal noise.

1.6 BJT Device-Based Circuits

In the previous sections, we saw that BJT forms the core of the bandgap reference circuit. While the voltage in reference is independent of temperature, another key aspect is to exploit the temperature dependence of the voltage constituents (PTAT or CTAT) to determine an on-chip temperature. Fig. 1.18 shows a simple architecture of a temperature sensor based on the PTAT characteristic of ΔV_{be} . The digital code produced by the back-end ADC gives representation of the sensed absolute on-chip temperature.

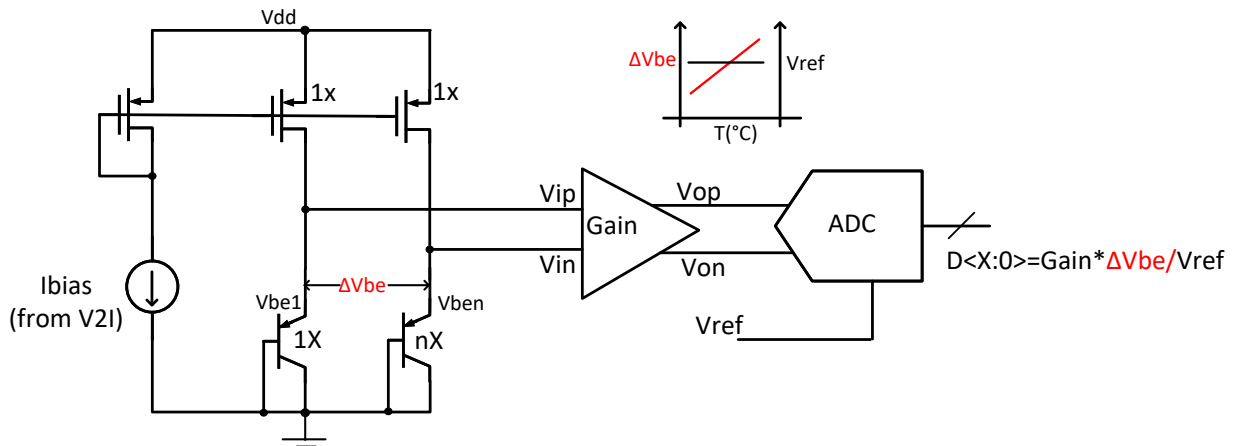


Figure 1.18: BJT-based temperature sensor [46]

This is useful in many system-on-chip applications where a temperature sensor or a distributed set of such sensors can help in determining accurately the temperature for the

system level functions, such as reliability, functional safety, compensation of circuit blocks for optimum performance, etc. This section explains its importance and hence the motivation for developing a good device model of BJT to enable the implementation of precision circuits based on such devices.

Temperature is one of the key parameters affecting the performance of integrated circuits. Measuring the temperature on-chip is important to prevent overheating and understand thermal gradients, which subsequently can be used to regulate the system performance. Besides, thermal management is a key requirement for ensuring functional safety in some key applications, such as automotive, communications.

Thermal issues are responsible for more than 50% of all integrated circuit failures [47]. Technology scaling coupled with system integration have led to higher power density leading to hot spots across the chip. This places strong constraints on thermal reliability. Recent examples are that of integration of high-speed GHz data converters within FPGA or the move to 112 Gbps SerDes transceivers. This has increasingly necessitated the need for distributed on-chip temperature sensors for thermal and power management in today's FPGA and microprocessors. Moreover, since the temperature is directly related to the activity in the circuit blocks and is dynamic in nature, it becomes key to have enough sensors distributed to detect different hot spots. Temperature estimates above or below the actual temperature will result in late or early activation of thermal management. While late estimation results in degradation of reliability due to the resulting temperature being higher than the threshold, early estimation can have a penalty on the performance [47].

There have been several attempts in the literature to use structures in CMOS to realize the temperature-sensing element. Ref. [48] uses a dynamic threshold MOSFET to measure temperature, [49] uses an on-chip resistor, while [50] uses temperature dependence of a delay cell in ring-oscillator to measure temperature. Another phenomenon used to measure temperature is that of thermal diffusivity in silicon [51]. However, BJT based temperature sensors appear to be the choice, even in deep nanoscale process, for high volume manufacturing [19], [52] owing to its established physical phenomenon which is less sensitive to process spread as well as through the product life-cycle ageing compared to others. Recent implementations of BJT based circuits in FinFET technology show that their performance has degraded. One

of the key components contributing to this is the challenge of realizing BJT in FinFET process [15]. Chapter 2 discusses the substrate PNP BJT used in this design

1.7 State-of-the-Art Voltage References

Voltage references are widely used circuits and have been studied for a very long time. There has been many published works in the area and a selection of the State-of-the-Art performing bandgap references from published sources has been presented in Table 1.2.

One of the most widely cited and used architecture is the Banba's bandgap reference [32]. It is because of a few attractive aspects of the architecture, namely, because it proposed a current domain summation of the PTAT and CTAT components, besides these components were generated by a single negative feedback loop. This resulted in a low-voltage and low-power bandgap reference. Without trimming and second-order curvature correction, the circuit achieved $\pm 2.9\%$ inaccuracy across a temperature range of 27°C to 125°C . Another alternative to overcome the headroom requirement of the BJT diodes was to employ MOS (in sub-threshold region), thus requiring lower supply voltage. This approach was presented in [53] and showed that such a reference requires supply voltage of only 1.2 V. It achieved a reasonable inaccuracy of $\pm 3.33\%$ across a temperature range of -25°C to 125°C and also had a disadvantage of limited cold ($>25^\circ\text{C}$) operating temperature region. The temperature non-linearities of MOS (in sub-threshold) based bandgap are stronger than those of BJTs and CMOS in strong inversion, hence it limits the '*temp-co*' performance. Moreover, it is not widely adopted in industry due to the lack of supporting information on characterization across different wafers.

In order to achieve high precision reference, trimming at one temperature together with a higher order curvature correction was employed in [5]. This architecture achieved a very good performance of $\pm 0.15\%$ inaccuracy across a temperature range of -40°C to 125°C as well as a max '*temp-co*' of 12 ppm/ $^\circ\text{C}$. Another work based on a current domain summation and used BJT based curvature compensation scheme was by Charalambos [6] and achieved excellent performance. An alternative technique to BJT based curvature compensation is using piecewise linear correction of higher order curvature proposed in [4]. This work achieved

low power as well as good precision ($\pm 0.34\%$ across a temperature range of -50°C to 150°C). Meanwhile, research was done on achieving low supply voltage operation while using BJT devices. Some of the work [37] employed charge pump thus enabling supply voltage down to 0.5 V . Alternatively, [36] proposed a reverse bandgap concept together with switched-capacitor operation. This work required only 0.75 V supply and employed both trimming and higher order correction. It achieved a ‘*temp-co*’ of $40\text{ ppm}/^{\circ}\text{C}$. Fuel gauge monitoring, which involves measuring current and voltage, is a very important application and demands strict accuracy on the reference used in the system. Targeting such an application, [54] used digital assistance to improve the bandgap performance along with a chopped OTA for input offset error correction. The core non-PTAT errors were removed by chopping while all other errors which are PTAT removed by a single temperature trim. The digital assistance proposed by [54] is to remove remnant errors by using a temperature sensor, stress sensor and a lookup table. It also included curvature correction and achieved a good ‘*temp-co*’ of $7\text{ ppm}/^{\circ}\text{C}$.

The subsequent research works show that in spite of the challenges posed by BJT realization in nanometer CMOS, the references still achieve good accuracy. An implementation [55] of a first-order compensated reference in 16 nm FinFET process achieved an inaccuracy of 0.64% across a temperature range of -45°C to 125°C with minimum ‘*temp-co*’ of $9\text{ ppm}/^{\circ}\text{C}$. It was based on Banba [32] architecture shown in Fig. 1.9.

reference	Technology	Supply voltage(V)	Temperature Range (°C)	Power (uW)	Temperature Co-efficient (ppm/°C)	Accuracy(%)	Trimming	Higher-order correction
Banba et al. JSSC'99 [26]	0.4 μ m	2.1	27 to 125	13.6	116	2.9	No	No
Giustolisi et al. JSSC'03 [53]	1.2 μ m	1.2	-25 to 125	3.6	119	3.33	No	No
Ge et al. JSSC'11 [5]	0.16 μ m	1.62	-40 to 125	99	5-12	0.15	Yes (1-point)	Yes (subtraction of two Vbe)
Ivanov et al. JSSC'12 [36]		0.75	-20 to 85	0.17	40	-	Yes	Yes (using poly res)
Sano et al. VLSI'12 [4]	0.13 μ m	0.9	-50 to 150	3.51	30	0.34	Yes	Yes
Charalambos et al. JSSC'12 [6]	0.35 μ m	2.5	-50 to 150	95	13.7		Yes	Yes
Osaki et al. JSSC'13 [56]	0.18 μ m	0.7	-40 to 120	0.0525	114	1.05	No	Yes (using PTAT)
Ma et al. '14 [57]	0.18 μ m	1.2	-40 to 120	43.2	3.4	-	Yes	Yes (using MOS)
Duan et al. TCASII'15 [58]	0.13 μ m	1.2	-40 to 120	144	4.2	1.7	No	Yes (PNP against NPN)
Shrivastava et al. JSSCC'15 [37]	0.13 μ m	0.5	0 to 80	0.032	75	2	Yes	No
Maderbacher et al. ISSCC'15 [54]	0.13 μ m	-	-40 to 120	-	7	0.08	Yes	Yes
Chang et al. ASSCC'16 [55]	16nm FinFET	1.62	-45 to 125	-	9-33	0.64	No	No
Wadhwa et al. VLSID'17 [59]	16nm FinFET	1.62	-40 to 125	340	-	1.3	No	No
Chen et al. ISSCC'19 [60]	12nm FinFET	0.7	-20 to 125	6.88	40.51	2.35	No	No

Table 1.2: State-of-the-art voltage references

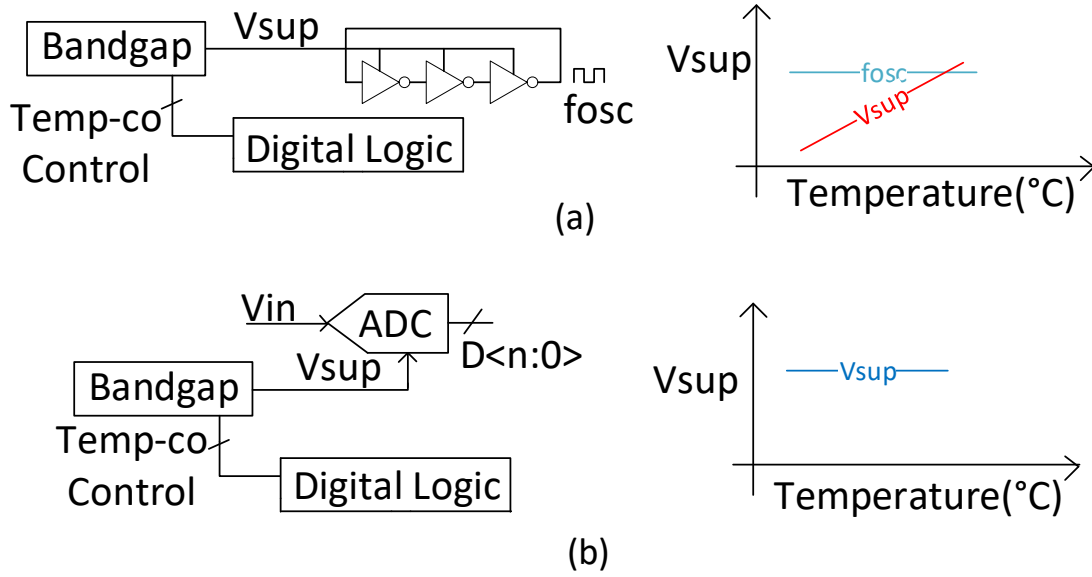


Figure 1.19: Concept of programmable temperature co-efficient of voltage reference.

1.8 Motivation for Programmable Temperature Coefficient of Voltage Reference

Temperature is one of the main environmental parameters which affects the analog and mixed-signal circuit performance. This sensitivity is usually minimized by using auxiliary circuit blocks that sense the temperature for feedback or by using various compensation loops and calibration techniques. An alternative solution, preferred in this work, is to make the reference voltage for the analog system to counteract the temperature change directly. For example, in ring oscillators, the temperature sensitivity of the resonating frequency f_{osc} can be reduced by making the oscillator supply to track the temperature.

Fig. 1.19(a) shows the context within an FPGA or SoC, where a bandgap reference is shown to generate and buffer the supply voltage (V_{sup}) for a ring oscillator. The digital logic within the FPGA/SoC can be used to control the “temp-co” of the voltage reference, thus compensating for the temperature dependency. In some applications, however, a flat ‘temp-co’ of the supplied voltage might be preferred, as in the case of an A/D converter shown in Fig. 1.19(b).

Fig. 1.19(a) further illustrates the concept in terms of curves where the reference voltage

$V_{sup} = V_{ref}$ shows a positive ‘*temp-co*’ thus stabilizing the ring oscillator frequency f_{osc} which is thus constant across temperature. This motivates the design of reference circuits capable of generating a voltage with both zero and programmable non-zero ‘*temp-co*’s’. Such an approach has previously been used in discrete components for a variety of applications [61]. Besides, the adjustable ‘*temp-co*’ of voltage reference appears mandatory in face of strong thermal gradients (‘local hot spots’) observed in large FPGAs due to their dynamic switching activity, which will get only worse in advanced process nodes. Thus, ‘*temp-co*’ programmability and accuracy are prioritized over area and power, in the context of voltage references targetted for integration into large FPGAs.

1.9 Thesis Objective

In this thesis, we present a voltage reference implemented in a 7-nm FinFET technology that addresses both high precision and ‘*temp-co*’ programmability. Two curvature correction methods, together with the proposed digitally assisted trimming techniques, are implemented to achieve good accuracy and temperature stability. The design is intended for integration in an FPGA, which means that the reference circuit’s power and area budgets are fairly relaxed compared to the full-chip power and area. This work provides details about the BJT device structure in FinFET as well as device-circuit co-optimization details and proposes a digitally assisted trimming technique. In Chapter 2, we discuss the technology aspects of bipolar junction transistors (BJT). Chapter 3 describes the bandgap architecture, circuit details, and proposed trimming techniques. Chapter 4 presents conclusion. Finally, comparison with the latest published results shows that the presented design compares favourably with state-of-the-art. To the best of our knowledge, this is the first 1 V precision voltage reference in 7-nm FinFET technology as well as which presents the characterization BJT model parameters useful for the design of precision references and temperature sensors in FinFET technology.

CHAPTER

2

BJT Realization in 7-nm FinFET Technology

2.1 Motivation

As discussed in Chapter 1, the main device enabling the CMOS voltage reference and temperature sensing is a bipolar junction transistor (BJT) [62]. As demonstrated earlier, there have been explorations in literature of alternative devices [51] [11], but BJT continues to be the core device used in scaled CMOS technology by industry for implementing reference and temperature sensors [19] [55]. Moreover, the BJTs are also useful for chemical and biological sensing, as reported by [63], where the BJT's base is connected to a surface which is in contact with the solution to be sensed. Understanding the device models and their usage is key to achieving high performance of these circuits.

An accurate SPICE modeling of BJTs in scaled processes is challenging and usually requires many iterations of test chips to derive stable and robust models. Therefore, the design of such circuits requires both device modeling and interaction with circuit design to achieve the “first-time right silicon”. Unfortunately, there is scant literature available which

discusses the characterization of BJTs and their mismatch in scaled CMOS technologies. The key parameters of BJT devices in 7-nm FinFET, which are of relevance for the application circuits, will be presented in this chapter. It also shows their trend compared to the scaled planar CMOS vs. the FinFET process. In Section 2.2, we present the device structure and process technology steps involved to realize the BJT in the FinFET process. We also present a layout view of such a structure. Section 2.3 discusses the parameters of interest of BJT for the implementation of two commonly used circuits, namely, the bandgap voltage reference and temperature sensor.

Vertical fin-shaped field-effect transistor (FinFET) has emerged as a strong contender to the planar MOS technology for sub 28-nm nodes. The economic (area scaling) as well as performance (higher speed) benefits due to the adoption of FinFETs is evident for FPGAs and large SoCs as seen by the trends in the industry. As the process technology shrinks, it becomes difficult to ensure the transistors have a good gain as well as a high ratio of switch-ON vs. switch-OFF current. This scaling trend has been followed with planar devices until the 28-nm node. The planar process scaling has not typically provided proportional performance improvements since the gate length has not shrunk proportionally. Instead, the performance has been improved by various device boosters [3], such as: 1) higher mobility of strained channel region, 2) high-k dielectric provides higher oxide capacitance. This has led the industry, at around the 16-nm CMOS node, to move to the FinFET devices, in which the gate covers the channel along the vertical dimension, thus having a better control of the channel current [3]. A single MOS transistor usually has a limited number of fins dictated by the maximum poly density; any further increase is obtained by putting multiple devices in parallel. In order to increase the output resistance as well as for improved matching, a large device length is required. This is realized in FinFET process by stacking of multiple devices. Methods, such as stacked gates for uniform gate density, metal colouring for matching, and parameterized cell (PCell) automation, are examples of the methodologies we have employed to implement precision analog layout in 7-nm CMOS. Besides, since the device models, especially for the BJT, were fairly immature at the time of design, care was taken to ensure the circuit architecture can absorb uncertainty in these models in addition to implementing custom test chips for device characterization and in-house Simulation Program for Integrated

Circuits Emphasis (SPICE) model development. We achieve this by adding design margins, for example, in: 1) matching of current mirrors, 2) amplifier offset and noise, 3) Extended trim capabilities.

In fine geometry technology, the beta factor (current-gain) of the BJT is very low and the process variation is observed to be larger [15]. Section 2.2 discusses the details of the BJT performance in FinFET. Indeed, recent voltage references [55] implemented in sub-16-nm show worse precision than before. PNP BJTs have been used traditionally for temperature sensor design in CMOS. This is mainly due to the fact that long-term drift of temperature sensors and bandgap references caused by package-induced stress is lower with PNP BJTs than with NPN BJTs [41]. Therefore, this paper mainly targets the PNP BJT devices.

2.2 Process Technology Steps

The BJT devices in this work exploit the existing foundry technology developed for advanced FinFETs. The PNP BJT is a parasitic vertical PNP transistor that shares the same process steps as with PMOS. Our estimated process flow lists the major FEOL steps in Fig. 2.1, followed by HKMG, MEOL, and BEOL process steps to complete the BJT device [15].

- **Fin Patterning & STI**

- **NW Implant**

- **Poly Gate Patterning**

- **PLDD Implant**

- **S/D Etch and eSiGe Growth**

- **S/D P+ Implant**

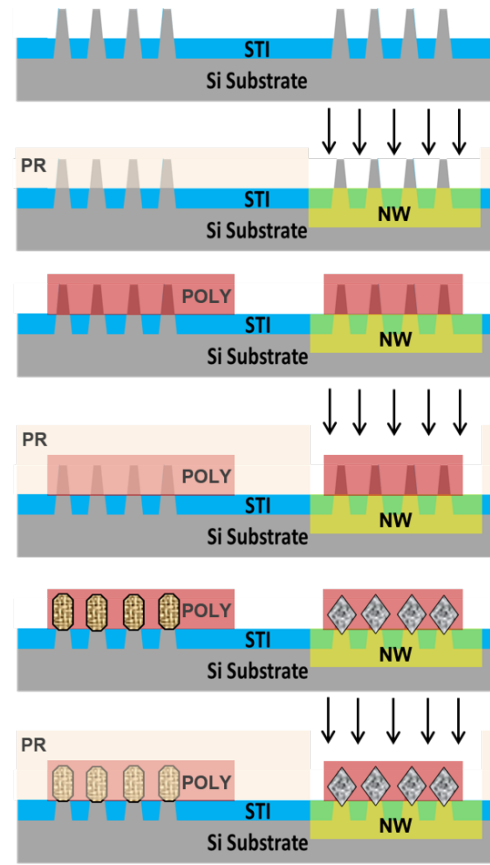


Figure 2.1: Estimated FinFET processing steps for creating a parasitic BJT device (excluding HKMG, MEOL, BEOL).

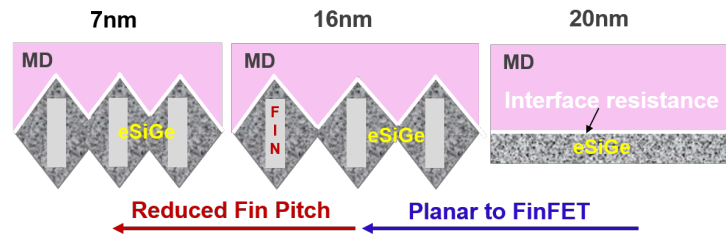


Figure 2.2: BJT emitter profile.

The emitter profile of such a device is shown in Fig. 2.2 which shows the appearance of a diamond shape of the emitter profile moving to FinFET process from planar. The diamond shape is due to the epitaxial Silicon Germanium (eSiGe) layer, one of the strained technology choices used to improve PMOS mobility. It has been widely used for process technology since the 45-nm node. The reason for the diamond shape is due the silicon orientation on which eSiGe is grown. The 3D view of the constructed BJT and the corresponding illustrated

proposed layout cell is shown in Fig. 2.3. The emitter still shows a diamond shape at the channel but has a flat shape at the interface with the MEOL contacts. For FinFET, each fin is a silicon seed where the embedded silicon germanium (eSiGe) grows into a diamond shape.

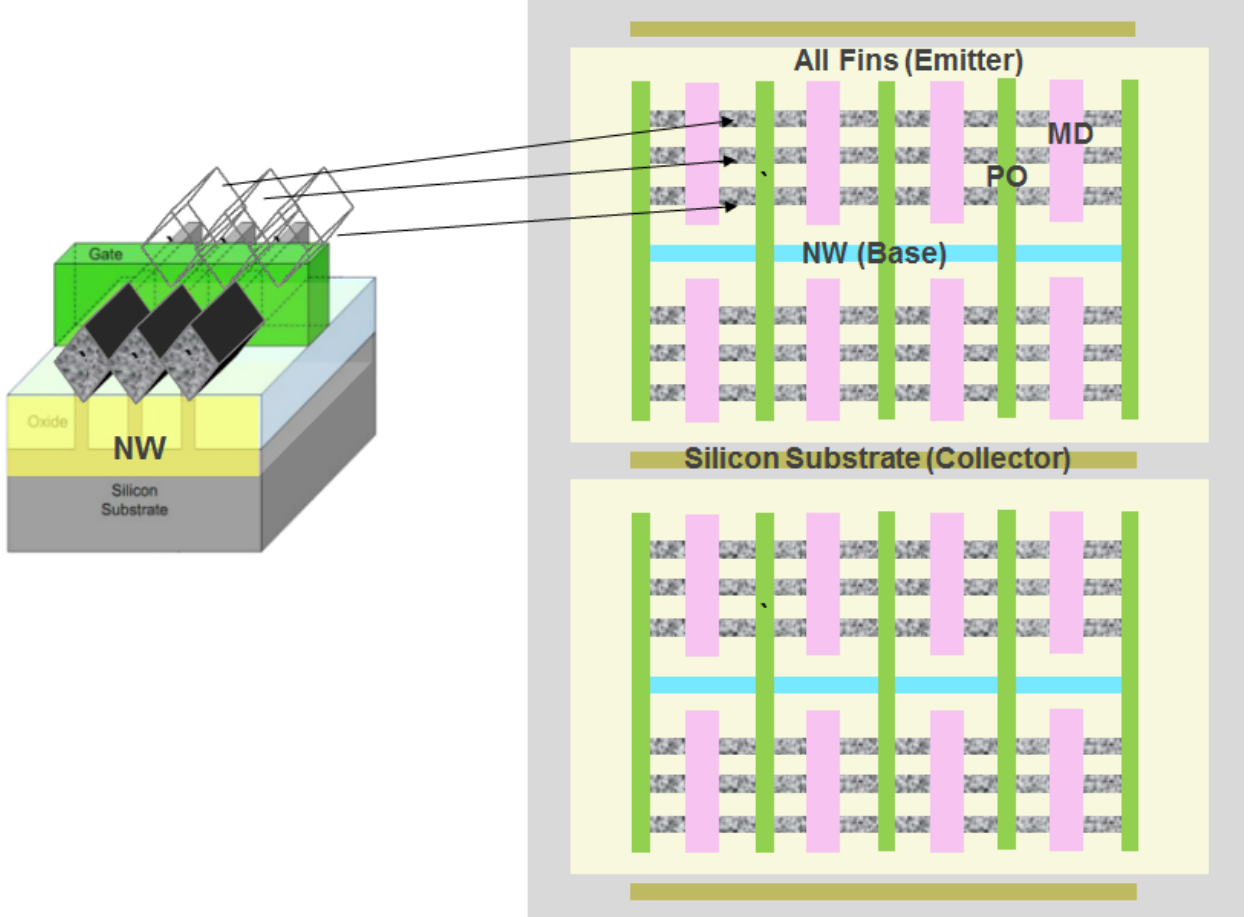


Figure 2.3: (a) [Left] 3D view of FinFET BJT. (b) [Right] Proposed merged BJT layout. (for illustration only, modified from semiwiki.com).

The FinFET technology facilitates a gated BJT layout, as shown in Fig. 2.3, with an extra poly on top of the emitters but tied to the base, which is different from that in planar BJTs. Compared to the foundry's FinFET BJT array, the proposed merged layout used in our design structure can reduce the cell area by 20%.

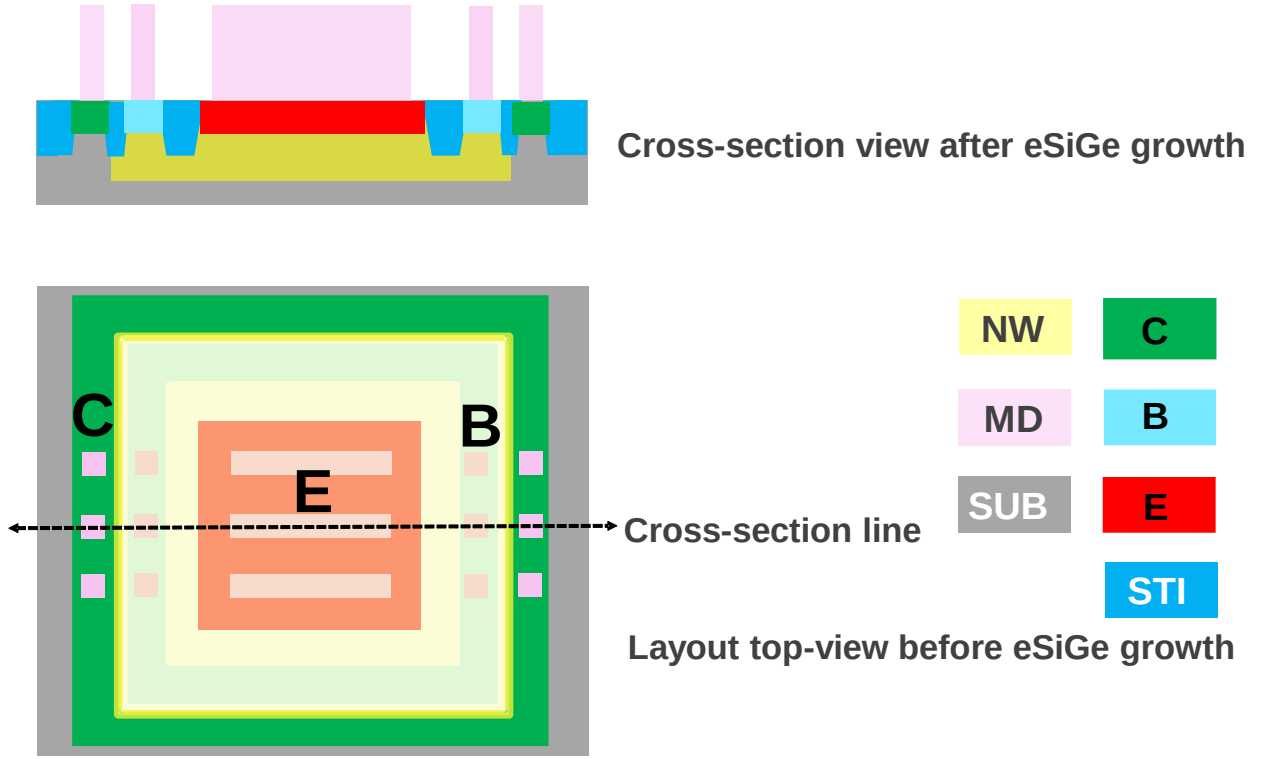


Figure 2.4: BJT device in planar CMOS process.

Cross-sections of BJT implementation in planar and FinFET process technologies are shown in Figs. 2.4 and 2.5. The latter is a custom layout used in our implementation. In these structures:

M_d = contact to the source drain diffusion,

PO = polysilicon,

SUB = substrate,

E = emitter of the BJT device,

B = base of the BJT device,

C = collector of the BJT device.

In Fig. 2.5, the vertical cross-section of the emitter then takes the shape of a diamond. This is due to the use of an eSiGe layer, which is one of the strained technology choices used to improve the mobility of PMOS devices [3].

Instead of directly using a foundry's BJT parameterized cell (PCell) to form a BJT array, we modify and merge the collectors by removing and customizing dummy patterns inside the

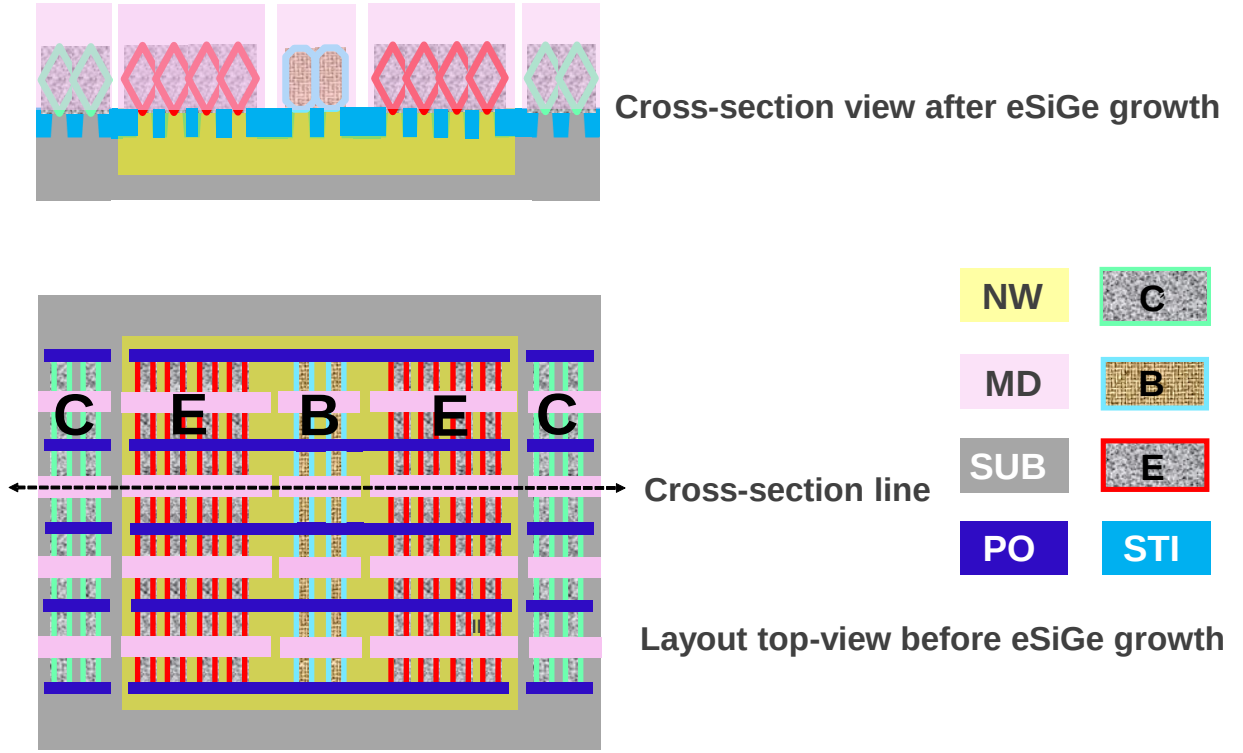


Figure 2.5: BJT device in FinFET process.

BJT PCell. This was motivated to provide a compact cell structure (for routing) which is also area efficient. Effectively, 20% area reduction of the layout is achieved compared to the foundry's PCell array for the same emitter area.

2.3 BJT Device Characterization

BJT is a parasitic device typically usually operated with its collector tied to the base. This work required extensive characterization of the BJT in order to develop accurate SPICE models to enable precision bandgap reference as well as temperature sensor design. Such a BJT sees disadvantages given by: 1) large non-ideality factor changes from a gated diode, 2) more process corner spread of the non-ideality factor, 3) worst ΔV_{eb} variability for a 1:N BJT pair caused by the emitter fin width/eSiGe control, 4) higher ON-resistance from decreasing the fin pitch and diamond shape epi profile dependence (Fig. 2.2). Compared to the conventional BJT structure, other BJT device options in the FinFET technology, such as NPN, PWell/DeepNWell/Psub, have been explored but found to be of no benefit to the

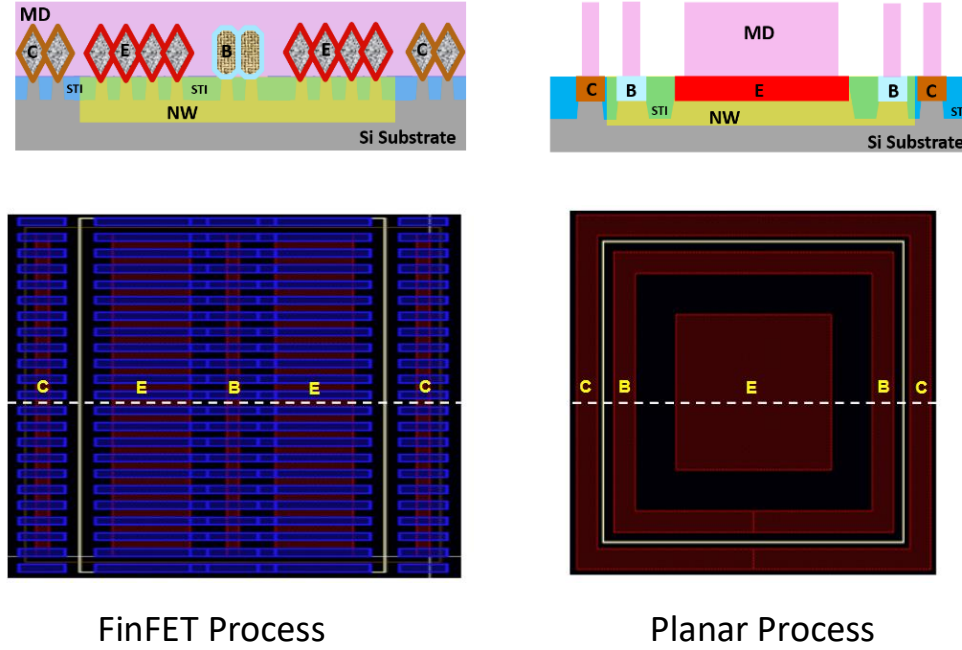


Figure 2.6: BJT device in FinFET and planar CMOS process: (top) cross-section, (bottom) top-view. targeted applications [15].

Characterization of devices to match the actual use case condition is crucial to develop an accurate model to be used in design. One of the SPICE model parameters useful for design is data useful for Monte Carlo or sensitivity analysis. Conventional BJT mismatch models are based on SPICE Gummel-Poon (SGP) model [62]. Mismatch data for I_c and $\beta = \frac{I_c}{I_b}$ is used to fit the variance given by Eq. (2.1) [15]

$$\sigma_{I_{cMM}\beta_{MM}}^2 = \frac{b_1^2}{W_e L_e} + \frac{b_2^2}{W_e^2} + \frac{b_3^2}{L_e^2} + b_4^2 s^2 \quad (2.1)$$

Section 2.4 presents the device characterization results, which shows that there is an inverse dependence of mismatch variance on I_c as well as the inverse relationship on area $\sqrt{W \cdot L}$ which is not uniform at all lengths.

This work required an extensive characterization of the BJT in order to develop accurate SPICE models. The parasitic BJT normally operates with its collector tied to the base. In this work, as shown in Fig. 2.5, a so-called gated diode is used, in which a polysilicon layer (PO) is placed on top of the fins, making the resulting device look more like a normal MOSFET in compliance with Design Rule Checking (DRC) rules. The source/drain is used

for the diode-connected BJT operation. However, the presence of the PO gate negatively impacts the BJT's performance, resulting in more leakage and a larger non-ideality factor η .

Other disadvantages are: 1) More process corner spread of η , 2) Worse ΔV_{eb} variability for a 1: N BJT pair caused by the emitter fin width and the eSiGe control, 3) Higher on-resistance caused by the decreased fin pitch and diamond-shaped epi profile dependence (Fig. 2.5). Two parameters are crucial to the accuracy of the bandgap voltage reference, namely, ΔV_{eb} and V_{eb} . The process spread and variations of these parameters across temperature as well as current density J of the BJT can affect the raw performance of the bandgap reference. These will be discussed in the measurement section where we extract the useful parameters required to determine the circuit performance. Recent FinFET [55] publications have shown good accuracy of such references. In our work, in order to achieve low area, we have used a custom BJT layout cell which is a merged area-efficient version, as well as used common-centroid layout and dummies all around the BJT array in order to achieve good matching. The emitter contacts are ensured to have very low resistance in order to enable high current density operation where the IR drop dominates. The BJT pair (emitter area ratio 1: N) is biased by the emitter current. The V_{eb} voltage is dependent on: 1) collector current I_c , 2) Saturation current I_s .

Current gain (β) of the BJT relates the emitter current I_e to I_c , as given by Eq. (2.2).

$$I_c = \frac{\beta}{1 + \beta} \cdot I_e \quad (2.2)$$

β is very low (2–3) in FinFET technology and its process and mismatch variance is dependent on the BJT bias current density. The difference in emitter-base voltage holds true when the ideality factor (η) is constant across the bias current density for both the BJT (emitter area ratio of N). Since V_{eb} depends on η , we need to ensure biasing at the current density that provides a flat-region of operation.

$$V_{eb} = \eta \frac{kT}{q} \cdot \ln\left(\frac{I_c}{I_s}\right) \quad (2.3)$$

$$\Delta V_{eb} = \eta \frac{kT}{q} \cdot \ln(N) \quad (2.4)$$

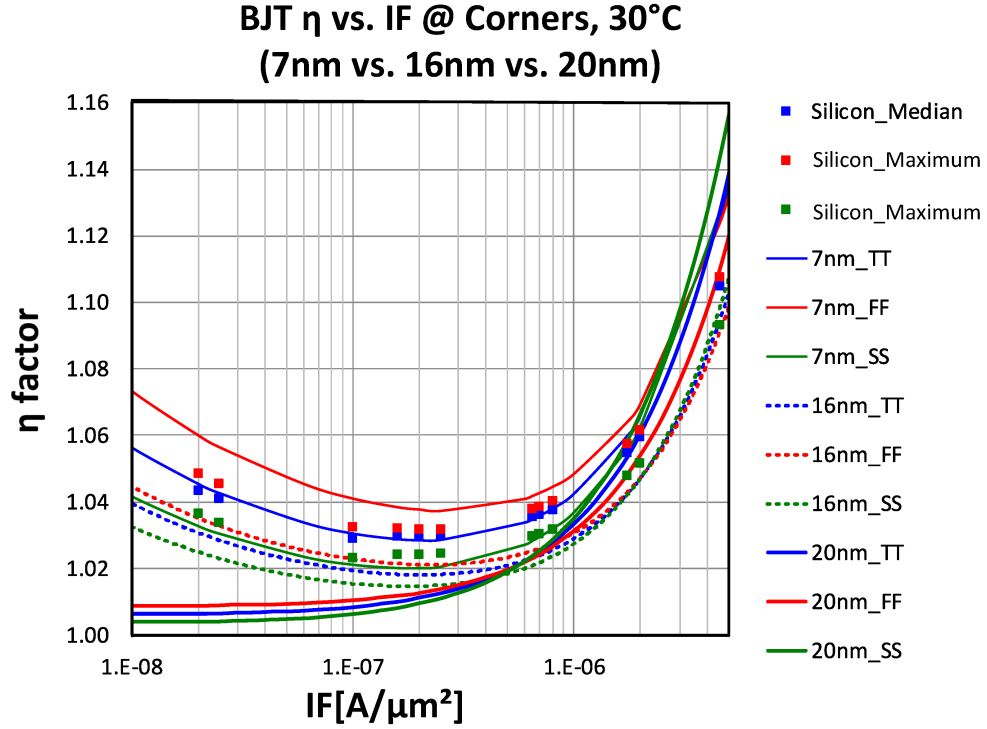


Figure 2.7: Simulated and measured process variation of non-ideality factor across BJT current. Note: The lines are simulated results. Measured data points are shown as markers.

The approximate expression for ΔV_{eb} is given by Eq. (2.4). In order to have a large signal-to-ratio, the ratio N should be increased from the circuit perspective. However, this could be disadvantageous since it would depend on the device characteristics (flatness of ideality factor η). Therefore, the parameter is co-optimized based on the SPICE model of BJT together with the circuit specification criteria to arrive at the current bias as well as the N ratio.

2.4 Device Modeling and Measurement

This section presents various experimental results of the test chips implemented in 7-nm FinFET to develop and validate the BJT SPICE models used for circuit design. Two 7-nm test chip results capture the silicon behavior of PNP BJT transistors and a comparison with 16-nm FinFET and 20-nm planar process is presented. All plots in the device modeling and measurement section are based on SPICE models unless specifically mentioned as ‘*silicon*’.

The non-ideality (η) factor is an important aspect of the BJT device characterization due to its direct impact on circuit performance. Fig. 2.7 shows the η variation across current

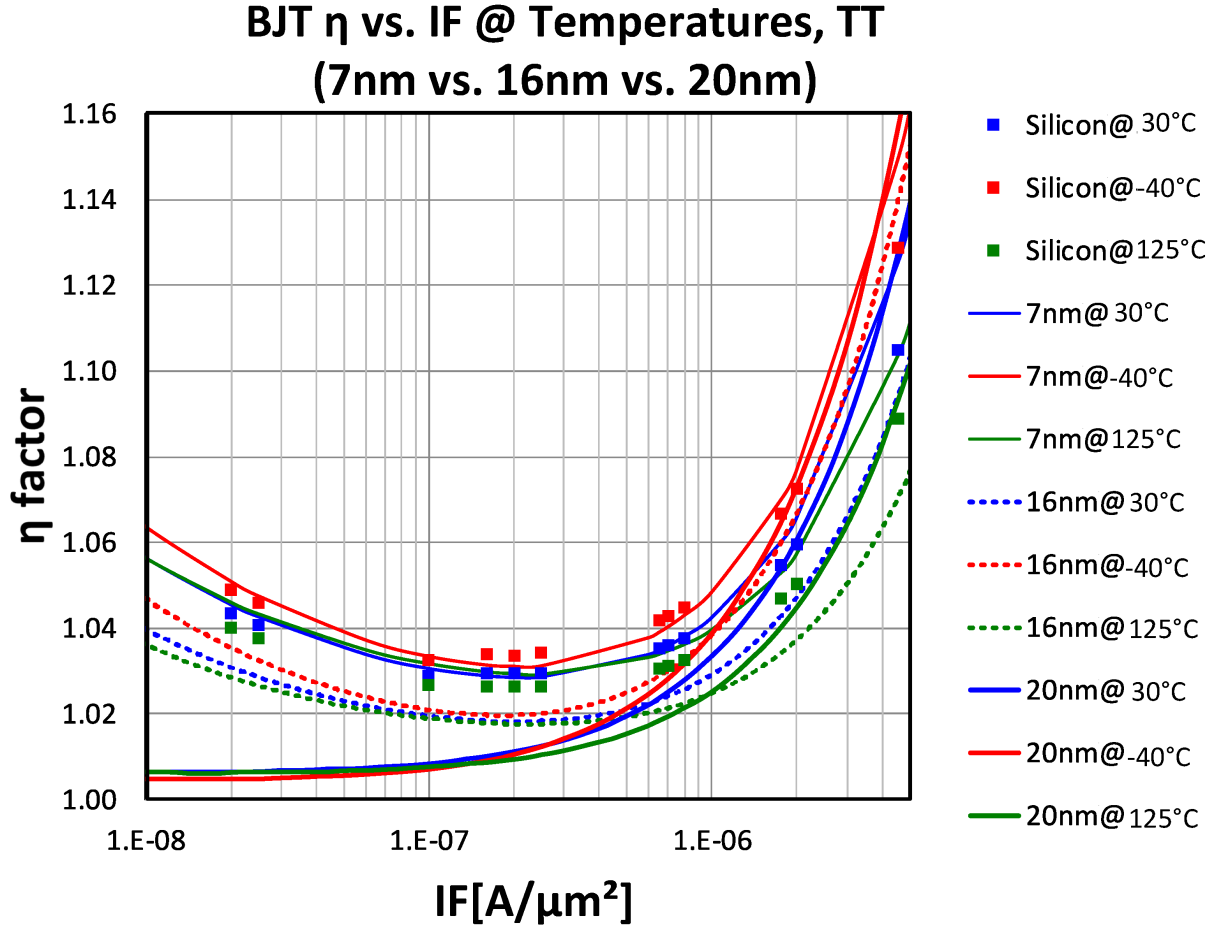


Figure 2.8: Simulated and measured temperature variation of non-ideality factor across BJT current. Note: The lines are simulated results. Measured data points are shown as markers.

density (I_F) for various process technologies and strengths. Compared to 20 nm and 16-nm nodes, the 7-nm FinFET shows larger variability. For example, at I_F of $0.1 \mu\text{A}/\mu\text{m}^2$, the variation is 2%, which translates to $\pm 400 \mu\text{V}$ for ΔV_{eb} of 40 mV. This variation is significant for the intended circuit applications, thus requiring trimming to reduce it further for better accuracy. Furthermore, the non-ideality factor also depends on temperature. Silicon results for 7-nm FinFET are also plotted in Fig. 2.8 to compare with the SPICE models. Based on the characterization results in Figs. 2.7 and 2.8, it is recommended that the BJT diode pair be biased with a current density between $0.1 \mu\text{A}/\mu\text{m}^2$ to $1 \mu\text{A}/\mu\text{m}^2$. This ensures the operation in the approximate flat non-ideality factor region. This choice also limits the usage of large diode array ratios, which were possible in older technologies. In the current design, we use

the nominal bias current density of $1 \mu\text{A}/\mu\text{m}^2$ for the smaller diode and the diode array ratio of seven. Each diode unit in the 1:7 ratio is made up of six minimum-size BJT devices available in the technology. Figure 2.8 shows the η variations at various temperatures.

Case 1: $I_F > 1 \mu\text{A}/\mu\text{m}^2$, non-ideality factor shows a distinct CTAT characteristic

Case 2: $I_F < 0.1 \mu\text{A}/\mu\text{m}^2$, the characteristic is a combination of positive and negative temperature coefficients.

These factors are crucial in the design of bandgap reference and temperature sensors and help to predict their accuracy limits and to define the appropriate choice of current density. Furthermore, this information could be exploited for compensation against temperature.

Recent works [19], [59], [55], [64] have shown BJT based circuits in FinFET process. Substrate PNP BJT is a commonly used element of the temperature sensor due to its weak sensitivity to package stress compared to the NPN variant [41]. Principle of operation of temperature sensor is that the difference in emitter-base voltages (ΔV_{eb}) of two BJTs with different current density show a linear dependence on absolute temperature. Therefore, a 1:10-ratio BJT structure is used for the characterization. The transfer function of ΔV_{eb} voltage vs. temperature T is used to calculate the resulting temperature. Figures 2.9 and 2.10 plot the SPICE characterization results of the residual of ΔV_{eb} from ΔV_{eb} -vs.- T transfer function at low and high current densities. As evident, the spread of ΔV_{eb} variation reduces with the increased bias current density. This choice of current density becomes more critical for the 7-nm FinFET node (compared to the 16-nm or 20 nm nodes) since the spread causes a larger error in circuits utilizing ΔV_{eb} .

$$V_{eb} = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_c}{I_s} \right) = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_e - I_b}{I_s} \right) \quad (2.5)$$

Equation (2.5) relates the emitter base voltage with the collector current and the saturation current of the BJT.

η = non-ideality factor,

k = Boltzmann constant,

q = charge,

T = absolute temperature.

Since the silicon substrate is commonly tied to ground, PNP BJT is biased via the emitter and hence is related to the collector current by the finite current gain (β) of the BJT ($I_e = (1 + \beta)I_c$).

$$V_{eb} = \eta \left(\frac{kT}{q} \right) \ln \left(\frac{I_{bias}}{I_s} \frac{\beta}{\beta + 1} \right) \quad (2.6)$$

In the above equation, non-ideality factor η depends on the current density used to bias the BJT, the saturation current depends on the process as well as the temperature. In the fine geometry technologies, the h_{21} or β -factor of the BJT is very low and the process variation is observed to be larger. This can be explained due to the base-emitter junction being squeezed inside the fin [15]. Therefore, it is important to take these into consideration. [15] discussed these aspects and design choices based on PNP BJT in 7-nm FinFET process. The bias current together with the BJT diode array ratio should be chosen so as to have a relatively flat non-ideality factor region. It should be noted that any non-linearity and spread directly contributes to the inaccuracy budget of temperature sensor. The difference in emitter-base voltage is a weak function of temperature (for example, a BJT diode array of 1:7 in 7-nm FinFET results in slope of $172\mu\text{V}/^\circ\text{C}$) and hence care must be taken to reduce the contribution of additional errors. It is observed that the above individual non-linearity and process spread due to η and β is lumped together and represents finally in the resulting voltage ΔV_{be} measurement. Figs. 2.9 and 2.10 show the residuals (between the actual ΔV_{eb} and linear fit) for three bipolar process corners at the low current density and high current density biasing of the BJT.

It is seen that the spread is higher for FinFET process compared to the planar CMOS process. Besides, it can be seen that the spread reduces at higher current density in both 7-nm and 16-nm FinFET process and the improvement ($\sim 1.6\times$) is higher at 7-nm. We believe the possible reasoning for this is that at higher current density the non-linearity due to η and β cancel each other approximately. We have chosen current density of $2\mu\text{A}/\mu\text{m}^2$ as the design parameter with the possibility to change this using digital registers based on the silicon-to-model correlation. It should be noted that at this large bias current, the accuracy of ΔV_{eb} is impaired by the parasitic resistances R_B and R_E associated with the base and emitter terminals respectively. Therefore, care should be taken that the series parasitic resistance

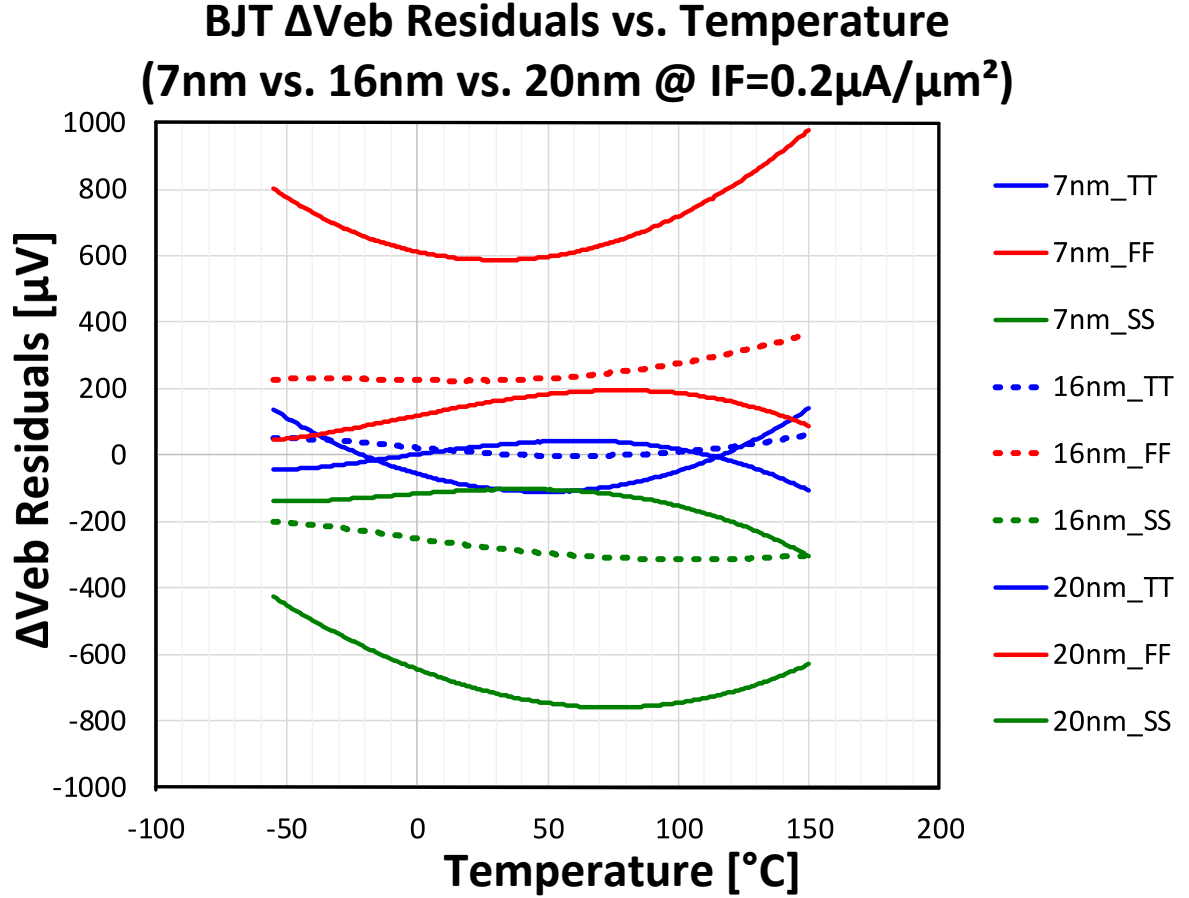


Figure 2.9: Simulated ΔV_{eb} residuals of 1:10 BJT pair.

is minimized and Kelvin connection is employed for measuring ΔV_{eb} . Fig. 2.10 shows the absolute max error in sensing temperature on-chip. It can be observed that the max error for each corner is low while the offset across different corners results in a larger error. The overall sensing error can be reduced if a unique digital equation mapping the voltage to temperature is used for each of the three corners. A conceptual figure of this is shown in Fig. 2.11.

Figures 2.12 and 2.13 reveal the mismatch (MM) results of the BJTs in the 7-nm FinFET node across the current density (I_F) and the array size. The x-axis indicates the number of cells of minimum-size unit-BJTs from the foundry. A Monte Carlo SPICE model parameter was developed for the design analysis [62]. Mismatch data for I_c and $\beta = \frac{I_c}{I_b}$ are used to fit the variance given by Eq. ((2.7)), where ‘s’ represents the spatial gradient [15]:

$$\sigma_{I_{cMM}\beta_{MM}}^2 = \frac{b_1^2}{W_e L_e} + \frac{b_2^2}{W_e^2} + \frac{b_3^2}{L_e^2} + b_4^2 s^2 \quad (2.7)$$

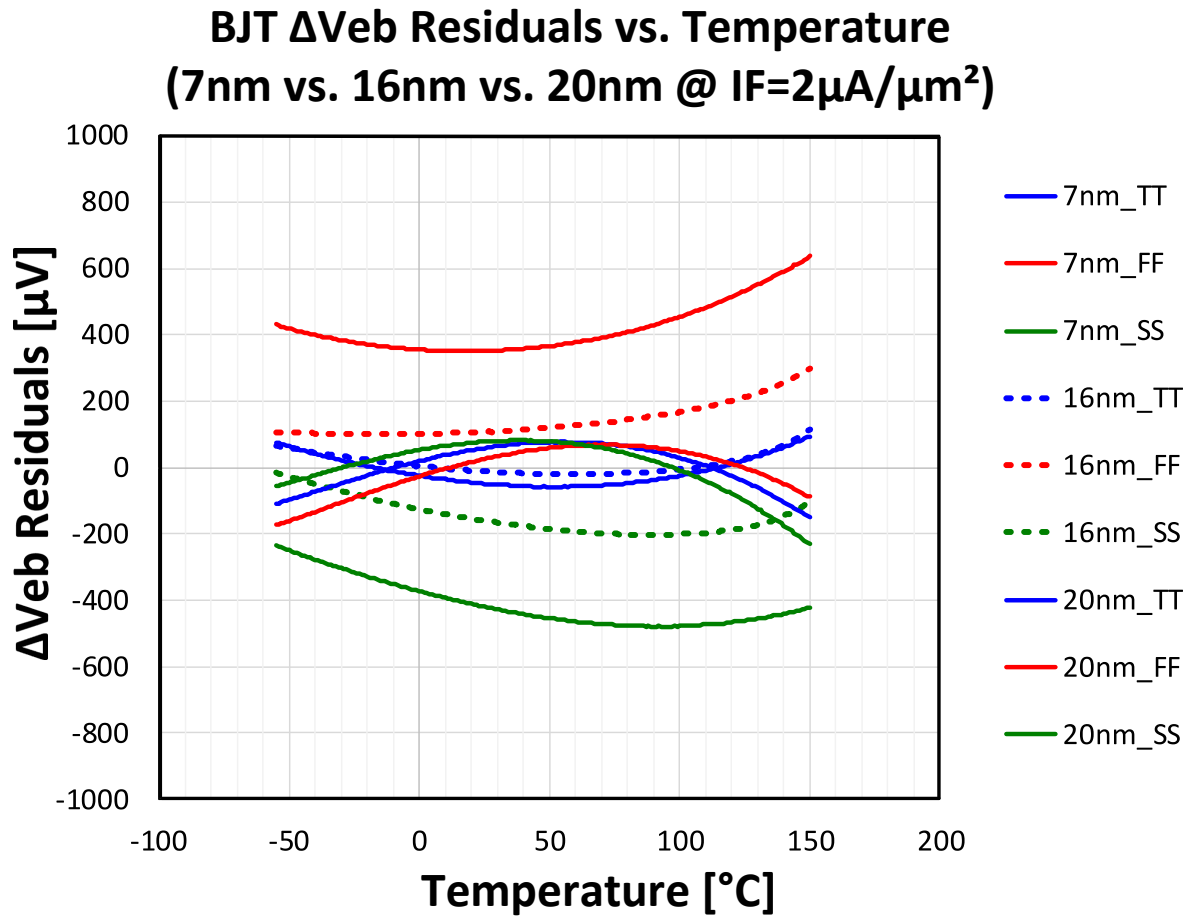


Figure 2.10: Simulated ΔV_{eb} residuals of 1:10 BJT pair.

It is observed from Figs. 2.12 and 2.13 that there is an inverse dependence of mismatch variance on I_c as well as on the area, $\sqrt{W \cdot L}$ (not uniform at all the lengths). This provides

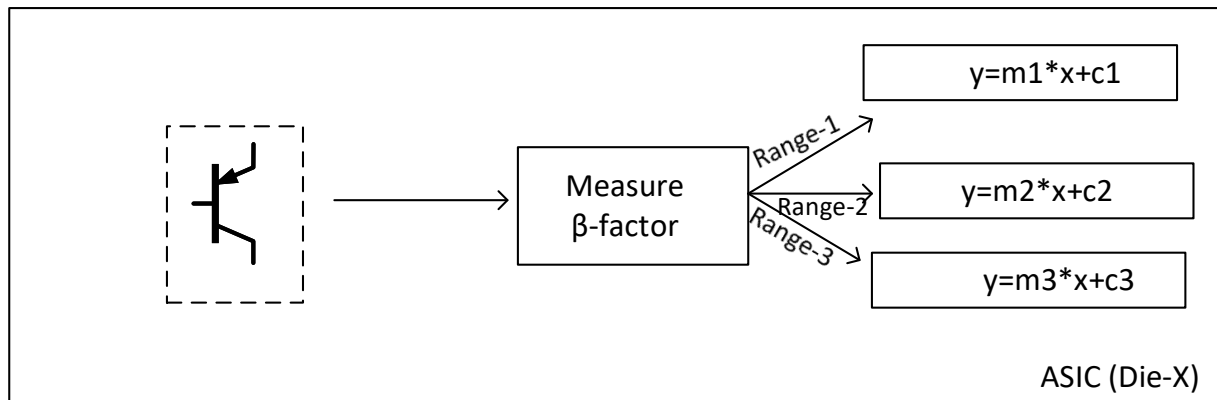


Figure 2.11: Trim to identify the BJT process.

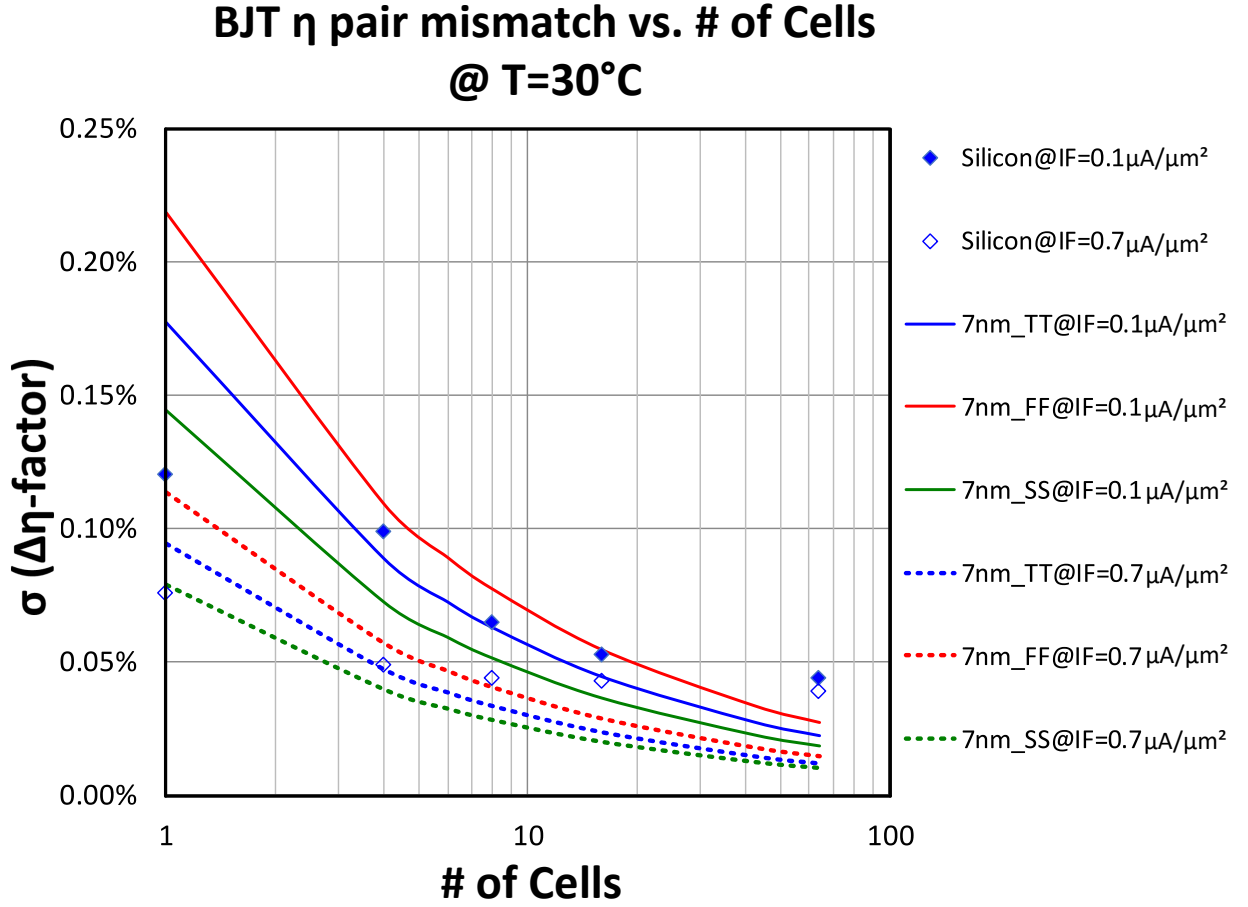


Figure 2.12: Simulated and measured BJT pair mismatch technology comparison (n-factor pair MM vs. number of cells). Note: The lines are simulated results, while the measured data points are shown as markers.

a guidance for the choice of array size for the BJT in the circuit design as well as the corresponding I_F .

Figures 2.14 and 2.15 show the comparison of the mismatch with respect to earlier technologies. They show a dependence on the bias current density. Compared to the process variation, it appears that mismatch is not a significant component for the design error budget. For example: 1) approximately $<0.2\%$ vs. 3.3% for n -factor, 2) $<0.2\text{ mV}$ vs 2.7 mV for V_{eb} .

2.5 Conclusion

This chapter presented the process technology and characterization results of PNP BJT devices in 7-nm FinFET CMOS. Multiple test-chip device characterization was done to

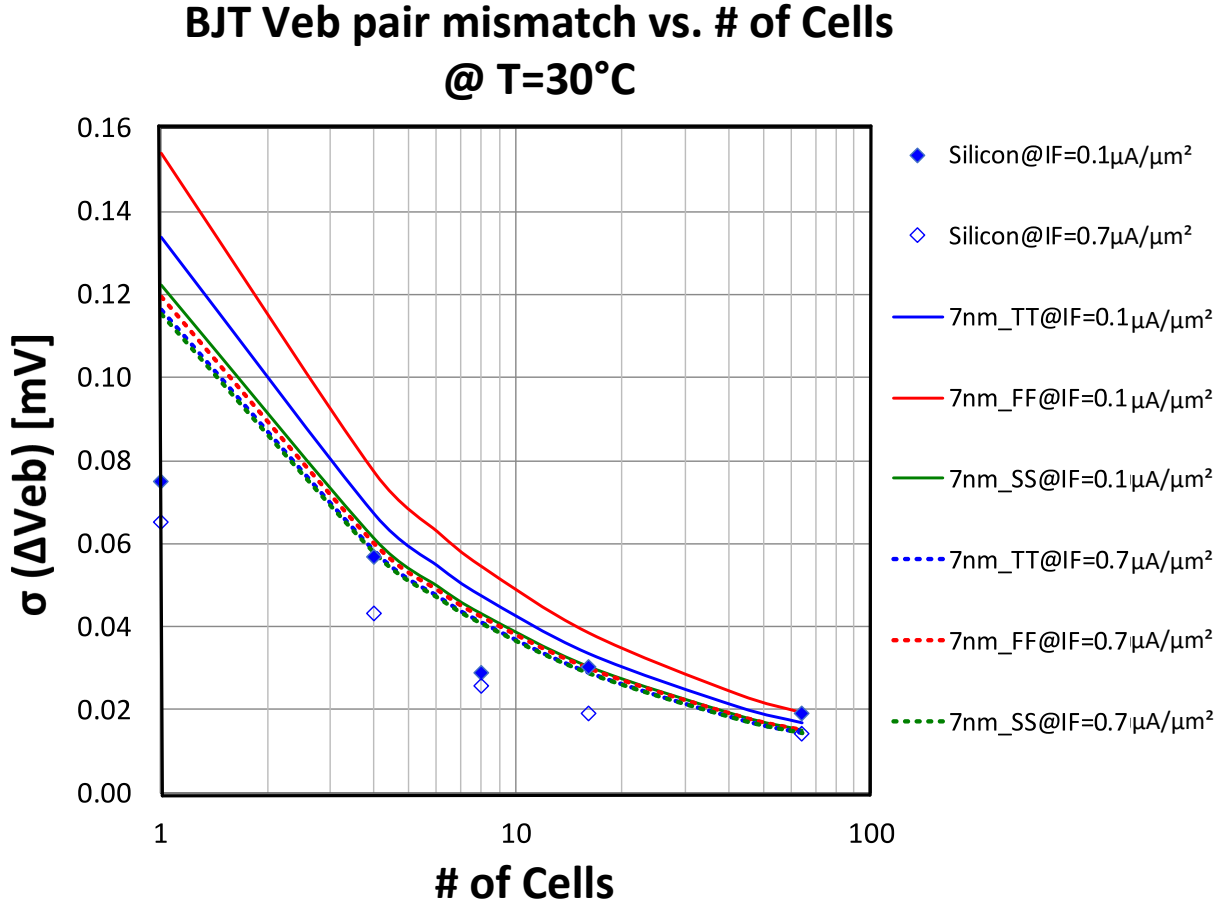


Figure 2.13: Simulated and measured BJT pair mismatch technology comparison (V_{eb} pair MM vs. number of cells). Note: The lines are simulated results, while the measured data points are shown as markers.

arrive at accurate device models. Comparison with previous process technologies showed the challenges associated with designing voltage references and temperature sensors in FinFET. Parameters, such as ideality factor (η), ΔV_{eb} voltage and its dependence on current density and temperature, have specifically been reviewed. Relevant device parameters have been matched between SPICE model and experimental characterization results, which are useful for circuit designers. This provides guidance for the design of BJT based circuits in scaled CMOS technologies. Example analog circuits, such as bandgap references and temperature sensors, which use BJTs will benefit from this guidance optimization to achieve high performance. Custom merged layout cell for BJT provides 20% area savings in the proposed implementation.

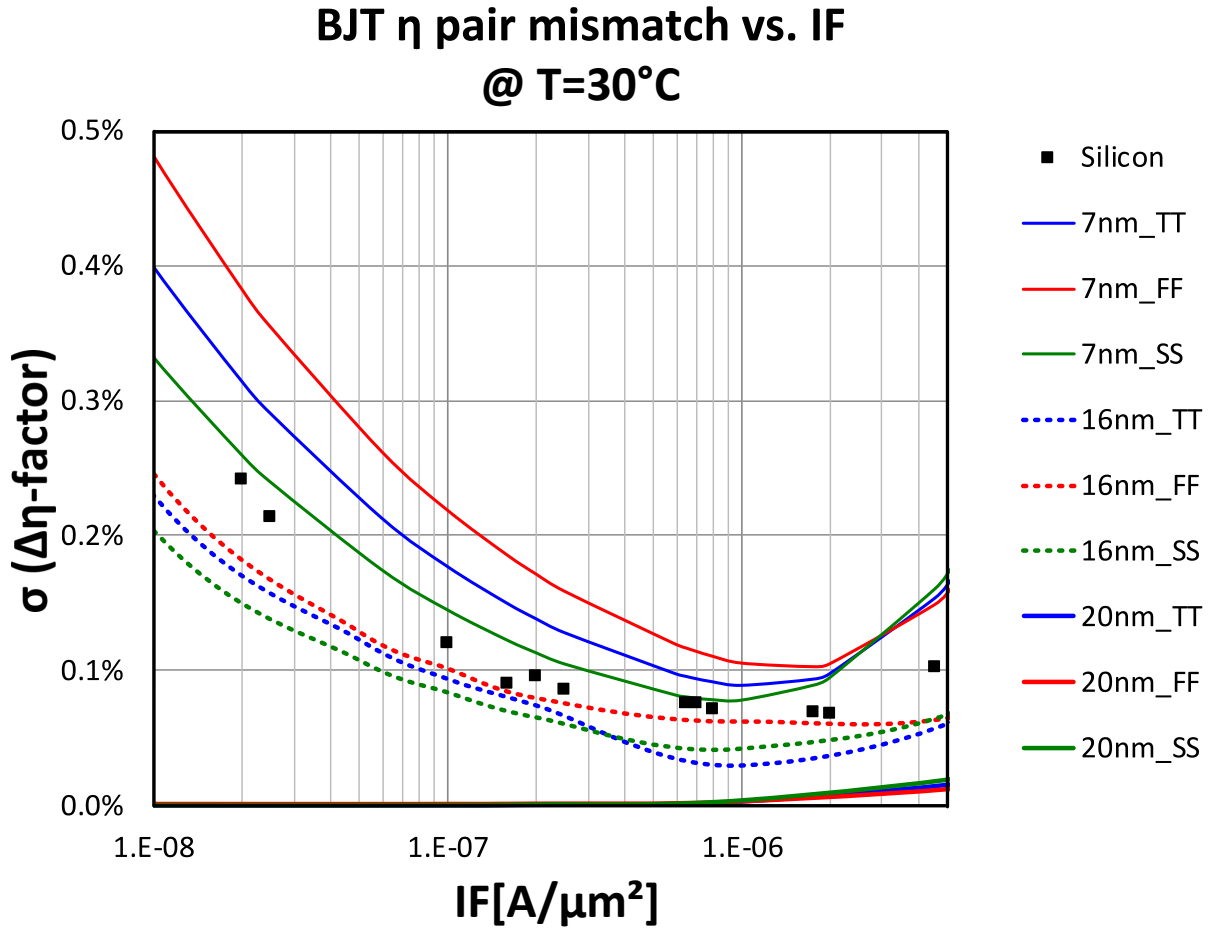


Figure 2.14: Comparison of BJT-pair mismatch of n-factor vs. I_F . Note: The lines are simulated results. Measured data points are shown as markers.

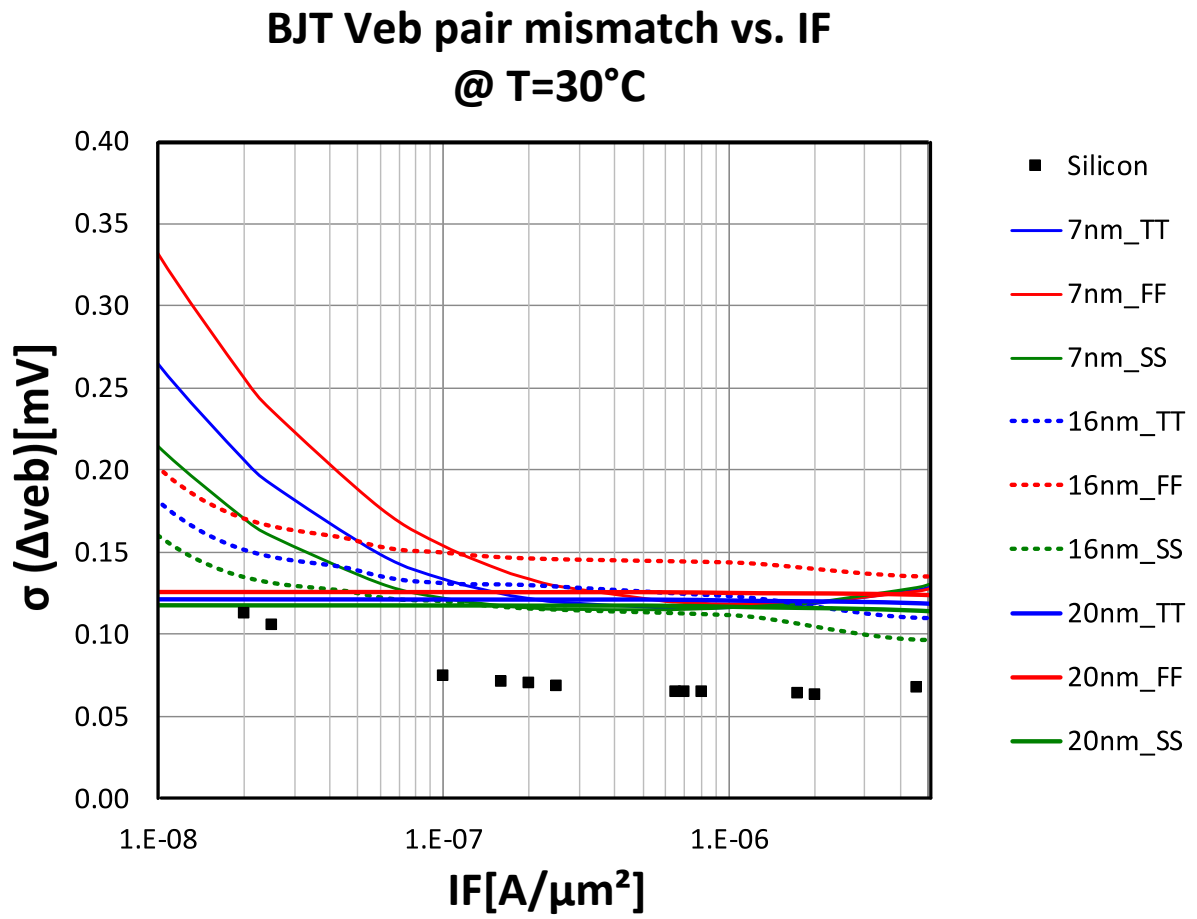


Figure 2.15: Comparison of BJT-pair mismatch of V_{eb} vs. I_F . Note: The lines are simulated results. Measured data points are shown as markers.

CHAPTER

3

Voltage References

The details of realizing a BJT in FinFET process and its associated characterization data and device modeling have been presented in Chapter 2. BJT forms a core for the realization of bandgap references. This chapter proposes the main architecture of the BJT-based bandgap reference which provides a curvature compensated output voltage across a wide temperature range (-45°C to 125°C). Two different curvature compensation schemes have been implemented, namely, a piecewise linear current summation method and secondly using a transconductance which converts a non-linear voltage to current to sum at the output voltage, thus reducing the non-linearity in reference voltage. There were few requirements from the voltage reference proposed in this work. The first requirement was that is needed to be of high accuracy, besides also being able to provide voltage with a certain ‘*temp-co*’. Since the PDK for the 7-nm technology was still not mature at the time of design, the architecture required to take into account any post-silicon changes with respect to the model. Therefore, sufficient trimming range had to be incorporated. The circuit performance has been verified by measurement.

3.1 Proposed Voltage Reference Architecture

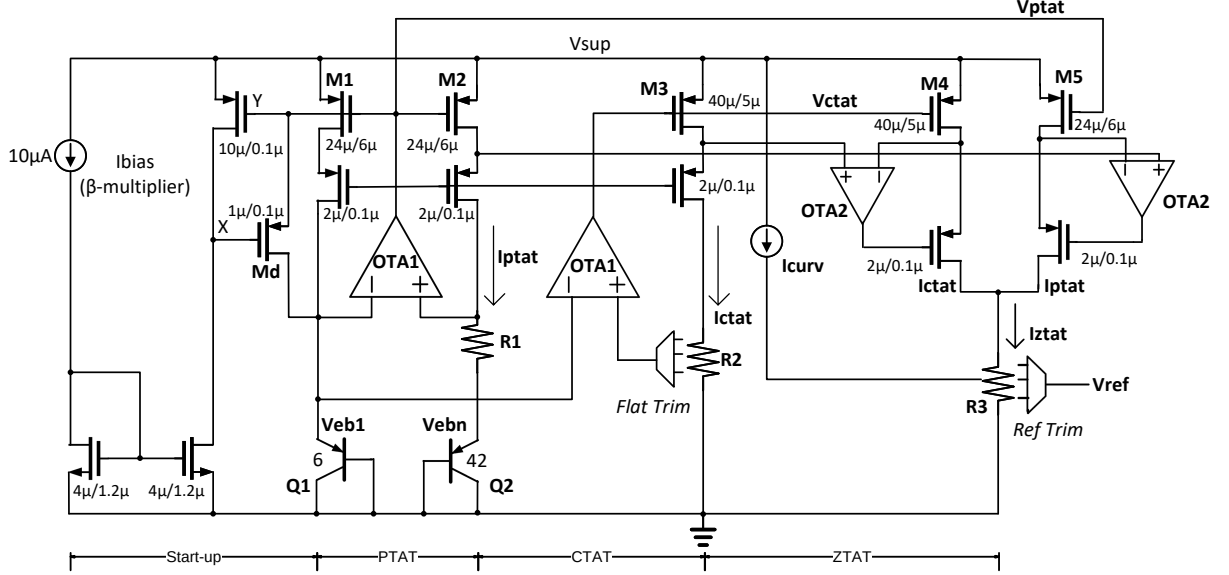


Figure 3.1: Architecture of 1-V bandgap reference with programmable ‘*temp-co*’. Note: Biasing circuitry not shown.

Fig. 3.1 shows the proposed overall architecture of the bandgap voltage reference. Parasitic PNP transistors Q_1 & Q_2 (ratio of emitter area 6:42) form the core of the reference architecture. The feedback loop formed by the BJT devices Q_1 & Q_2 together with the operational transconductance amplifier (OTA1) controls the gate voltage of PMOS devices M_1 and M_2 . The currents through M_1 and M_2 are identical and given by the difference in the emitter-base voltages of the two BJT divided by R_1 , shown by I_{ptat} in Fig. 3.1. The BJTs are biased with the current density required to keep them in the flat non-ideality (η) region of operation.

V_{eb1} refers to the emitter-base voltage of Q_1 while ΔV_{eb} is the difference between emitter-base voltages of Q_1 and Q_2 . The other OTA senses the emitter-base voltage of Q_1 and together with the resistor R_2 regulates the gate voltage of M_3 via a negative feedback loop. This sets the drain current of M_3 , given by I_{ctat} in Eq. (3.1). Both the OTAs are implemented as a folded-cascode architecture.

$$I_{ctat} = V_{eb1}/R_2, \quad I_{ptat} = \Delta V_{eb}/R_1 \quad (3.1)$$

The two components have opposite *temp-co*’s and are intended to have a ratio shown

by Eq. (3.2) in order to cancel their respective ‘*temp-co*’ thus giving a flat output across temperature.

$$\frac{V_{eb1}}{\Delta V_{eb}} = \frac{I_{ctat} R_2}{I_{ptat} R_1} = \frac{R_2 \ln(N)}{R_1} \quad (3.2)$$

The critical part of the bandgap is the accurate mirroring of the current since the mirror devices (M_1, M_2, M_5 as well as M_3, M_4) carry PTAT and CTAT current, respectively. A conceptual diagram of stacking [65] is shown in Fig. 3.2 to implement a long channel device, thus achieving a large output impedance for the current source.

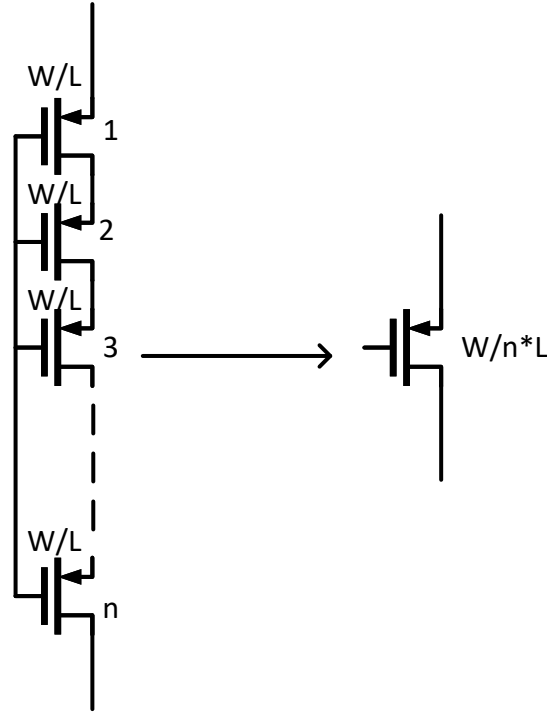


Figure 3.2: Stacking to achieve accurate current mirroring in FinFET.

Two main factors affecting the mirror accuracy is the threshold voltage (V_t) and current mirror factor (β) mismatch given by Eq. (3.3).

$$\sigma\left(\frac{\Delta I_{ds}}{I_{ds}}\right) = \frac{g_m \cdot A_{vt}}{I_{ds} \sqrt{W \cdot L}} + \frac{A_\beta}{\sqrt{W \cdot L}} \quad (3.3)$$

where: A_{vt} = mismatch of threshold voltage, A_β = mismatch of device geometric size. Assuming the MOS in strong inversion, we replace $g_m = \mu \cdot C_{ox} \cdot W/L \cdot (V_{GS} - V_T)$ and make

Eq. (3.3) as a function of L to evaluate the effect of stacking. This is given by Eq. (3.4) [65]

$$\sigma\left(\frac{\Delta I_{ds}}{I_{ds}}\right) = \frac{\sqrt{\mu C_{ox}} \cdot A_{Vt}}{L \cdot \sqrt{I_{ds}}} + \frac{A_{\beta}}{\sqrt{W \cdot L}} \quad (3.4)$$

From equation (3.4), we see that for a fixed drain current, the mismatch is inversely proportional to the channel length (stacking number). Each of the MOS forming the stack is made up of the longest allowed device in the FinFET process. As an example, [65] used 40 stack devices to achieve high accuracy mirroring. It is also interesting to note that based on Eq. (3.4), the V_t mismatch is inversely proportional to L while A_{β} mismatch is inversely proportional to $\sqrt{W \cdot L}$.

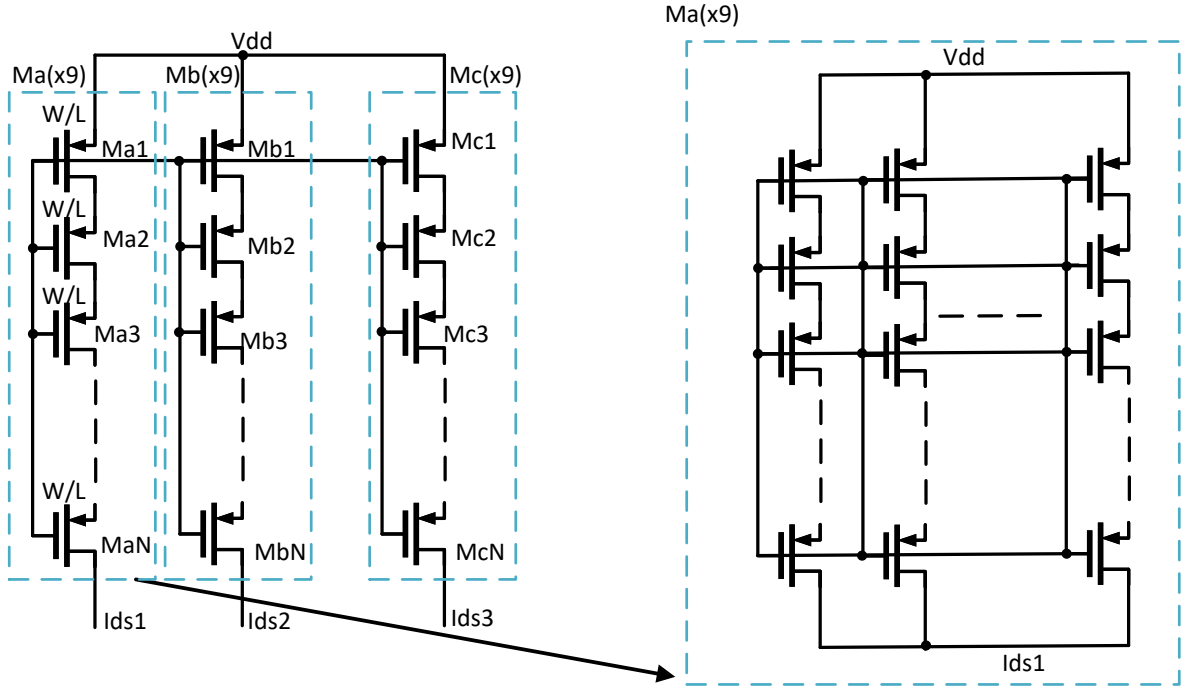


Figure 3.3: Stack device structure for matching current mirror. (Plot from Ref. [55])

For a given stack of devices M_a shown in Fig. 3.3, the overdrive on each device is given by:

$$V_{GS1} = V_G - V_{DD} \quad (3.5)$$

$$V_{GS2} = V_G - (V_{DD} - I_{DS1} R_{DS1}) \quad (3.6)$$

$$V_{GS2} = V_G - (V_{DD} - I_{DS1}R_{DS1} - I_{DS1}R_{DS2}) \quad (3.7)$$

where:

I_{DS1} = mirror current,

R_{DS1} = finite output impedance,

V_{GS1} = gate-to-source voltage associated to the device 1.

It can be seen from the above equations that the overdrive across different devices is descending (device forming the stack closest to the supply has the largest overdrive voltage). Therefore, it can be deduced that the contribution to mismatch due to devices at various stages of the stack and in turn having different overdrive voltages is different (referring to Eq. (3.3), we see that a lower g_m or in other words higher overdrive voltage translates to a lower mismatch).

Fig. 3.3, which is taken from Ref. [55] shows the contribution to mismatch based on the position in stack.

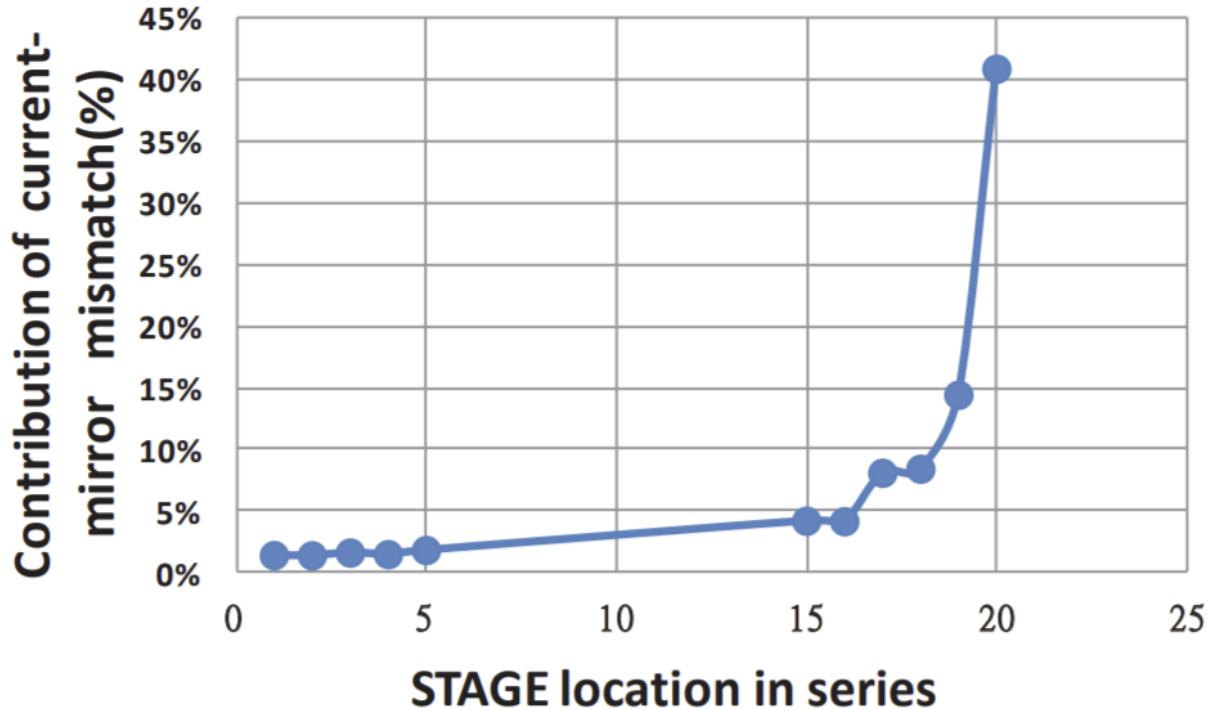


Figure 3.4: Stack device contribution to mismatch in current mirror. [Plot from Ref. [55]]

Fig. 3.5 (taken from ref. [65]) shows an area efficient floorplan structure for such mirrors where the devices which contribute low to the mismatch (for example M_{a1} to M_{a16} for a

20 stack) form the periphery (or similar to dummy devices in traditional layout) while the critical devices (for example M_{a17} to M_{a20} for a 20 stack) form the inner core of the layout cell. This technique can be particularly useful when the area available for the realization of such mirror structures is limited.

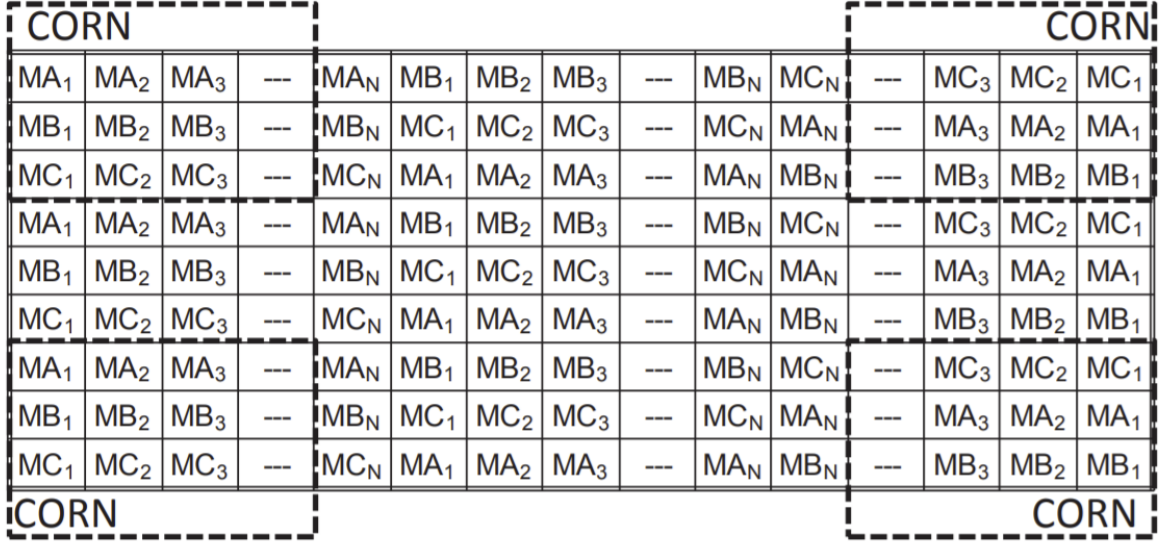


Figure 3.5: Floorplan of current-mirror. (Plot from Ref. [55])

The loop in Fig. 3.1 formed together with Q_1/Q_2 has two stable points of operation (zero current or the required current state); therefore, the start-up circuit ensures the right region of operation. The start-up circuit involves PMOS M_d . During the zero-current state of the loop formed with Q_1/Q_2 , node Y is at the supply level while node X is at the ground. This causes M_d to inject current into Q_1 thus building up the emitter-base voltage (V_{eb1}). This continues until node Y is pulled low to the required level for M_1/M_2 to provide the bias current I_{ptat} . As soon as this condition is reached, the start-up device is shut-off and M_d no longer conducts.

In order to satisfy the stated system-level requirement of providing a controllable ‘temp-co’, the two feedback loops are made independent. The difference in emitter-base voltage (ΔV_{eb}) is PTAT, while the emitter-base voltage (V_{eb}) is CTAT. ΔV_{eb} has a lower absolute ‘temp-co’ compared to that of V_{eb} . Therefore, resistor $R_2=42.08\text{ k}\Omega$ must be larger than $R_1=4.38\text{ k}\Omega$ and hence, the programmability of ‘temp-co’ is provided by adjusting R_2 . The “flat-trim” code controls the effective value of R_2 through a MUX which selects the tap-off point for

the feedback. The resulting currents are summed into the load resistor ($R_3=33.61\text{ k}\Omega$) to produce the desired voltage V_{ref} , as given by Eq. (3.8). The “*ref-trim*” code selects an R_3 tap for the absolute value of output voltage.

$$V_{ref} = \left(\frac{\Delta V_{eb}}{R_1} + \frac{V_{eb1}}{R_2} \right) \cdot R_3 \quad (3.8)$$

The mux control “*flat-trim*” and “*ref-trim*” codes are 7-bit wide. Each step in either R_2 or R_3 corresponds to a change of $\sim 40\text{ }\Omega$. For the “*flat-trim*” control, the trimmable resistor section of R_2 is $\pm 6\%$ while for the “*ref-trim*” code control, the trimmable resistor section of R_3 is $\pm 7.5\%$. Although the bus-width of the “*ref-trim*” code could have been smaller than that of the “*flat-trim*” code, in this design, the same resistor ladder and mux were used to implement both. The effect of offset is minimized by tapping-off both loops from the same BJT’s (Q_1) emitter-base voltage. There is no offset compensation employed for the amplifiers. Section 3.3 discusses the trimming techniques proposed to select the *flat-trim* code for the bandgap reference.

Since the circuit operates at a minimum supply of 1.375 V , both feedback loop amplifiers are implemented in a folded-cascode architecture. The PTAT and CTAT mirrored currents are gain-boosted in order to achieve accurate mirroring as well as to maximize the power supply rejection ratio (PSRR).

3.2 Curvature Compensation in Voltage Reference Circuits

To achieve a better voltage reference precision, the architecture in Fig. 3.1 implements a curvature correction current (represented simply as I_{curv}), which adds to the CTAT (mirrored by M_4) and PTAT (mirrored by M_5) components. Two methods are implemented to realize I_{curv} , one of which is an approximation based on a piecewise-linear current DAC [66], shown in Fig. 3.6, while the other is a BJT-based second-order curvature correction, shown in Fig. 3.7. These can be enabled separately.

3.2.1 IDAC-Based Approximate Curvature Correction

The first method of implementing the I_{curv} current source in Fig. 3.1 is based on the use of multiple current sources to generate the required non-linear current shape to correct the second-order (bow shaped) bandgap voltage curvature.

I_{ctat} and I_{ptat} are mirrored from transistors M_4 and M_5 in Fig. 3.1, respectively.

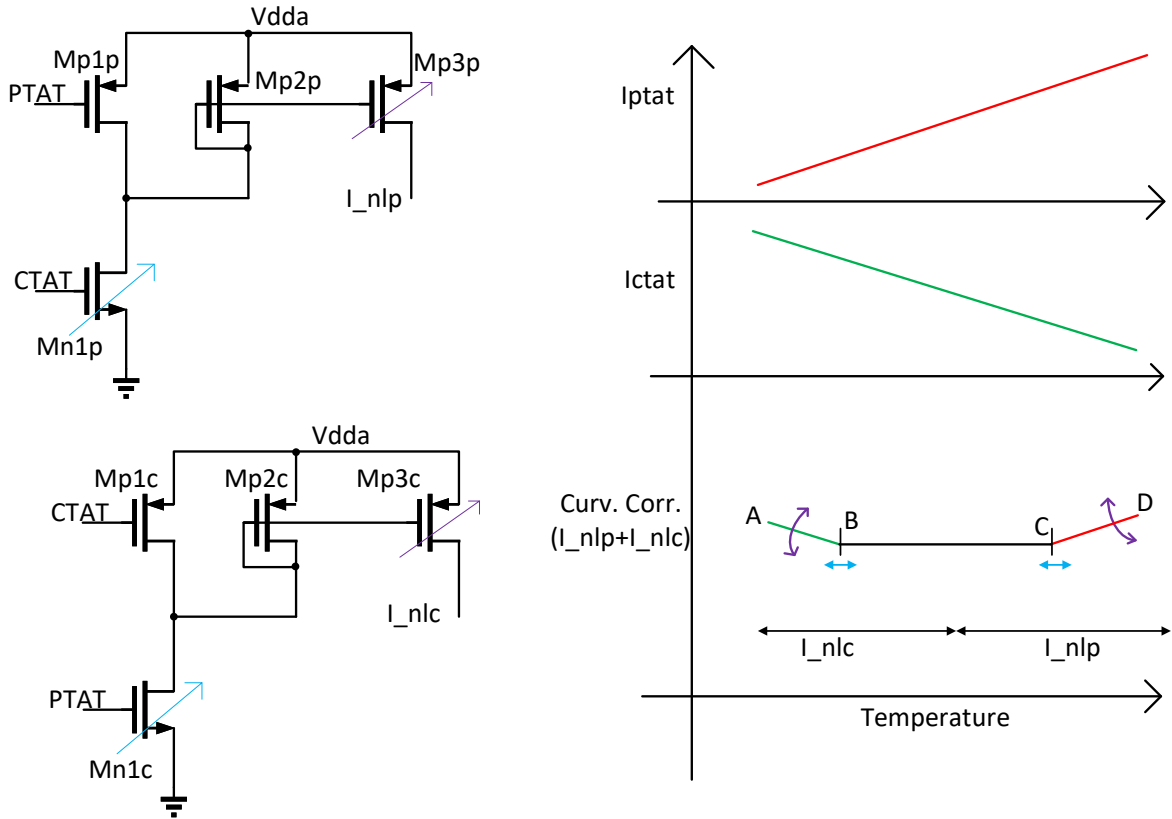


Figure 3.6: IDAC-based approximate curvature correction method.

The diode-connected devices, M_{p2c} and M_{p2p} , in Fig. 3.6 provide the required currents when the source current (top left-most transistor) is less than that of the sink (bottom left-most transistor). This generates I_{nlc} and I_{nlp} which sum together to form the I_{curv} current source in Fig. 3.1. In Fig. 3.6, the part of the curve from A to B is produced by M_{p3c} when M_{p1c} sources less current than M_{n1c} sinks, i.e. CTAT current is greater than PTAT current, while the part of the curve from C to D is produced by M_{p3p} when M_{p1p} provides

less current than M_{n1p} i.e. PTAT current is greater than CTAT current. This is summarized in Eqs. (3.9) and (3.10).

$$V_{sg,Mp2c} = \begin{cases} \sqrt{\frac{2(I_{ctat} - I_{ptat})}{\beta_p}} + |V_{thp}|, & \text{if } I_{ctat} \geq I_{ptat} \\ 0, & \text{otherwise} \end{cases} \quad (3.9)$$

$$V_{sg,Mp2p} = \begin{cases} \sqrt{\frac{2(I_{ptat} - I_{ctat})}{\beta_p}} + |V_{thp}|, & \text{if } I_{ptat} \geq I_{ctat} \\ 0, & \text{otherwise} \end{cases} \quad (3.10)$$

where:

$$\beta_p = \frac{\mu_p \cdot C_{ox} \cdot W}{L},$$

μ_p = mobility,

C_{ox} = oxide capacitance density,

$\frac{W}{L}$ = dimension ratio of the corresponding PMOS device,

V_{thp} = threshold voltage of PMOS device.

In the design, we include two controls: 1) adjust the mirror ratio (two bits) for the final copy (M_{p3p} and M_{p3c}) which controls the slope. 2) other two bits are to adjust the sinking current ratio (M_{n1p} and M_{n1c}) which sets the intersection points (B and C) in Fig. 3.6. These controls are intended to be fixed settings for all the chips and were only included to handle any possible uncertainty in the early model. Mirror copy of the diode voltages, given by Eqs. (3.9)–(3.10), produces the required piecewise linear shape (I_{curv}), shown in Fig. 3.6. The output current I_{nlc} is given by $I_{ctat} - I_{ptat}$ when the CTAT current is larger than the PTAT current, while I_{nlp} is given by $I_{ptat} - I_{ctat}$ when the PTAT current is larger than the CTAT current. This is expected to approximately correct the 2nd-order curvature of the bandgap's bow shape. The sizing of the current mirrors is done to ensure the cancellation is accurate by design.

3.2.1.1 Analog Bipolar Curvature Correction Method

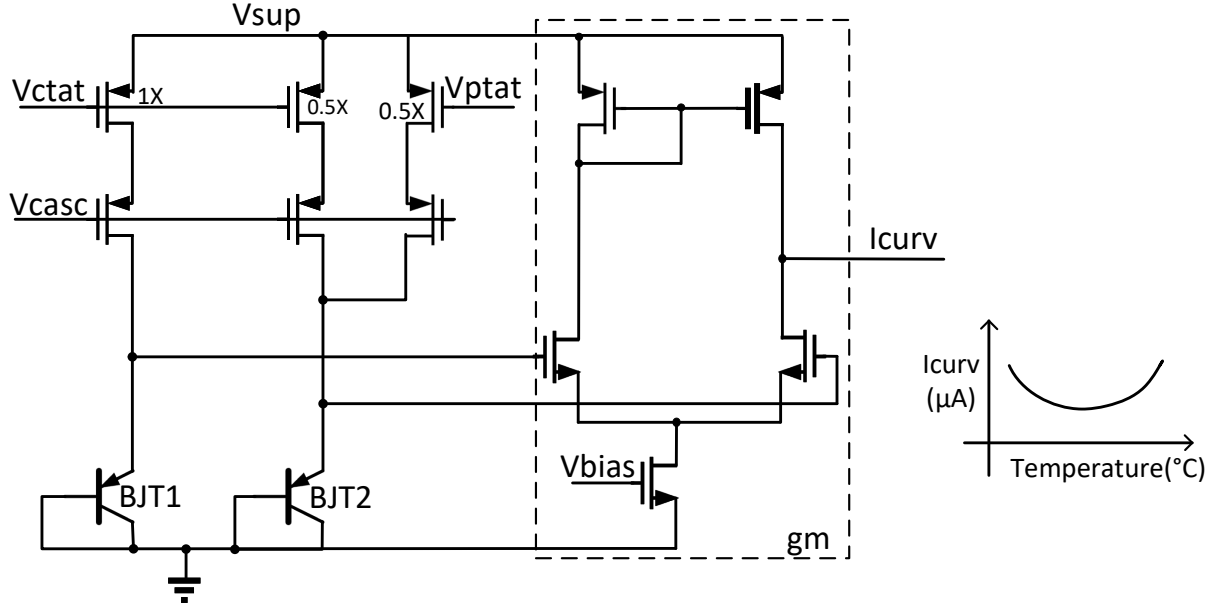


Figure 3.7: Analog bipolar curvature correction method.

The emitter-base voltage of BJT has a component which depends on ‘*temp-co*’ of the current used to bias the BJT. A more generic form of emitter-base voltage at any arbitrary T as a function of a specified reference temperature T_r is given by Tsividis [13].

$$V_{eb}(T) = V_{Go} \left(1 - \frac{T}{T_r} \right) + \frac{T}{T_r} V_{eb}(T_r) - (n - \delta) \left(\frac{kT}{q} \right) \ln \left(\frac{T}{T_r} \right) \quad (3.11)$$

Since the BJTs are biased using PTAT current, the value of $\delta=1$ in Eq. (3.11). If the biasing current is CTAT, then value of $\delta=0$. This leads to the following:

$$V_{ebPTAT}(T) = V_{Go} \left(1 - \frac{T}{T_r} \right) + \frac{T}{T_r} V_{eb}(T_r) - (n - 1) \left(\frac{kT}{q} \right) \ln \left(\frac{T}{T_r} \right) \quad (3.12)$$

$$V_{ebCTAT}(T) = V_{Go} \left(1 - \frac{T}{T_r} \right) + \frac{T}{T_r} V_{eb}(T_r) - n \left(\frac{kT}{q} \right) \ln \left(\frac{T}{T_r} \right) \quad (3.13)$$

Subtracting Eq. (3.13) from (3.12) provides V_{NL} given by:

$$V_{NL} = V_{ebPTAT}(T) - V_{ebCTAT}(T) = \left(\frac{kT}{q} \right) \ln \left(\frac{T}{T_r} \right) \quad (3.14)$$

This term, V_{NL} , given by Eq. (3.14) presents the inverse of the bandgap bow curvature [12]. This voltage difference (V_{NL}) is converted to a current by a simple transconductor (g_m) and summed into R_3 , as shown in Fig. 3.1 and given by eq. (3.15). The main source of non-linearity is the term V_{eb1} which has nonlinear dependence on temperature. Therefore, the additional current provided by $g_m \cdot V_{NL}$ compensates for the non-linearity.

$$V_{ref} = \left(\frac{\Delta V_{eb}}{R_1} + \frac{V_{eb1}}{R_2} + g_m \cdot V_{NL} \right) \cdot R_3 \quad (3.15)$$

The transconductor is realized using a simple single-stage differential pair as shown in Fig. 3.7, while the mismatch is minimized by using standard layout techniques for the additional BJT pair and PMOS current biasing shown in Fig. 3.7. Additionally, the bandgap reference involves digitally assisted trimming (explained in Section 3.3) and, therefore, any variation in g_m is trimmed out. This is because the contribution of the g_m variation is included in the voltage measurement done at the two temperatures as part of the trim procedure. In order to accommodate any BJT model variation (compared to silicon), the BJT2 was chosen with two different sizes which can be configured using a single bit. This bit-control once set, is not changed across the different samples for the measurement results.

3.2.2 PTAT Bias Current Generation

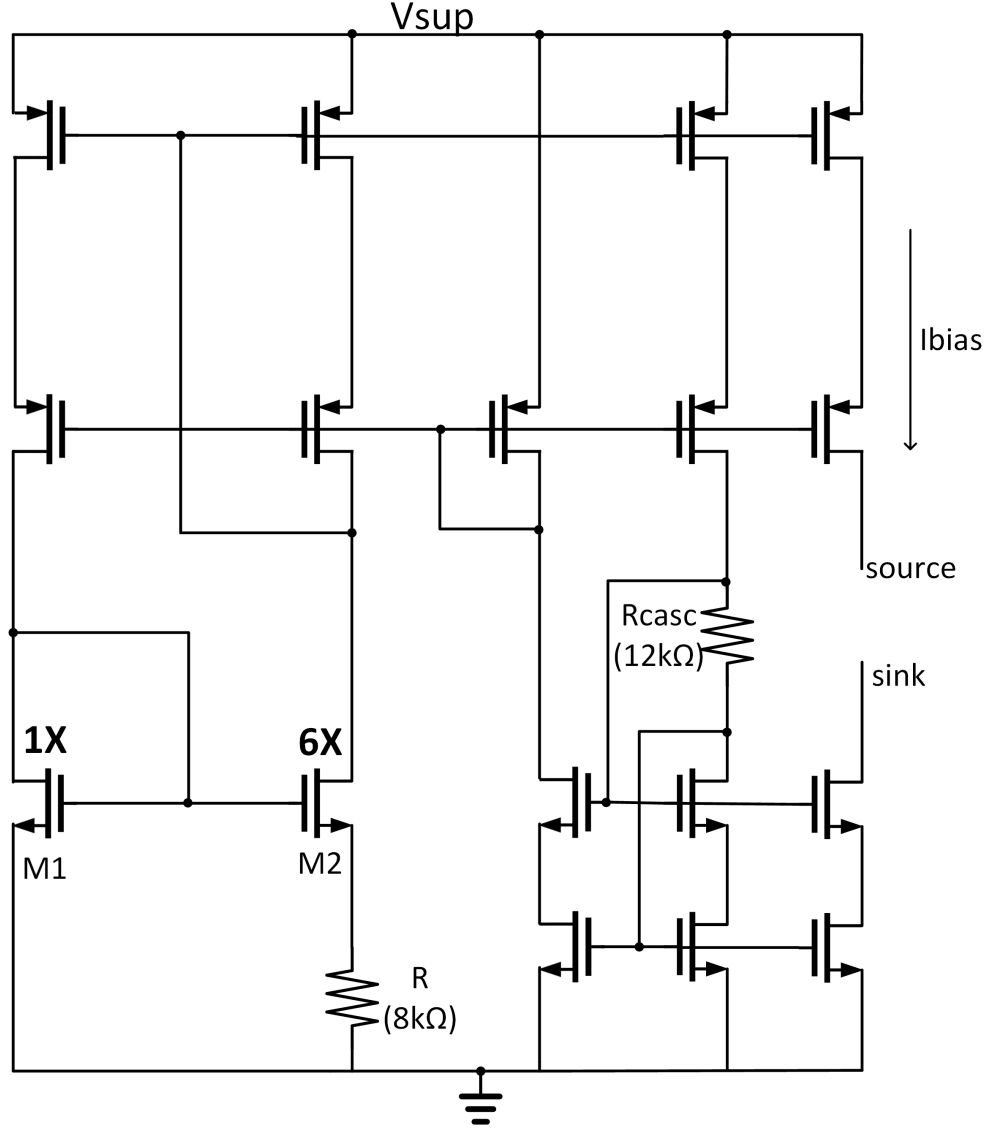


Figure 3.8: PTAT bias current generation.

A PTAT current generator [67] is at the heart of the bias current generation circuitry (I_{bias}) used for generating the bias and cascode voltages in Fig. 3.1. Figure 2.2 shows circuit details of the complete bias generation block. It consists of the core circuitry made up of the β -multiplier part (1:6 width ratio of the NMOS devices M_1/M_2 together with the resistor $R=8\text{k}\Omega$). The negative feedback loop ensures that the current flowing through M_2 is the same as through M_1 . Using Eqs. (3.16) and (3.17) together with the M_1/M_2 ratio i.e.

$\beta_{n2} = 6 \times \beta_{n1} = 6 \times \beta$ in Eq. (3.18)) gives the bias current in Eq. (3.19)).

$$V_{gs1} = \sqrt{\frac{2 \cdot I_{bias}}{\beta_{n1}}} + V_{thn} \quad (3.16)$$

$$V_{gs2} = \sqrt{\frac{2 \cdot I_{bias}}{\beta_{n2}}} + V_{thn} \quad (3.17)$$

$$V_{gs1} = V_{gs2} + I_{bias} \cdot R \quad (3.18)$$

$$I_{bias} = \frac{0.7}{\beta \cdot R^2} \quad (3.19)$$

in which $\beta = \frac{\mu_n \cdot C_{ox} \cdot W}{L}$, where:

μ_n = mobility,

C_{ox} = oxide capacitance density,

$\frac{W}{L}$ = dimension ratio of unit NMOS used for M_1 and M_2 in Fig. 3.8. The mirror devices are cascoded to ensure a good rejection of supply noise. The currents are brought out onto the pads for characterization purposes. The spread of output current is dominated by the process spread of the resistor (R), which is fixed in our design as the current was used mainly for biasing purposes. A further improvement is to trim the resistance, thus achieving lower output current variation.

Equation (3.19)) provides the expected output current which has an inverse relationship with β and the square of resistance. The resistor R was implemented using high-R flow in FinFET which has a low temperature dependency.

3.3 Trimming Techniques

Wafer-level trimming is adopted in CMOS ICs to overcome imperfections due to process spread and random device variations, which are expected to be large in the deep nanoscale technology. This helps to achieve high yield without sacrificing the performance.

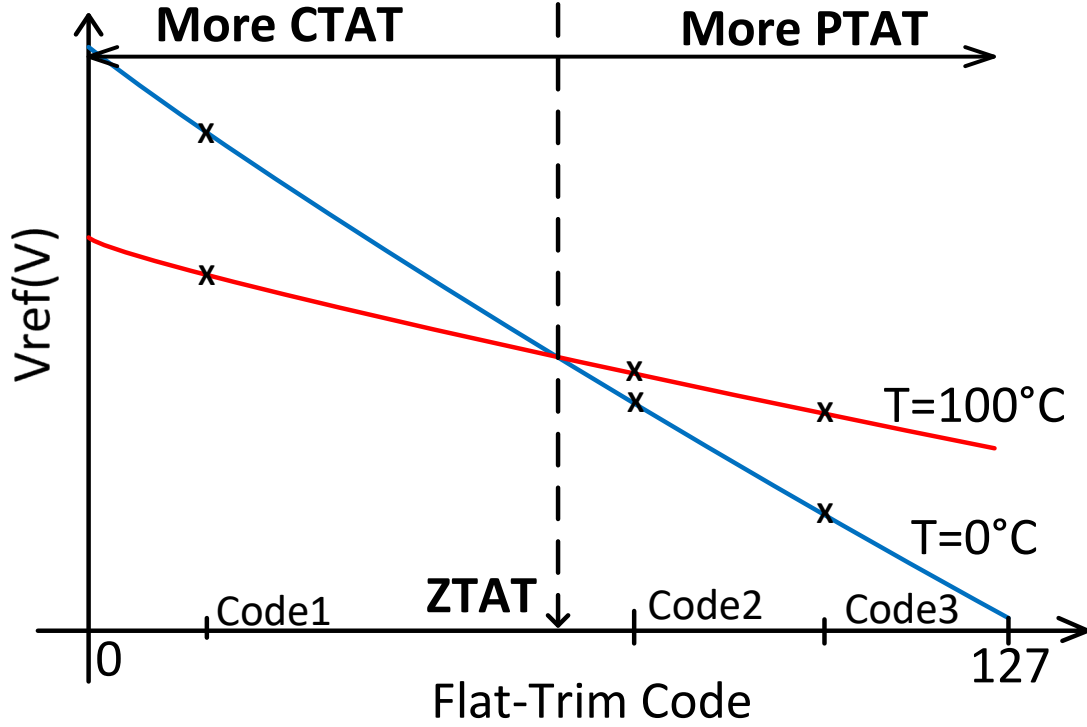


Figure 3.9: Concept of digitally assisted trim scheme with adjustable ‘temp-co’.

In our design, the trim procedure is as follows:

1. Measuring the output voltage for three widely spaced values of the *flat-trim* code, which estimates the transfer function of the output voltage (V_{ref}) vs. *flat-trim* code for a given temperature.
2. These voltages are first measured at 0°C , and then again at 100°C .
3. The two sets of three initial measurements are stored in e-fuses, which completes the trimming step.
4. These six values are then used within an FPGA to fit two quadratic equations of the output voltage vs. *flat-trim* code, which is illustrated by Fig. 3.9.

The residuals after the linear and quadratic equation fit at $T=0^{\circ}\text{C}$ are shown in Fig. 3.10. It is found that most errors can be removed (to within $< \pm 100 \mu\text{V}$) after the quadratic equation fit, which necessitated measurement at three *flat-trim* codes. The residual error after the quadratic equation fit at $T=0^{\circ}\text{C}$ and 100°C is shown in Figs. 3.11 and 3.12 respectively. During the regular operation, a ZTAT ‘temp-co’ is obtained as the *flat-trim* code corresponding to the intersection of both curves, as shown by the “ZTAT” code in Fig. 3.9. Once this “golden

code" has been calculated, it is set and the "*ref-trim*" code, which is linear and whose step-size is known by design, is adjusted to obtain an output as close to 1 V as possible. This way, an additional voltage measurement step for *ref-trim* is avoided. It should be noted that this trim technique removes most of the offset related to OTA1 (Fig. 3.1) as well as to that of the curvature-correction g_m (Fig. 3.7). This is because, as part of the trimming procedure, the output voltage is measured at two temperatures. Therefore, any variation in gain is expected to be removed and any remaining contribution is below our error budget. Furthermore, since the three measurements are done at each temperature, the effect of offset is trimmed out. This is explained further using a Matlab model developed to show the effect in appendix 5. The measurement results presented in Section 3.4 do not involve any additional offset cancellation techniques for the OTAs.

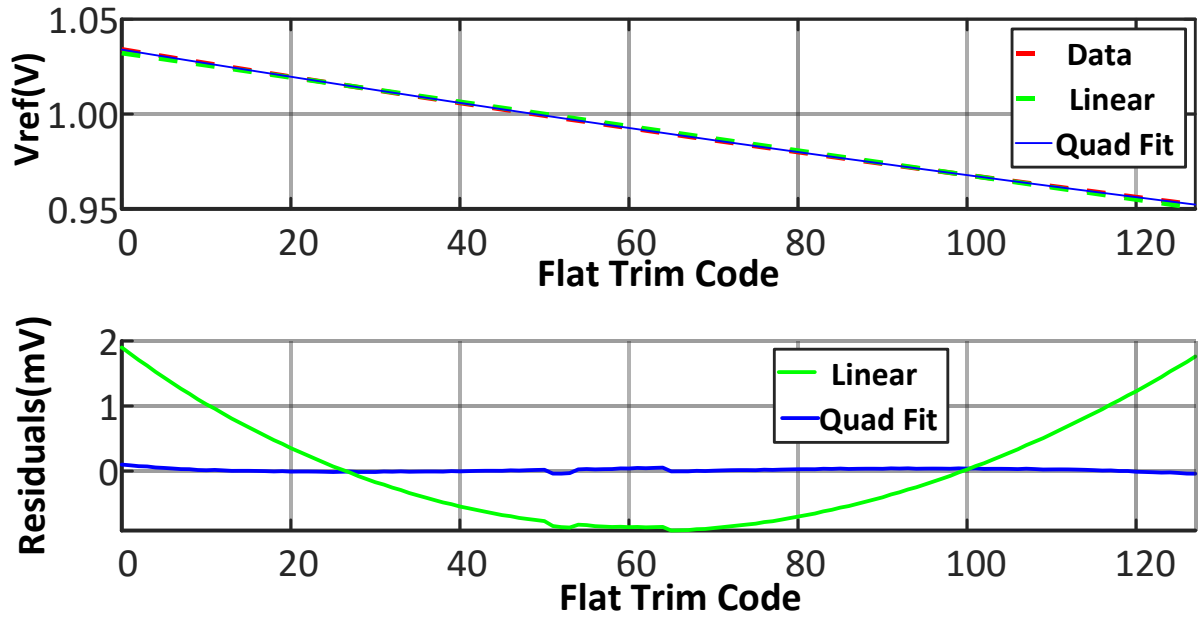


Figure 3.10: Residual error comparison between linear and quadratic equation fit at $T=0^{\circ}\text{C}$.

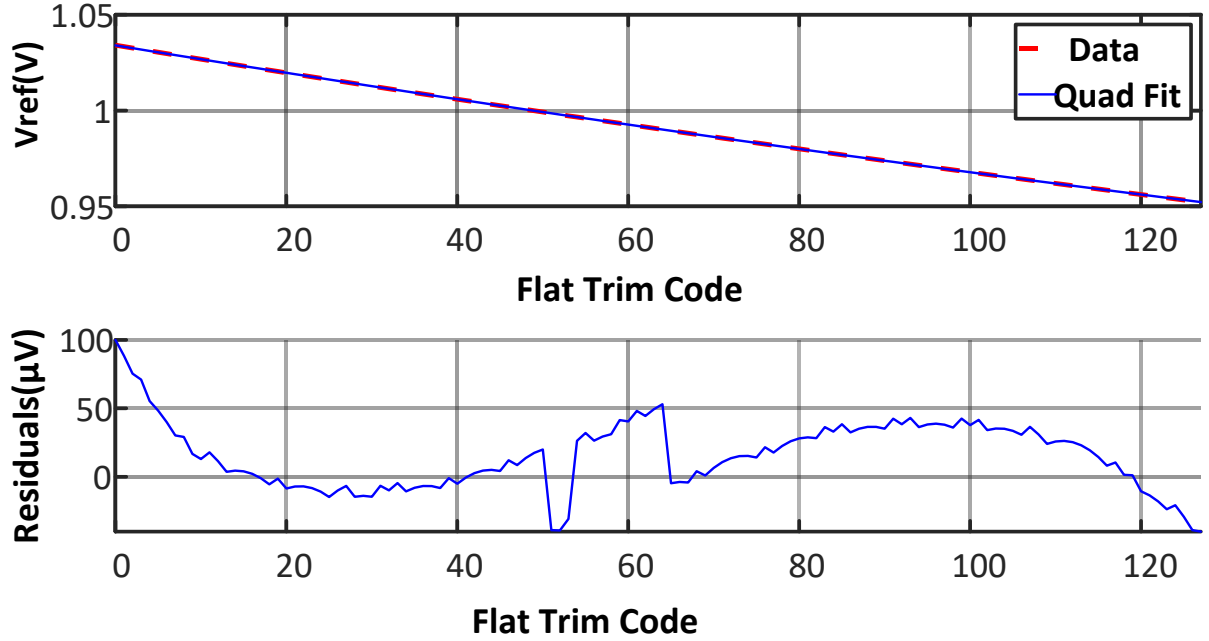


Figure 3.11: Residual error using quadratic equation fit at $T=0^{\circ}\text{C}$.

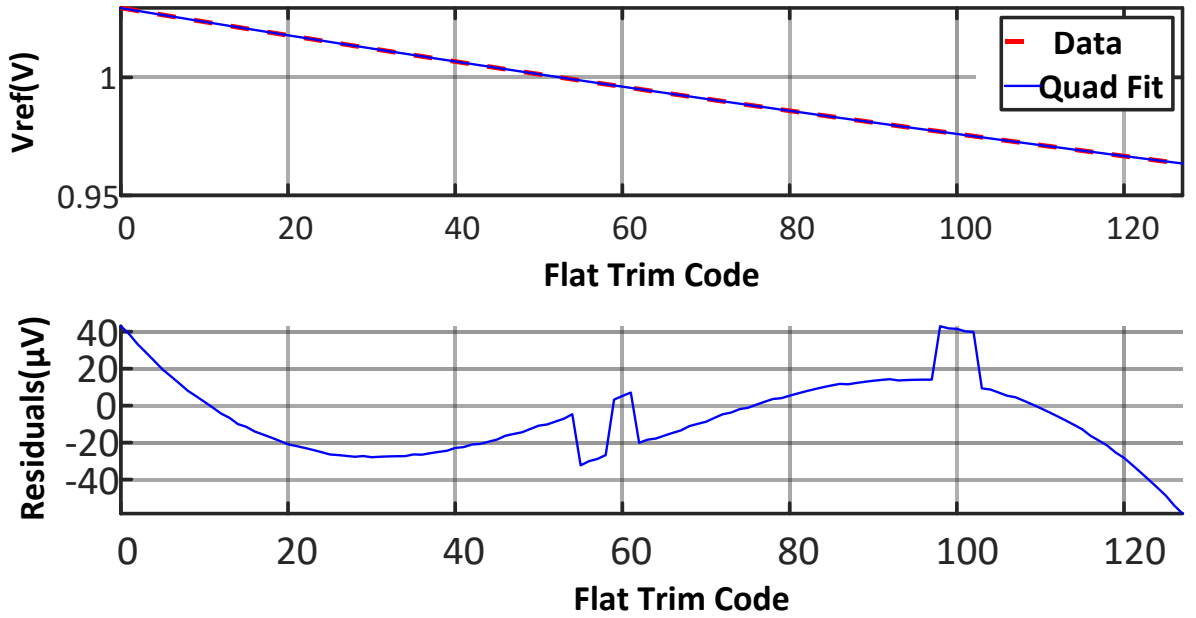


Figure 3.12: Residual error using quadratic equation fit at $T=100^{\circ}\text{C}$.

By storing the six measurements in e-fuses, a precise ‘*temp-co*’ can be set at run-time. Indeed, by recalculating the original quadratic equations, the *flat-trim* code corresponding to the correctly interpolated ‘*temp-co*’ can be selected. This digital processing adds negligible

overhead in a 7-nm FPGA. In the present implementation, the 7-bit *flat-trim* DAC is designed to only provide $-7\text{ mV}/100^\circ\text{C}$ to $+8\text{ mV}/100^\circ\text{C}$ ‘*temp-co*’ range, but this can be extended with negligible area/accuracy penalty.

3.4 Circuit Measurements

The proposed bandgap reference is implemented in 7-nm FinFET and 7 samples were obtained for measurements. All the measurements were done at wafer level and using National Instruments DAQ 6230 [68]. Fig. 3.13 shows the relevant portion of the die micrograph. The circuit, including the digital control and one extra copy of the output voltage branch, occupies 0.078 mm^2 , which is easily absorbed in the FPGA’s floorplan.

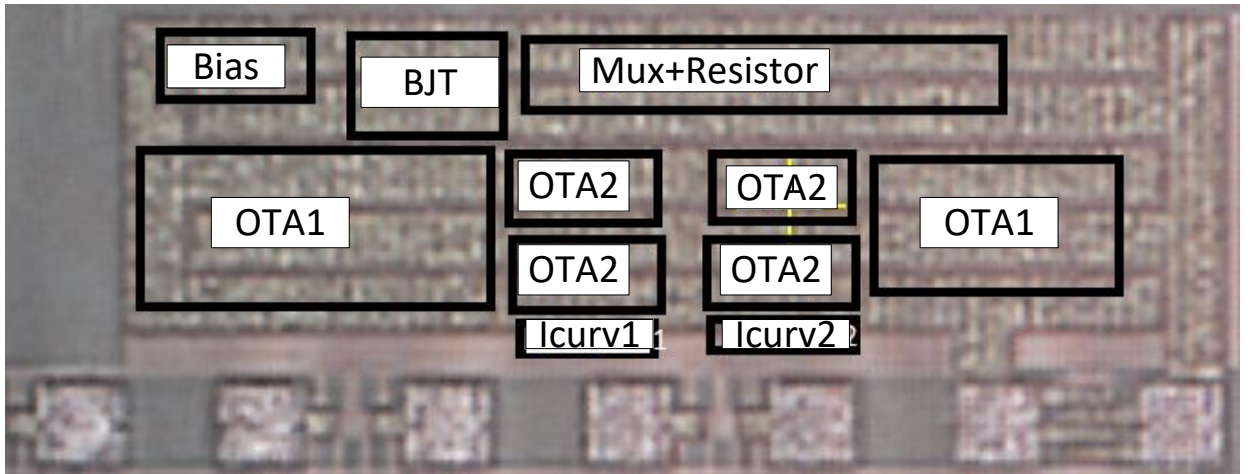


Figure 3.13: Die micrograph of the bandgap reference.

The whole design (including the β -multiplier bias and the two curvature correction schemes) consumes $689\text{ }\mu\text{A}$ at room temperature which is sufficiently low for the FPGA power budget.

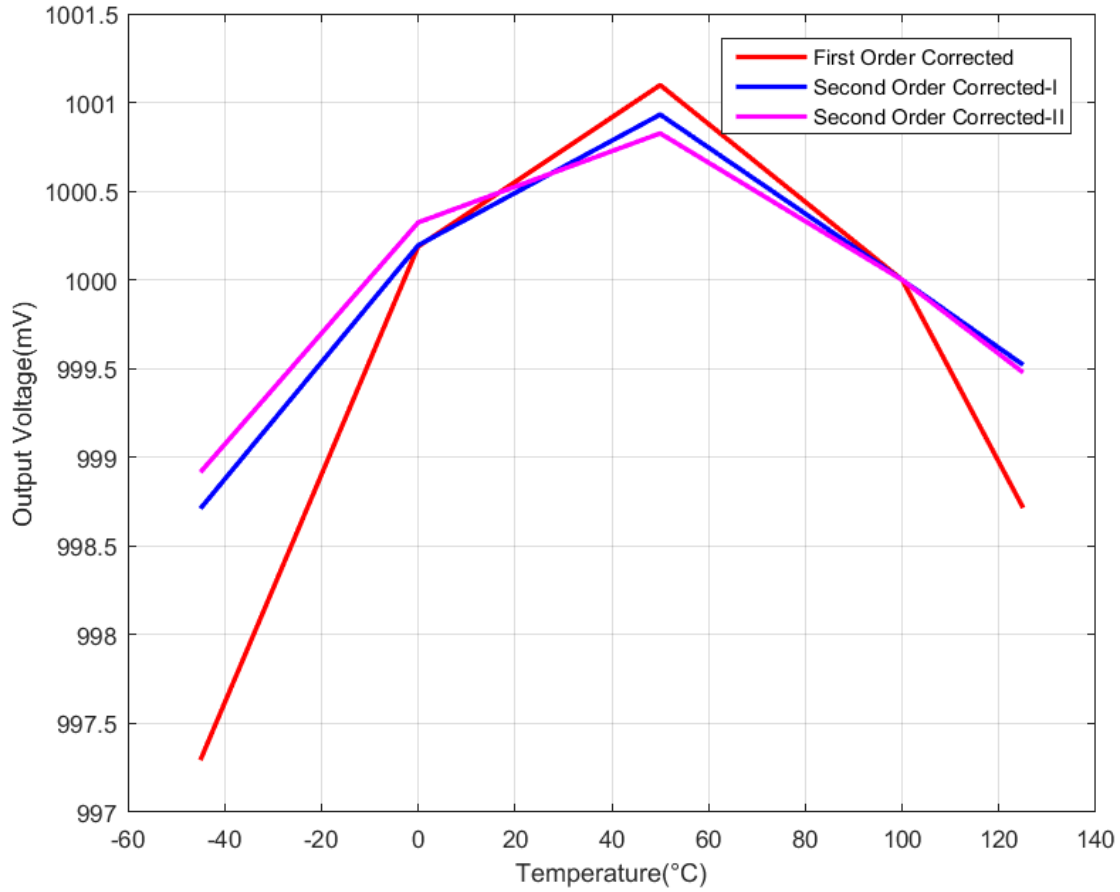


Figure 3.14: Measurement results of post-trim with different compensation techniques.

Figure 3.14 shows measurement comparison of first-order compensated bandgap reference with the two second-order curvature correction techniques. These were measured for one sample by disabling both second-order curvature correction and subsequently enabling each individually. Figure 3.15 shows the complete measurement results over 7 samples when enabling IDAC-based curvature correction. It should be noted that the control settings used for the IDAC-based curvature correction were fixed and not changed between different samples. It shows a maximum inaccuracy of $\pm 0.27\%$ across the complete temperature range.

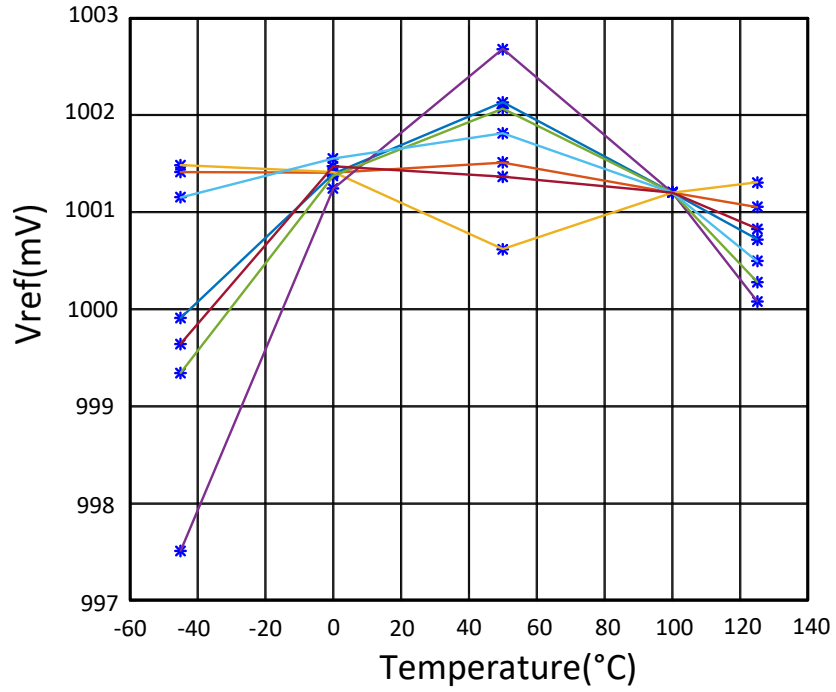


Figure 3.15: Measured output voltage vs. temperature with IDAC-based compensation for 7 samples.

While Fig. 3.16 shows the complete measurement results over 7 samples when enabling BJT-based curvature correction. The control setting used for the BJT diode array selection within the BJT-based curvature correction was fixed across all 7 samples. The maximum inaccuracy is $\pm 0.2\%$ across the complete temperature range. As it can be seen, the BJT-based method provides a slightly better ‘*temp-co*’ by cancellation of nonlinearity as compared to the IDAC-based correction.

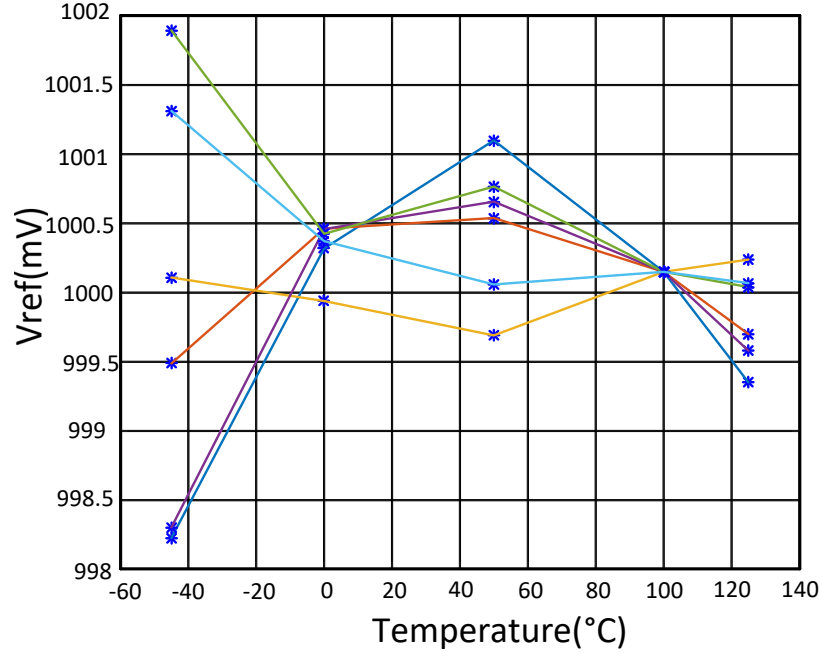


Figure 3.16: Measured output voltage vs. temperature with BJT-based compensation for 7 samples.

The proposed circuit's '*temp-co*' is 6 ppm/°C across the temperature range of 165 °C which is the lowest among the high precision bandgap references. The temperature drift for the reference can be calculated as:

$$V_{\text{ref}}(TD) = TC \cdot TR \quad (3.20)$$

$$V_{\text{ref}}(TD) = 6 \text{ ppm}/^{\circ}\text{C} \cdot 165^{\circ}\text{C} \quad (3.21)$$

$$V_{\text{ref}}(TD) = 990 \text{ ppm} \quad (3.22)$$

where TD= temperature drift, TC= '*temp-co*' and TR= temperature range. For a given ADC with N number of bits, the least significant bit is given by $\frac{1}{2^N}$, and its equivalent in ppm is $\frac{10^6}{2^N}$. This translates to 976 ppm for 10 bit resolution while 1953 ppm for 9 bit resolution requirements. Therefore, based on Eq. (3.22) and above analysis, the bandgap reference can support 9 bits of resolution for an ADC within the full temperature range of 165 °C, while it can be employed for 10 bits of resolution for a limited temperature range.

One of the limitations which caused the degradation in performance is the reduction in headroom associated with the cascodes for current mirror devices M_4 and M_5 . Moreover,

the gain-boosting amplifier for these devices introduces a temperature coefficient when the associated headroom is reduced. This reduction in headroom is a result of the voltage at the top of the resistor ladder R_3 being >1 V, when the target $V_{ref}=1$ V. An alternative design choice is to lower the output voltage (V_{ref}) from the core and thus removing the gain-boosting amplifier. This could help to improve the temperature coefficient as well as reduce the trim range required. The only drawback is that it requires a subsequent gain stage, which can additionally act as a buffer for the reference voltage.

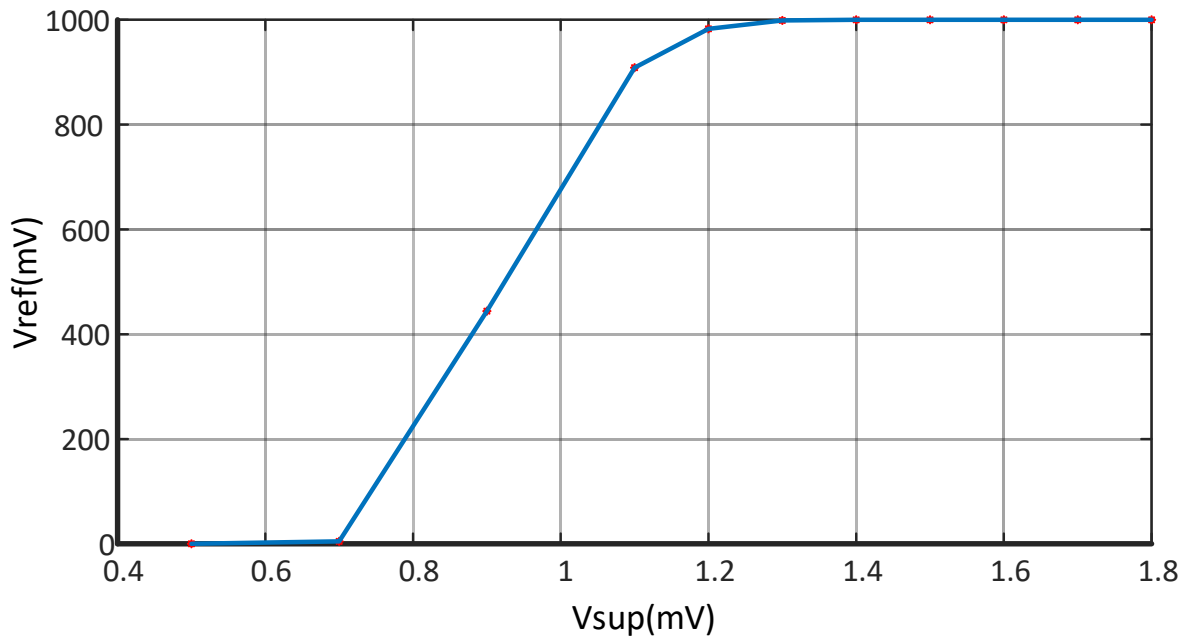


Figure 3.17: Measured supply-sensitivity of the bandgap reference at $T=125^{\circ}\text{C}$.

Figure 3.15 illustrates a max inaccuracy of $\pm 0.27\%$ when using the IDAC-based curvature correction over a temperature range from -45°C to 125°C . Figure 3.16 shows that the BJT-based correction achieves a slightly lower inaccuracy of $\pm 0.2\%$. Figure 3.17 proves the bandgap is functional at supplies $\geq 1.2\text{V}$, which easily meets our design spec of 1.375V .

Measurement results at 125°C show a good line-regulation performance of $0.1\%/V$. Normally, noise behavior and load sensitivity are relevant characteristics of a voltage reference. The motivation of this design was to evaluate the most basic parameters of the bandgap reference (inaccuracy), correlate the simulation models (since the design was done in parallel

with the in-house SPICE model development), and develop the newly proposed digital trimming method. Besides, test-chip was characterized using a probe station (without packaging due to the cost savings). Therefore, the measurement of noise was not part of the test set-up development. Fig. 3.18 and 3.19 show the simulation results for the noise. The application in which the circuit is employed has the source voltage buffered and distributed on-chip. Therefore, it is not required to extensively evaluate load sensitivity. Therefore, these two parameters have not been measured.

The noise simulations were done for the bandgap reference. The noise power spectral density has been plotted in Fig. 3.18.

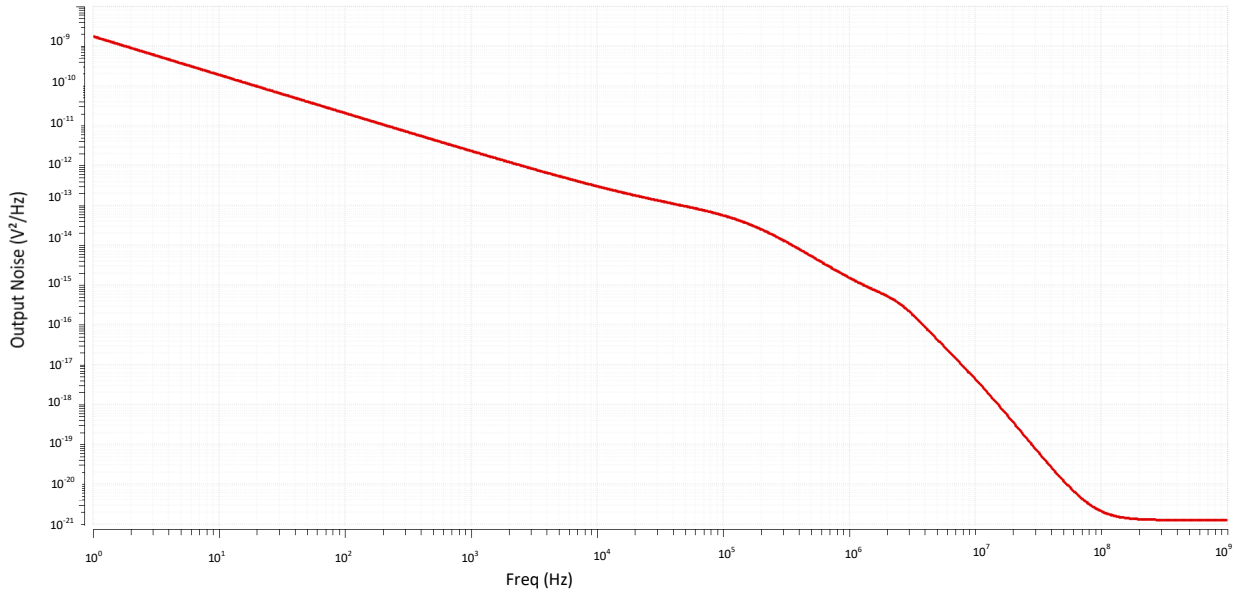


Figure 3.18: Simulated output noise power spectral density.

The integrated noise power spectral density has been plotted in Fig. 3.19. The integrated power spectral density in the range up to 10 Hz is $65 \mu\text{V}$ which is comparable to similar works ([69] [70]) without any additional chopping or noise-mitigation circuit techniques. There have been bandgap references [5] employing chopping which have been shown to reduce noise to $6.1 \mu\text{V}$.

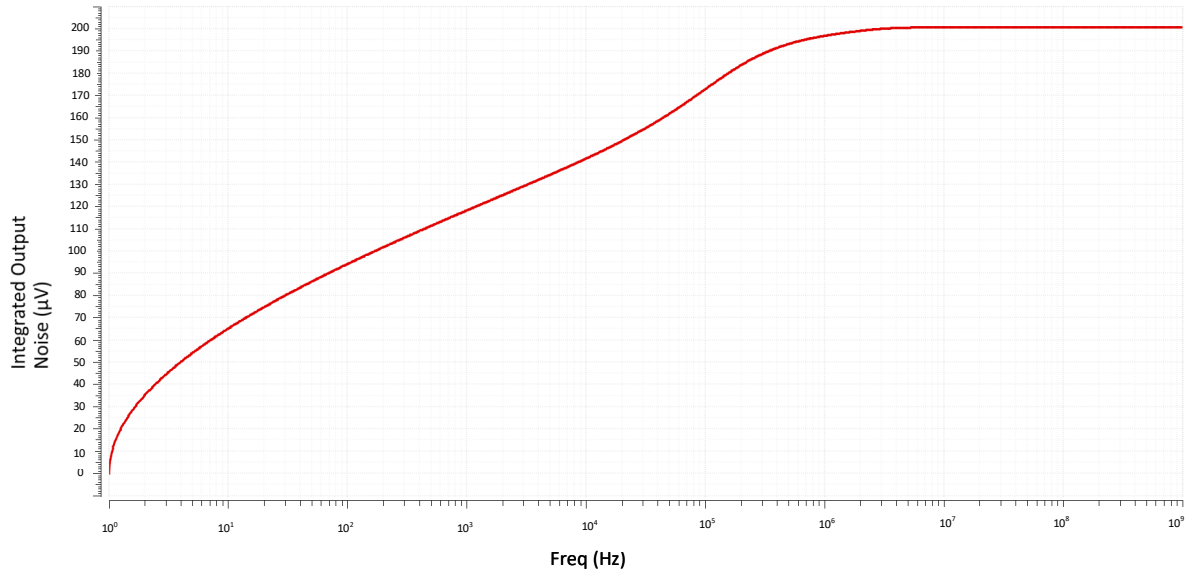


Figure 3.19: Integrated noise at output voltage

The bias current for various sub-blocks, such as amplifiers within the bandgap reference, is provided by a β -multiplier circuit. The nominal current is $10\ \mu\text{A}$ with a positive ‘*temp-co*’ and the measured results are shown in Fig. 3.20.

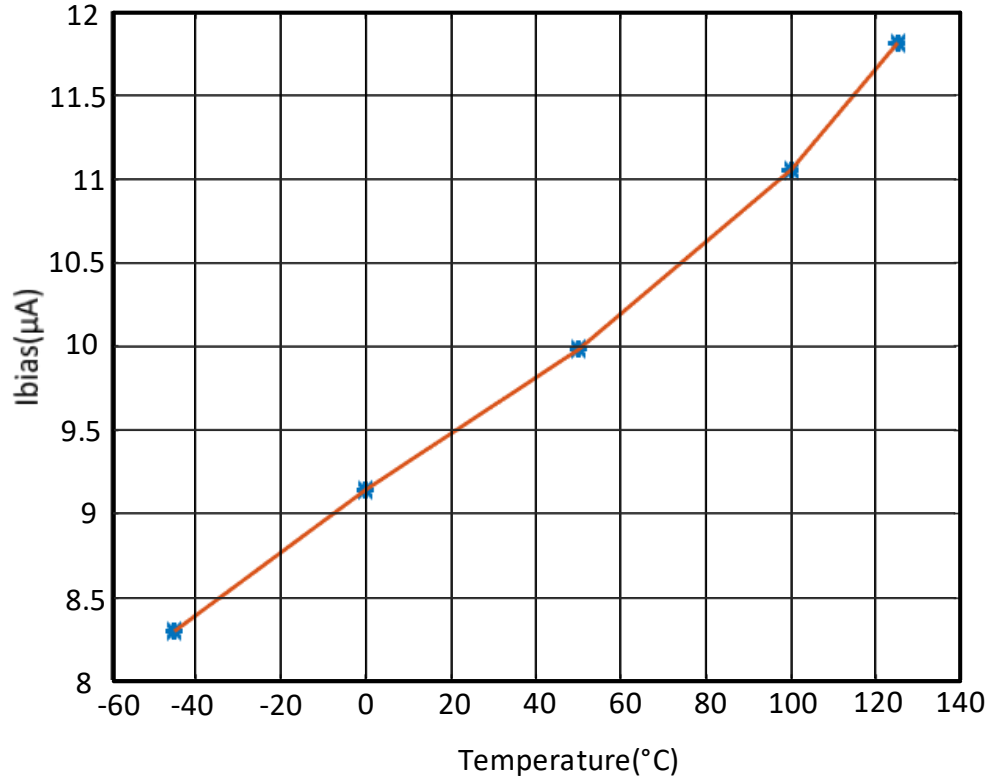


Figure 3.20: Measurement result of β -multiplier circuit.

Another claimed feature of the circuit is the ‘*temp-co*’ adjustment of the output voltage, as described by Fig. 3.9. Based on the six stored values, three at each of the two temperatures during the factory test, the FPGA logic can compute the two waveforms shown in Fig. 3.21. The output voltage (left y-axis) is plotted vs. *flat-trim* code for two different temperatures ($T=0^{\circ}\text{C}$ and 100°C). The difference between them gives the ‘*temp-co*’ ($\text{mV}/100^{\circ}\text{C}$) plotted on the right y-axis. Fig. 3.22 shows the programmability of ‘*temp-co*’ by varying the *flat-trim* code.

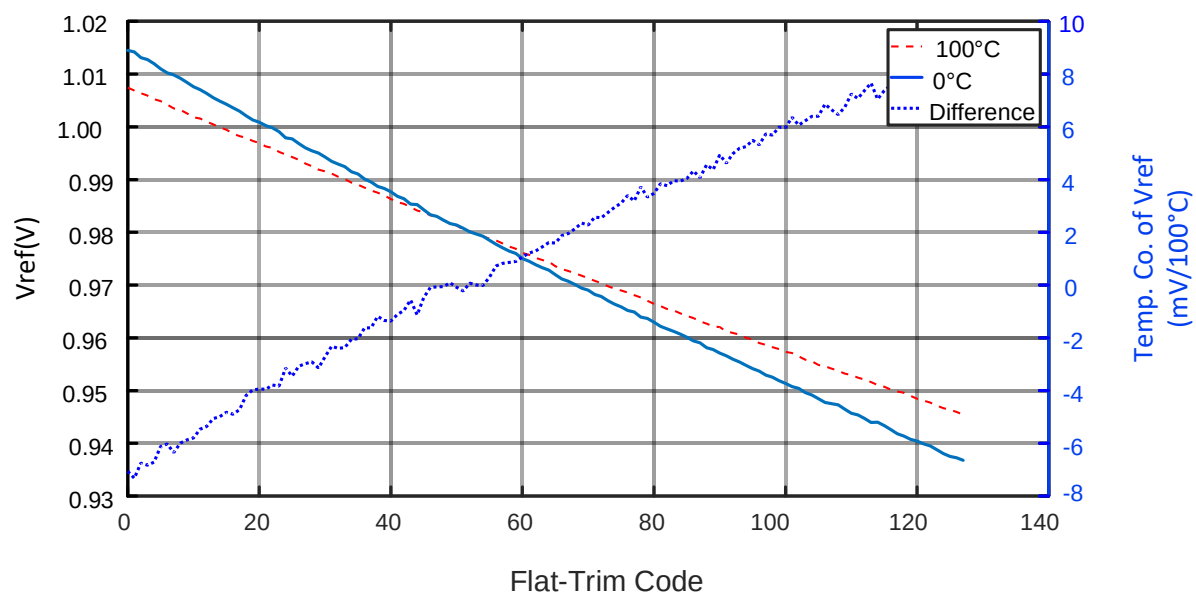


Figure 3.21: Measured V_{ref} and 'temp-co' vs. *flat-trim* code.

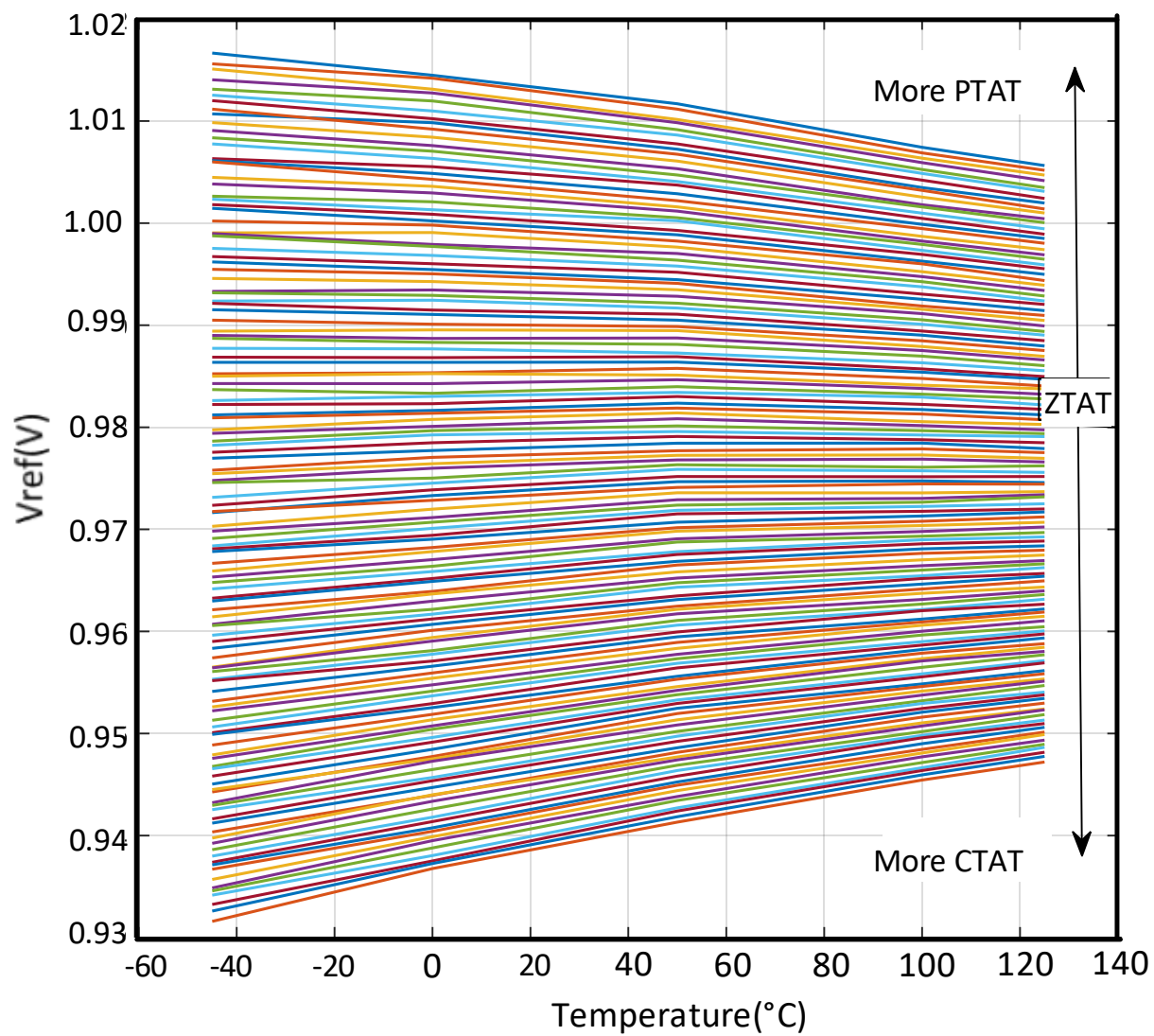


Figure 3.22: Control of voltage '*temp-co*' across different *flat-trim* code.

Table 3.1 summarizes the overall measured performance of the circuit which compares favorably with state-of-the-art ≤ 1 V CMOS voltage references in terms of inaccuracy and ‘*temp-co*’ while also providing the programmability of output voltage ‘*temp-co*’. It is one of the first analog circuit implemented in 7-nm FinFET published [19].

3.5 Conclusion

This chapter introduced an architecture to realize a 1-V bandgap reference with a programmable ‘*temp-co*’ in 7-nm FinFET CMOS. Theoretical analysis on sources of error as well as design techniques to circumvent them has been presented. A digitally assisted robust trim scheme is proposed and a sufficient trim range is provided to handle any deviations from the device models to the silicon. To achieve the target performance, two curvature compensation schemes have been implemented, which can be enabled separately to evaluate their efficacy. Additionally, support circuitry, such as bias generation and start-up, have also been discussed. Finally, measurement results to characterize various metrics of the design have been presented. It shows that the work achieves a maximum inaccuracy of $\pm 0.2\%$ over a temperature range between -45°C to 125°C , which matches well with the state-of-the-art works from the literature.

Table 3.1: Comparison of the proposed reference with prior art

Parameter	This Work	[60] ISSCC'19	[59] VLSI'17	[55] ASSCC'16	[4] VLSI'12	[51] JSSC'11
CMOS Node	7nm FinFET	12nm FinFET	16nm FinFET	16nm FinFET	0.13 μ m	0.16 μ m
Supply Voltage [V]	1.375	0.7	1.62	1.62	0.9	1.62
Output Voltage [V]	1.0	0.235	0.605	0.602	0.615	1.0875
Inaccuracy (max) [%]	$\pm 0.2^a, \pm 0.27^b$	$\pm 2.35^*$	$\pm 1.3^*$	$\pm 0.64^*$	± 0.34	± 0.15
'Temp-co' [ppm/ $^{\circ}$ C]	6-14.7	40.51	-	9-33	30	5-15
Temperature range	-45 $^{\circ}$ C to 125 $^{\circ}$ C	-20 $^{\circ}$ C to 125 $^{\circ}$ C	-40 $^{\circ}$ C to 125 $^{\circ}$ C	-40 $^{\circ}$ C to 125 $^{\circ}$ C	-50 $^{\circ}$ C to 150 $^{\circ}$ C	-40 $^{\circ}$ C to 125 $^{\circ}$ C
Active Area [mm ²]	0.078**		0.011	0.013	0.1	0.12
Current Consumption [μ A]	689**	9.83	189	-	3.9	55
'Temp-co' Programmability	Yes	No	No	No	No	No

^aBJT *curr-corr*, ^bIDAC *curr-corr*, *Untrimmed, **Incl. extra copy of V_{ref} , two curvature corrections

CHAPTER

4

Conclusion

This dissertation presents the design and implementation of a high-precision bandgap voltage reference based on BJT devices in 7 nm FinFET process technology. The semiconductor industry has adopted the FinFET technology to implement high-performance mixed-signal SoCs and FPGAs [19], [52]. Integrated voltage references are based on BJT devices in CMOS. We presented in Chapter 2 the process technology and characterization results of the PNP BJT devices in 7-nm FinFET CMOS which aid in understanding, modeling, and are critical in designing voltage references and temperature sensors. This also provides information on the fundamental limitations posed by the devices and gives the designer optimum choices for circuit-device co-interactions. Parameters, such as non-ideality factor (η), ΔV_{eb} voltage mismatch, and their dependence on current density and temperature, have specifically been discussed in Section 2.4. SPICE models were developed based on this characterization data. Then, a comparison of FinFET BJT with older planar process versions is presented (see Section 2.4). The key contribution of the first part of the thesis is co-optimization of device circuitry to achieve high precision for BJT device-based circuits, such as voltage/current

reference and temperature sensors.

One of the key requirements for a voltage/current reference or temperature sensor is the ability to operate across a wide temperature range, e.g., -55°C to 125°C , while maintaining accuracy. The stringent accuracy requirement in spite of the degradation of the BJT characteristics in FinFET CMOS necessitated postfabrication trimming. There is a trade-off between the targeted accuracy versus the output voltage measured at the number of trim codes for every temperature as well as the number of temperature settings. This translates into the number of trim code bits and the number of different temperature points and, in turn, the time required for the trimming. In the specific case of our design, it was targeted for integration into FPGAs (characterized by a large total silicon area, with digital logic occupying vastly more area than occupied by analog circuitry): Yield is critical and should not be dominated by imperfections in the analog circuitry. In this work, using the 7-nm FinFET, a process with less mature foundry models at the time of the design, required a risk mitigation (trimming) plan from the design conception. Hence, the number of temperature-point trims were not a factor to the first order in this case.

In the second part of the thesis, a voltage reference architecture is presented that achieves a maximum inaccuracy of $\pm 0.2\%$ while allowing for a control of the *temp-co* of the generated voltage. The circuit design was based on the SPICE models developed earlier. Device-circuit co-optimization has led to achieving the targeted maximum inaccuracy of $\pm 0.2\%$ as shown in Fig. 3.16.

4.1 Thesis Contributions

To the best of our knowledge, this work presents the first ever 1 V precision voltage reference in the 7-nm FinFET technology at the time of publication [19]. It is also one of the few available references in the literature for BJT realization in FinFET and its associated modeling, presented from a circuit design perspective. For example, Figs. 2.9 and 2.10 in Section 2.4 provide guidance on the optimum choice of bias current for the BJT to reduce the spread of ΔV_{be} versus temperature.

The BJT device characterization data comparison between planar and FinFET serves as

an overview to the reader. Besides, the presented data provides a reference for the theoretical limit on the precision of BJT-based circuits (current, voltage references) as well as the inaccuracy of sensors (on-chip temperature sensor). For example, Fig. 2.10 in Section 2.4 presented a plot of the spread of ΔV_{be} versus temperature, indicating that the inaccuracy of temperature measurement, without any trimming, using BJT device is on the order of $\pm 2^\circ\text{C}$.

A voltage reference architecture which provides a high precision is revealed in Chapter 3. In addition to its normal operation of providing a temperature-independent voltage reference, the architecture enables, with a very low overhead, a programmable temperature coefficient control of the output voltage. This is especially attractive in applications which require temperature compensation via a custom nonzero *temp-co* voltage reference, e.g., internal clock reference, phase locked loop, voltage-controlled oscillator, LDO. In view of the SoC and FPGA generating large thermal gradients across the die, this feature will be beneficial from a system design perspective in future analog, mixed-signal circuits that need an output that is independent of temperature.

To achieve high precision in spite of the challenges of the scaled technologies, a trim scheme is proposed. Moreover, the trim range was made sufficiently large to cover any tolerance required for the lack of mature BJT device models in 7-nm FinFET process at the commencement of this work. The two-temperature trim removes most of the errors, as was shown in Section 3.3. In addition, the proposed digital assistance scheme only requires three code measurements at each temperature, thus saving the test time with a negligible penalty on the error ($<100\ \mu\text{V}$). Besides, this scheme provides a means to control the temperature co-efficient of the output voltage since all information about the *temp-co* can be deduced from the six trim measurements, three measurements each at two temperatures.

Two second-order curvature correction techniques are implemented, which can be enabled separately in the design. The bandgap reference achieves a max inaccuracy of 0.27% (IDAC approximation correction) and 0.2% (BJT-based correction) across the temperature range of -45°C to 125°C maintaining the *temp-co* flatness of ~ 6 to $14.7\ \text{ppm}/^\circ\text{C}$, with line regulation of $0.1\%/V$. The *temp-co* is digitally adjustable between $-7\ \text{mV}/100^\circ\text{C}$ to $+8\ \text{mV}/100^\circ\text{C}$. These results compare very well with the state-of-the-art performance in voltage references implemented to date.

4.2 Future Research Directions

In this section, we offer possible avenues to improve the current work as well as directions leading to future research. In the current design, the occupied silicon area as well as power consumption were not among the main constraints. However, there are other applications, for example, in IoT sensor nodes or biomedical implantable chips, where silicon area as well as power are the limiting factors. Therefore, a possible direction to explore is to minimize the area and power consumed for such a voltage reference.

4.2.1 Single BJT Based switched-capacitor Bandgap Reference [1]

One direction which can be explored to reduce the area consumed by the BJT is by using a single BJT together with a control scheme and switched-capacitor back-end. This was not explored in this thesis but can be useful especially in deep nano-scale process where switched-capacitor circuits are more amenable compared to the continuous-time analog processing. The core idea, shown in Fig. 4.1, is to produce two emitter-base voltages corresponding to different current densities in the biased BJTs in two phases of a clock. In the first half of the clock cycle, the emitter-base voltage is stored on a capacitor, while in the second half of the clock cycle, the difference between the emitter-base voltage is amplified and added to the previous stored voltage. By choosing the right amplification factor (α), temperature independence can be achieved while an additional division factor (β) can be used to achieve a programmable sub-1 V output. The output voltage of such a scheme is not continuous and can be powered ON for a brief interval periodically, thus making it energy efficient. Moreover, this voltage can be held using a subsequent sample-and-hold stage if a continuous voltage is required by the application [1].

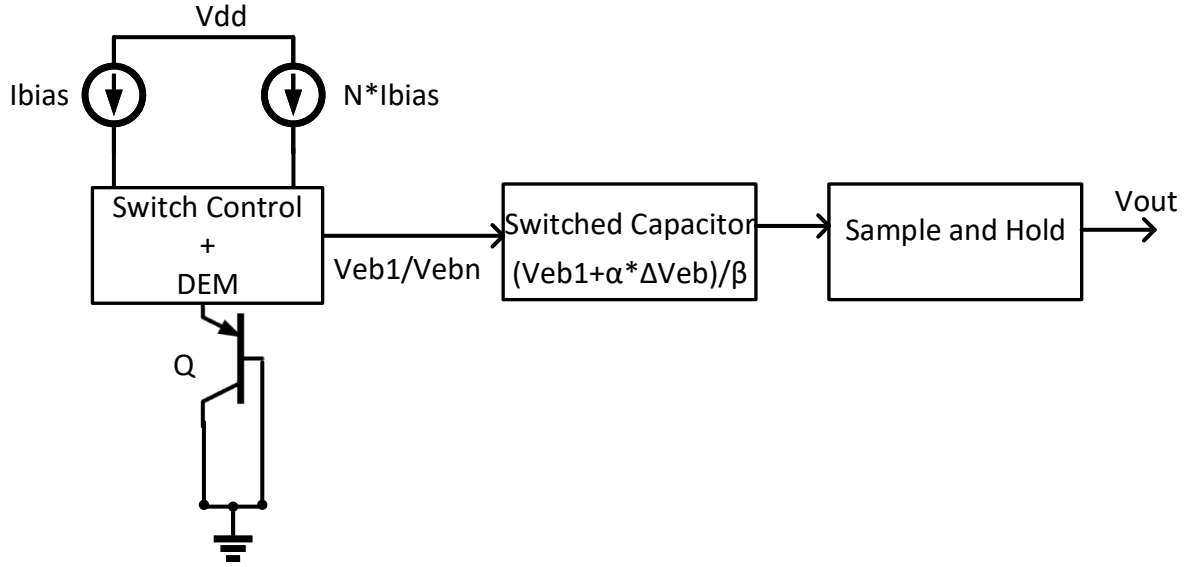


Figure 4.1: Area-efficient scheme to implement a programmable voltage reference.

The area of the BJT and the current mirror used in this work is determined by the mismatch requirement. In the scheme below, since there are switches already controlling the bias current, a dynamic element matching logic can be employed to rotate the use of unit current sources forming the ratiometric (1:N) bias. Dynamic element matching logic covers all possible combinations i.e. $^{N+1}C_1$. By doing so, the mismatch can be reduced to a large extent [71]. A representative timing scheme illustrated using an example of a 1:3 ratio bias current feeding a single BJT is shown in Fig. 4.2. It should be noted that since there is a logarithmic dependence between the bias current and the emitter-base voltage, averaging the emitter-base voltage over four cycles does not result in a reduction of the process mismatch of emitter-base voltage by a factor of $\sqrt{4}$.

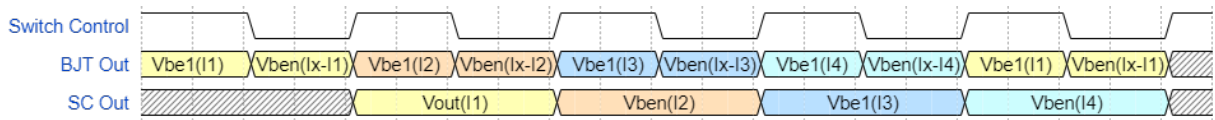


Figure 4.2: Timing waveform for a conceptual switched-capacitor bandgap reference

4.2.2 Single Circuit Providing Dual Functionality [2]

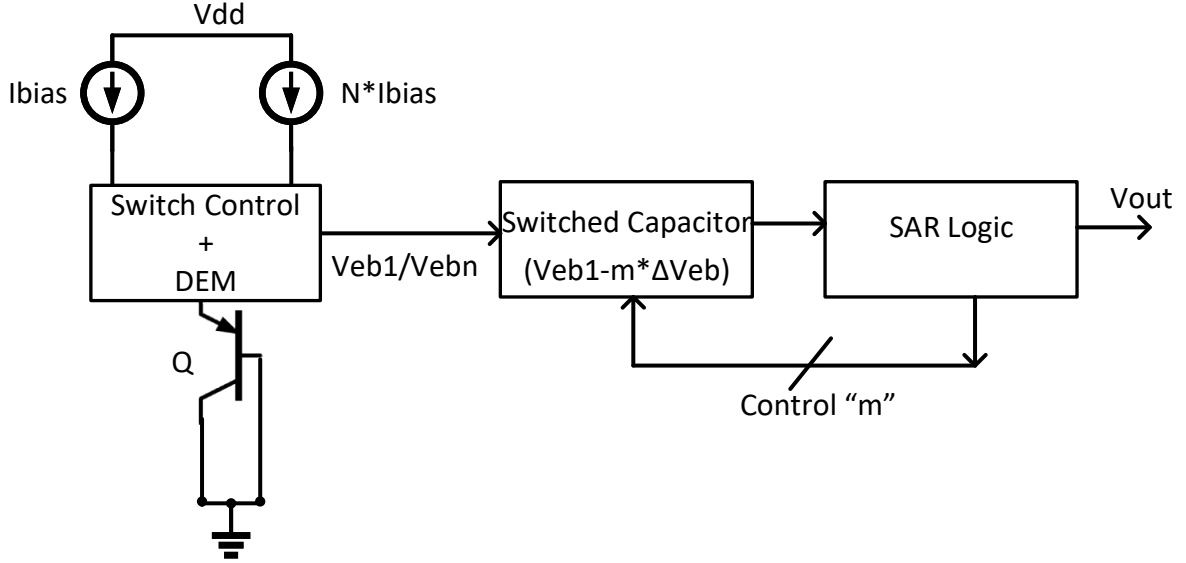


Figure 4.3: Modification of switched-capacitor front-end to realize temperature sensor

In the previous section, the switched-capacitor stage is used to perform the summation $(V_{eb1} + \alpha \cdot \Delta V_{eb})$. An additional improvement towards the area efficiency is to use the same circuit for performing temperature sensing [2]. This is because the voltage reference already has the temperature dependent component (PTAT and CTAT). This can be realized by doing subtraction as shown in Fig. 4.3 instead of the summation, i.e. $V_{eb1} - m \cdot \Delta V_{eb}$. By changing the value of m in the feedback, for example, based on SAR logic, a coarse temperature estimate can be obtained. This can be useful for achieving a medium-resolution thermal sensor for distributed monitoring across an SoC. Therefore, the same circuit block can be configured to provide the functionality of a bandgap reference as well as a coarse thermal sensor, based on the application requirement. This would save both the area as well as provide an energy efficient solution.

4.2.3 Dynamic Offset Correction Techniques

Another aspect, which was not a limiting factor for our application target, was the number of trim temperature points required to achieve the desired precision of the output voltage,

as well as output noise from the bandgap reference. Therefore, we have not implemented techniques to lower offset as well as noise from the bandgap reference in this work. There are known techniques such as chopping to reduce the offset of the feedback amplifier [5]. Dynamic offset correction technique together with an associated one-point temperature trim can possibly be employed to bring the accuracy to a medium precision level, which could be sufficient for certain applications, thus sacrificing accuracy for lower test/trim time and number of temperature trim points.

CHAPTER

5

Appendix

A Matlab model was developed as part of the work to evaluate the trimming techniques and for faster simulations during the architecture development phase. The architecture of the bandgap reference is reproduced again here in Fig. 5.1.

It should be noted that this model was not matched to the simulation results and only served the purpose of evaluating different digitally assisted trimming based on a general model of a bandgap reference based on the summation of the CTAT and PTAT currents as given by the equation below:

$$I_{ctat} = V_{eb1}/R_2, \quad I_{ptat} = \Delta V_{eb}/R_1 \quad (5.1)$$

The output reference voltage is given by Eq. (5.2).

$$V_{ref} = \left(\frac{\Delta V_{eb}}{R_1} + \frac{V_{eb1}}{R_2} \right) \cdot R_3 \quad (5.2)$$

The non-linear component of the emitter-base voltage is modeled as $k \cdot T/q \cdot \ln(T_r/T)$

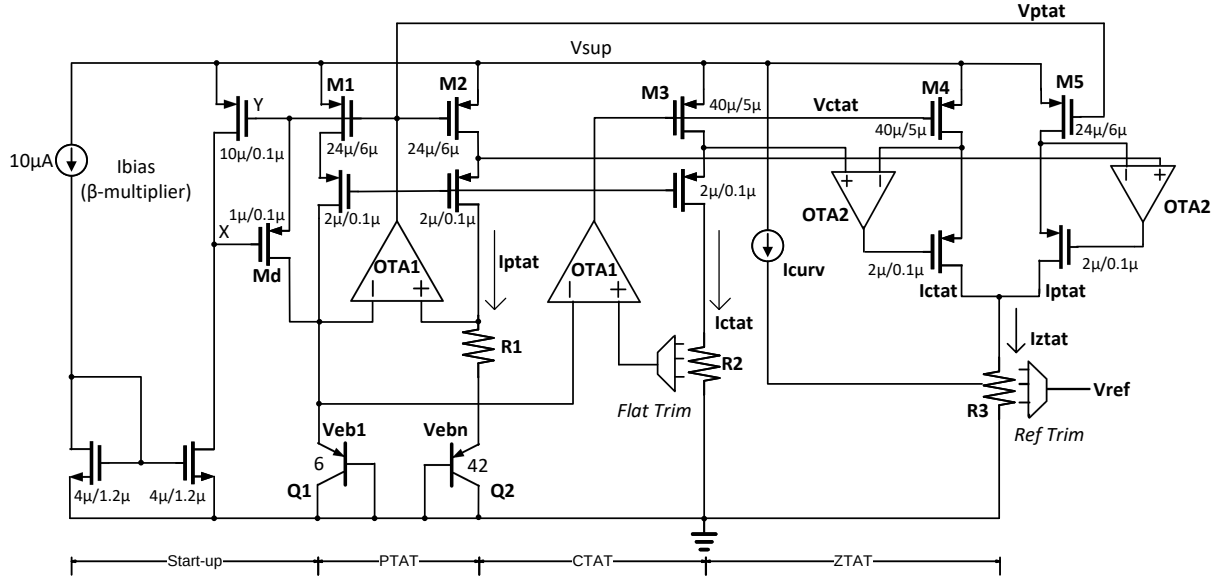


Figure 5.1: Architecture of 1-V bandgap reference with programmable *temp-co*. Note: Biasing circuitry not shown.

where T_r is the reference temperature. The theoretical analysis of this is discussed in detail in Chapter 1. The modeled voltage vs. temperature is shown in Fig. 5.2. In order to model the variation of the CTAT current, a fraction factor ("X") is introduced into the model by multiplying R_2 by the fraction X , where X is varied between 0.6 to 1.1.

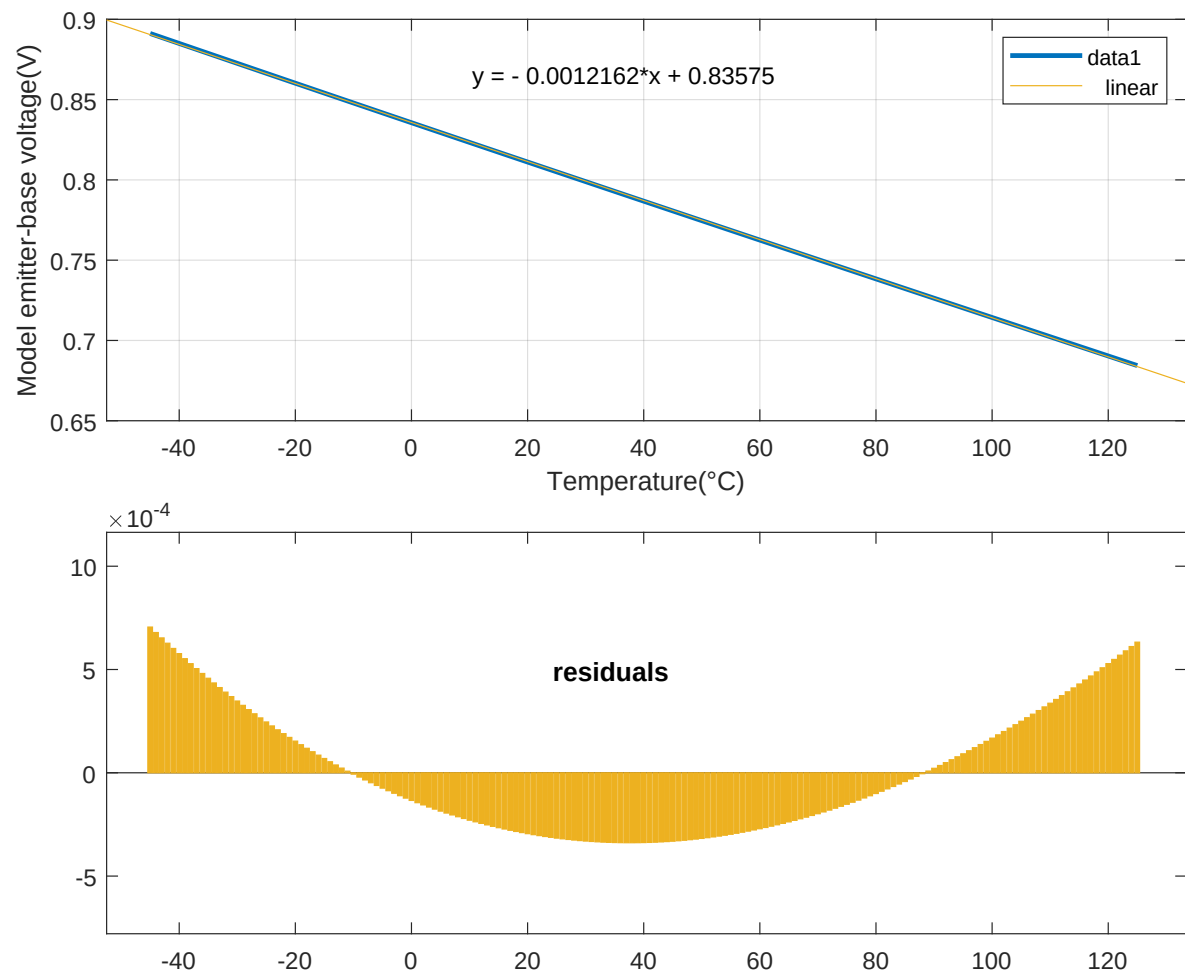


Figure 5.2: Model of emitter-base voltage in Matlab.

The plot in Fig. 5.3 shows the results of output voltage vs. temperature for various fractional values of R_2 .

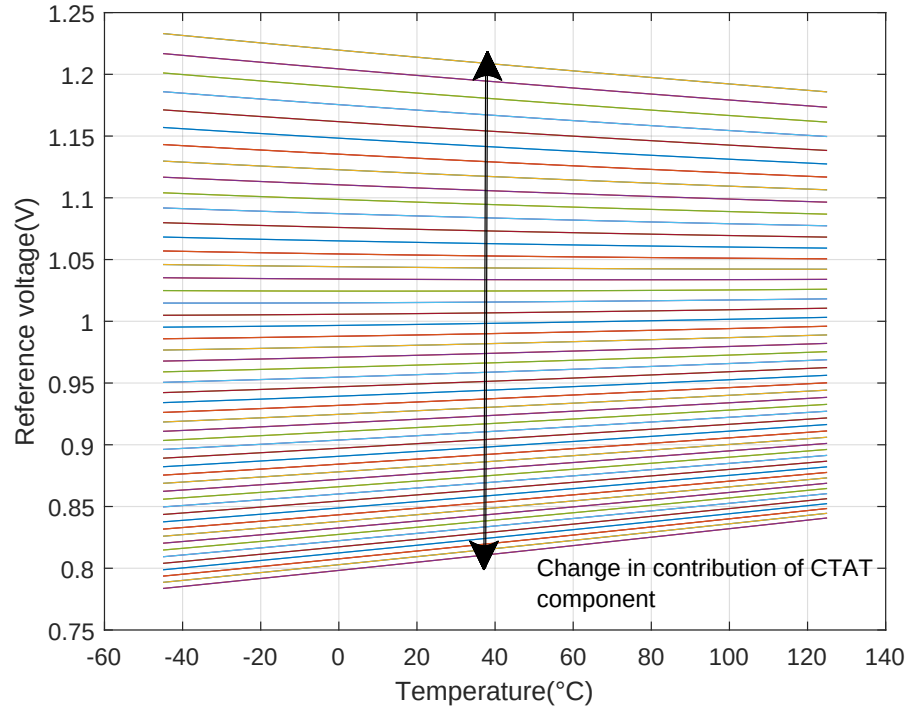


Figure 5.3: Output bandgap voltage for various fractional values of CTAT component with fixed PTAT component.

The trim method used in Fig. 5.4 is explained in Chapter 3. The “Golden Trim Code” representing the flat *'temp-co'* is obtained by evaluating at two temperatures ($T=0^\circ\text{C}$ and 100°C) as shown in Fig. 5.4.

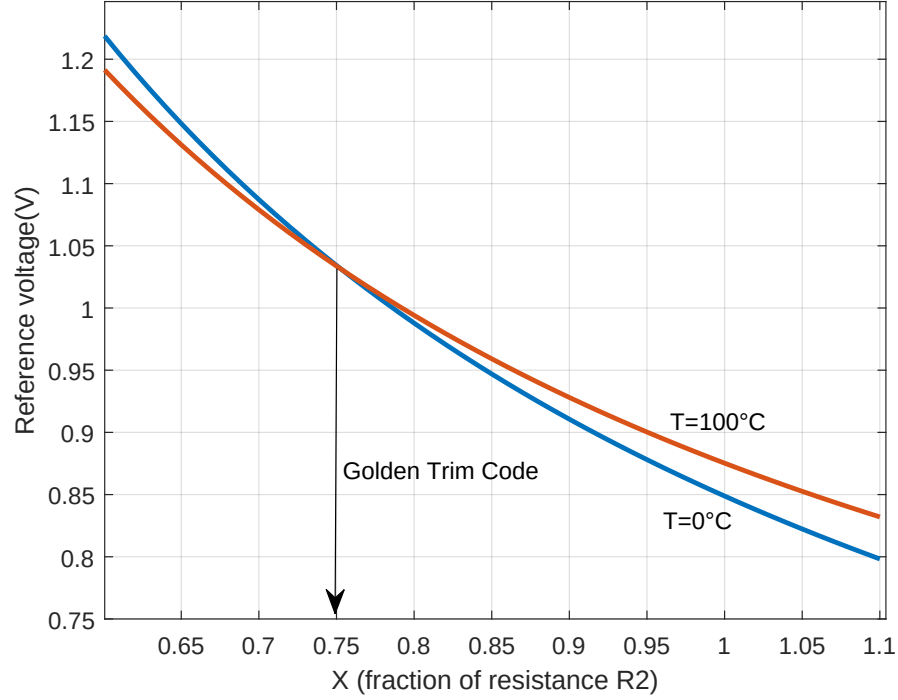


Figure 5.4: Output bandgap voltage at $T=0^\circ\text{C}$ and 100°C as a function of fraction of R_2 .

An important non-ideality which requires to be included in the model is that of the offset of the amplifiers (OTA1) used in the feedback in Fig. 5.1. The offset of OTA1 affects the output voltage since it influences both the generation of PTAT and CTAT currents. It should be noted that the offset of OTA2 used to bias the cascode transistors is expected to be of the second-order effect and hence are is not included in this analysis. Assuming that the offsets of the two amplifiers (OTA1) are represented as " V_{os1} " affecting I_{ptat} and " V_{os2} " affecting I_{ctat} . The output reference voltage is given by Eq. (5.3).

$$V_{ref} = \left(\frac{\Delta V_{eb} + V_{os1}}{R_1} + \frac{V_{eb1} + V_{os2}}{R_2} \right) \cdot R_3 \quad (5.3)$$

Fig. 5.5 shows three different cases as listed below:

Case 1: no offset i.e. $V_{os1}=V_{os2}=0$ (ideal),

Case 2: identical constant offset i.e. $V_{os1} = V_{os2} = +20\text{ mV}$,

Case 3: opposite offsets i.e. $V_{os1} = +20\text{ mV}$, $V_{os2} = -20\text{ mV}$.

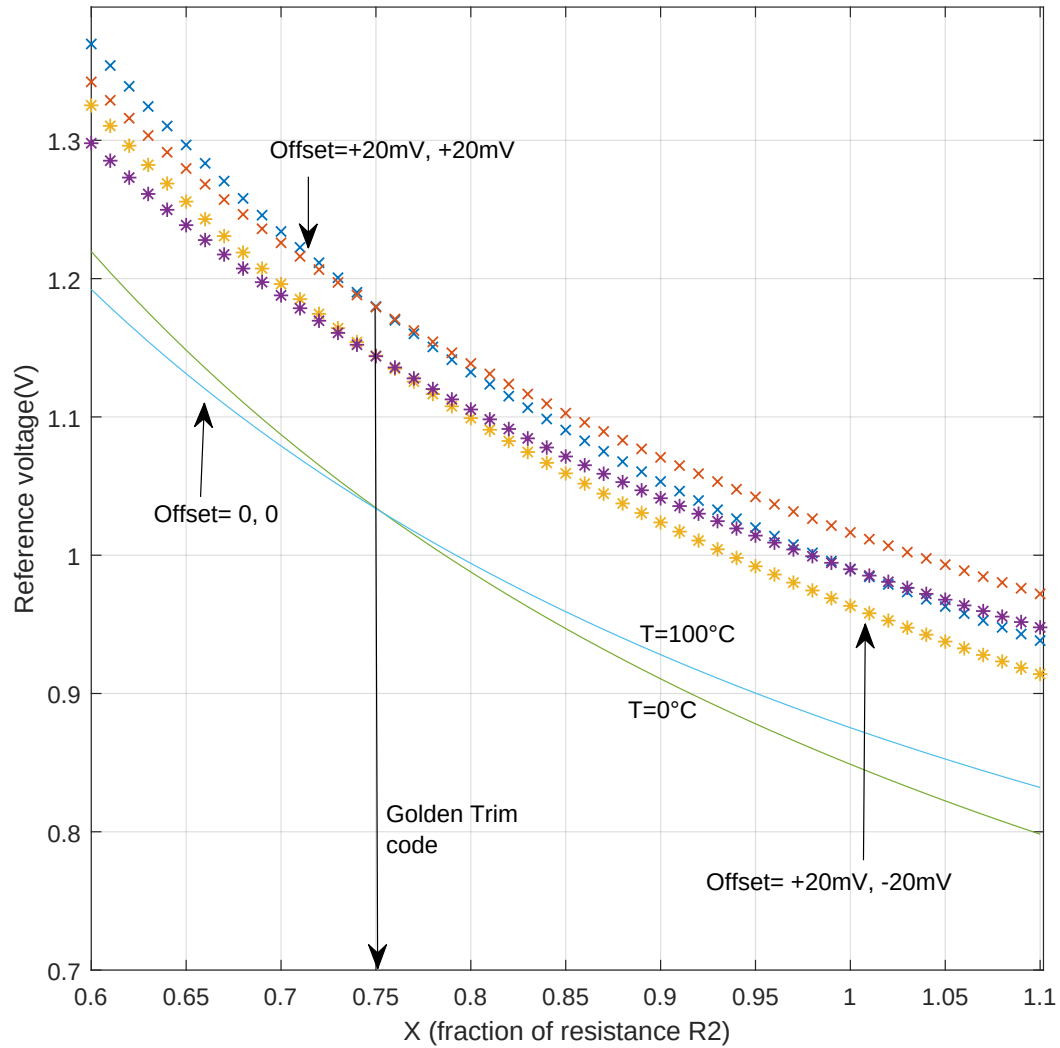


Figure 5.5: Output bandgap voltage at $T=0^\circ\text{C}$ and 100°C as a function of fraction of R_2 with OTA offset.

As can be seen, the resulting “golden trim code” still can be extracted based on the intersection of the $T=0^\circ\text{C}$ and $T=100^\circ\text{C}$ plots. For simplicity, the offset is assumed constant and hence the golden trim code is identical in all three cases. However, in case of additional temperature dependence on offset, the golden trim code shifts, but as long as there is a sufficient trim range, this will be compensated by the proposed trimming technique.

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List of Publications

Journal Papers

- **U. R. Kamath**, E. Cullen, T. Yu, J. Jennings, S. Wu, P. Lim, B. Farley, and R. B. Staszewski, “A 1 V Bandgap Reference in 7-nm FinFET with a Programmable Temperature Coefficient and an Inaccuracy of $\pm 0.2\%$ from -45°C to 125°C ,” *IEEE Journal of Solid State Circuits (JSSC)*, vol. 54, iss. 7, pp. 1830–1840, July 2019. DOI: 10.1109/JSSC.2019.2919134. [[IEEE Xplore link](#)]

Conference Papers

- **U. R. Kamath**, E. Cullen, J. Jennings, I. Cical, D. Walsh, P. Lim, B. Farley, and R. B. Staszewski, “A 1 V Bandgap Reference in 7-nm FinFET with a Programmable Temperature Coefficient and an Inaccuracy of $\pm 0.2\%$ from -45°C to 125°C ,” *IEEE European Solid State Circuits (ESSCIRC)*, sec. A6L-A1, pp. 78–81, 4 Sept. 2018, Dresden, Germany. DOI: 10.1109/ESSCIRC.2018.8494284. [[IEEE Xplore link](#)]
- **U. R. Kamath**, T. Yu, W. Yao, E. Cullen, J. Jennings, S. Wu, P. Lim, B. Farley and R. B. Staszewski, “BJT Device and Circuit Co-Optimization Enabling Bandgap Reference and Temperature Sensing in 7-nm FinFET,” *IEEE European Solid State Device (ESSDERC)*, sec. A6L-E3 pp. 86–89, 4 Sept. 2018, Dresden, Germany. DOI: 10.1109/ESSDERC.2018.8486902. [[IEEE Xplore link](#)]
- B. Vaz, A. Lynam, B. Verbruggen, A. Laraba, C. Mesadri, A. Boumaalif, J. McGrath, **U. R. Kamath**, R. Torre, A. Manlapat, D. Breathnach, C. Erdmann and B. Farley, “A

13b 4GS/s digitally assisted dynamic 3-stage asynchronous pipelined-SAR ADC,” *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 276–277

Patents

- **U. R. Kamath**, J. K. Jennings “Area-efficient high-accuracy bandgap voltage reference circuit,” Patent No. US10054968 , Granted Aug. 2018.
- **U. R. Kamath**, J. K. Jennings, A. Lynam “Circuit for and method of implementing a multifunction output generator,” Patent No. US20180226929A1 , Granted March. 2019.
- A. Lynam, J. K. Jennings, **U. R. Kamath**, M. Hart, J. Karp “Configurable single event latch-up (SEL) and electrical overvoltage stress (EOS) detection circuit,” Patent No. US 10,289,178 , Granted May. 2019.
- **U. R. Kamath**, E. Cullen, J. K. Jennings, “Trim techniques for voltage reference circuits,” Pub. No. US10120399B1, Granted Nov. 2018.
- **U. R. Kamath**, J. K. Jennings, E. Cullen, I. Cical, D. Walsh “Programmable temperature coefficient analog second-order curvature compensated voltage reference ,” Pub. No. US10290330B1, Granted May. 2019.
- **U. R. Kamath**, P. Kelly, J. K. Jennings “Dynamic element matching in an integrated circuit,” Patent No. US20180356294A1 , Granted Jan. 2020.
- **U. R. Kamath**, D. Collins, E. Cullen, “Control circuit for and method of controlling an operation of an integrated circuit device,” Pub. No. US10680583, Granted Jun. 2020.

Chip Micrograph Gallery

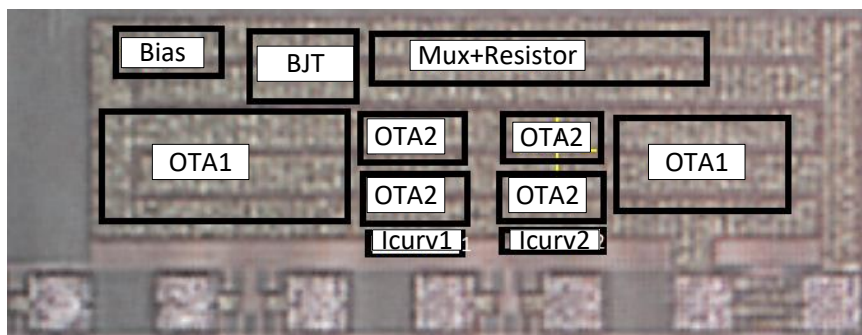


Figure 5.6: Die micrograph of the bandgap reference published at JSSC'19, ESSCIRC'18 and ESSDERC'18.

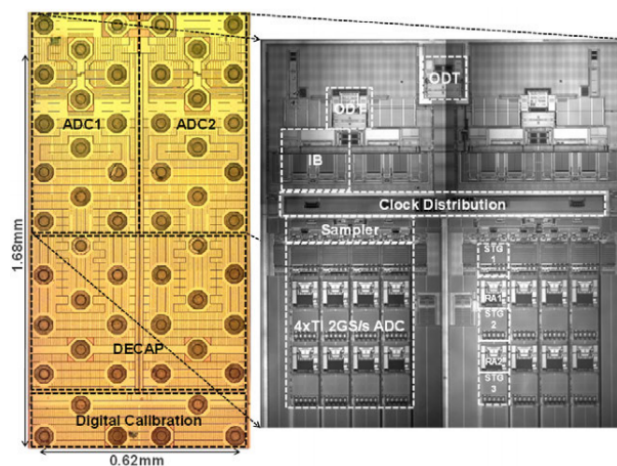


Figure 5.7: Die micrograph of the pipelined SAR-ADC published at ISSCC'17. (I was one of the co-authors for that work.)

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