Adaptive semiblind background calibration of timing mismatches in a two-channel time-interleaved analog-to-digital converter

Sujuan Liu[1] · Ning Lv[1] · Haixiao Ma[1] · Anding Zhu[2]

Abstract This paper introduces an adaptive semiblind background calibration of timing mismatches in a two-channel time-interleaved analog-to-digital converter (TIADC). By injecting a test tone at the frequency of half the overall sampling frequency of TIADC, the timing mismatch between two sub-ADCs can be quickly estimated with great accuracy without affecting the normal operation of the TIADC. The estimated coefficient can then be used in compensation module formed by a fixed structure to calibrate the timing mismatches. Simulation results demonstrate the effectiveness of the proposed estimation and correction technique.

Keywords Time-interleaved analog-to-digital converter (TIADC) · Timing mismatches · Calibration · Semiblind · Test tone

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1 Introduction

It is very difficult to achieve high sampling frequency and high resolution simultaneously in a single analog-to-digital converter (ADC) with the current Complementary Metal Oxide Semiconductor (CMOS) process. The time-interleaved (TI) ADC, first proposed by Black [1], parallelizes multiple sub-ADCs to increase the overall sampling frequency. For instance, a TIADC operates at a sampling rate of f_s by utilizing M sub-ADCs running at a sampling rate of f_s/M in the time multiplexing fashion. One of the main challenges in designing such time interleaved ADCs is that the performance is often degraded by mismatches between the component sub-ADCs, e.g., DC offset, gain mismatch and sampling time skew/mismatches [2]. Among these mismatches, gain and offset mismatches are relatively easy to calibrate, but removing timing mismatches is challenging.

Many calibration techniques have been developed in the past. Foreground calibration typically injects a known testing signal into the system for distortion estimation. Based on the equivalent signal recombination, a training signal is used during the calibration process to realize adaptive calibration of channel mismatches in TIADC in [3]. The foreground calibration method has the advantage of high estimation accuracy and simple structure but at the cost of the normal operation of TIADC being interrupted.

Blind calibration, on the other hand, can track slowly time-varying mismatches without stopping the normal operation of the ADC. However, many restrictive conditions are demanded. The estimation process requires a large number of samples to acquire the relevant parameters and hence the convergence speed becomes slow. In addition, blind methods typically require higher complexity in implementation. An adaptive background estimation for

static nonlinearity mismatches in a two-channel TIADCs is proposed in [4] where a normalized least-mean-square (N-LMS) algorithm is used to blindly identify the polynomial-represented nonlinearity mismatches. In [6], by representing frequency response mismatches as polynomials and utilizing the FxLMS algorithm frequency response mismatches in a two-channel TIADC are calibrated.

Comparing between the foreground and the blind calibration methods, each one has its own advantages and disadvantages. As a tradeoff, semiblind calibration has been proposed recently. Based on injecting a known signal during estimation, an iterative structure for online calibration is proposed in [7], which allows a faster convergence speed but a relatively large computational complexity is required. A semiblind method for calibrating bandwidth mismatches is presented in [8] under the condition that some restrictions are required on input signal.

In this paper, a semiblind calibration method is proposed based on injecting a test tone into the input signal. The test tone has the frequency of half the overall sampling frequency of the TIADC and is used to estimate the timing mismatch between the two channels in the TIADC. The estimated parameter will then be used to correct the timing errors in compensation module.

This paper is organized as follows. The TIADC system structure and compensation principle are presented in Sect. 2. The parameter estimation and system calibration process are given in Sect. 3. The simulation results are presented in Sect. 4 with a conclusion in Sect. 5.

2 System model and compensation principle

In this work, we assume that the gain and offset mismatches can be calibrated separately and we thus focus on the calibration of timing mismatches only. The system model of a two-channel TIADC is given in Fig. 1, where $x(t)$ represents analog input, and $y_0[n]$ and $y_1[n]$ represents the digital output of ADC#0 and ADC#1 respectively. The final output of the TIADC is $y[n]$ and T_s is the overall sampling period of the TIADC and f_s is the overall sampling frequency of the TIADC. Whereas r_0 and r_1 represent the relative timing errors related to T_s of the first channel and the second channel respectively. Ideally, if no timing errors occurs, $r_0 = r_1 = 0$, but in practice, $r_0 \neq r_1 \neq 0$.

Let's consider the input signal to the TIADC is band-limited, namely, $X(j\Omega) = 0$ for $|\Omega| \geq B$, and $B \leq \pi/T_s$. The discrete-time Fourier transform (DTFT) of the output $y[n]$ with timing errors, as shown in Fig. 1, is given by [5]

$$Y(e^{j\omega}) = \sum_{k=0}^{1} \alpha_k\left(e^{j(\omega-k\pi)}\right) X\left(e^{j(\omega-k\pi)}\right) \tag{1}$$

where

$$\alpha_k(e^{j\omega}) = \frac{1}{2}\sum_{m=0}^{1} e^{r_m H_d(e^{j\omega})} e^{-jk\pi m} \tag{2}$$

Applying the first order Taylor's series approximation to the term $e^{r_m H_d(e^{j\omega})}$, we obtain

$$e^{r_m H_d(e^{j\omega})} \approx 1 + r_m H_d(e^{j\omega}) \tag{3}$$

Since

$$H_d(e^{j\omega}) = j\omega \quad \text{for} \quad -\pi < \omega < \pi \tag{4}$$

thus

$$e^{r_m H_d(e^{j\omega})} \approx 1 + r_m j\omega \tag{5}$$

Substitute (5) in (1), we can obtain the output $y[n]$ in the time domain as

$$y[n] \approx x[n] + \hat{e}[n] \tag{6}$$

and

$$\hat{e}[n] = (-1)^n y[n] * h_d[n] \frac{1}{2}(r_0 - r_1) \tag{7}$$

where $h_d[n]$ is the impulse response of $H_d(e^{j\omega})$.

From (7), we can see that we can calculate $\hat{e}[n]$ if we know the value of $(r_0 - r_1)$ and subtract $\hat{e}[n]$ from $y[n]$ in (6), we can obtain the calibrated output $\hat{x}[n]$:

$$\hat{x}[n] = y[n] - \hat{e}[n] \approx x[n] \tag{8}$$

The structure of compensation module is shown in Fig. 2, where a differentiator is represented by $j\omega$ and D_d is the delay of the differentiator.

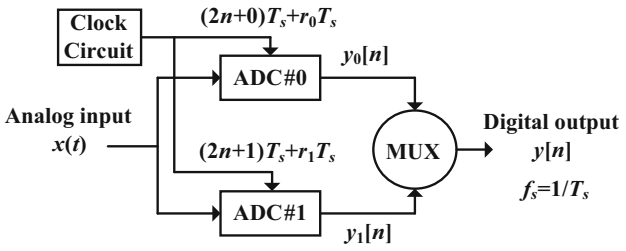

Fig. 1 Model of a two-channel TIADC with timing errors

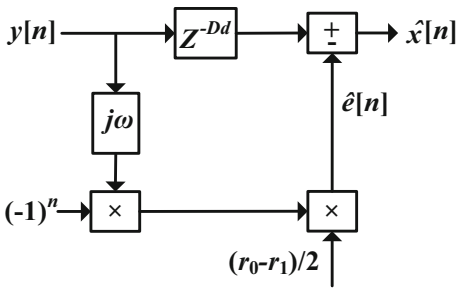

Fig. 2 The structure of compensation module

3 Parameter estimation and digital calibration

In this work, we assume that the input signal should have no spectral information out of the frequency band $[\varepsilon\pi, (1-\varepsilon)\pi]$ for $0 < \varepsilon < 1$. This constraint can be satisfied in a wide class of communication signals, such as DSL or UWB signals [8]. Even if this requirement cannot be met, a frequency shift method can be used to move the input signal into the required frequency band before it is calibrated. After calibration, a reverse frequency shift is used to move it back.

To find the value of $(r_0 - r_1)$, we propose a semiblind estimation method. We inject a test signal $x_t(t)$ which has the frequency of half the overall sampling frequency of TIADC, namely $f_t = f_s/2$. The magnitude response of the input signal $x(t)$ and the test signal $x_t(t)$ is shown in Fig. 3(a). The input signal is sampled by the two-channel TIADC and the sampled output of each sub-ADC is aliasing if the input signal frequency is beyond the Nyquist bandwidth of sub-ADC. The magnitude response of the alias band caused by the input signal and the test signal is shown in Fig. 3(b). As shown in Fig. 3(b), the alias component caused by the input signal will not exceed the frequency band $[\varepsilon\pi, (1-\varepsilon)\pi]$ and the alias component caused by the test signal is at zero frequency. Therefore a low-pass filter can be used to get the aliasing caused by the test signal from the sampled output of sub-ADC. Here the test signal we use is a sine wave. We assume that sampling happens at the rising edge of the clock. In an ideal case, when the sine wave ascends, it is sampled at zero crossing by ADC#0 and when the sine wave descends, it is sampled at zero crossing by ADC#1. When there is a timing error in the system such as a delay in the sampling clock, the real sampling value will not be zero, as shown in Fig. 4.

As the timing error is usually much smaller than the sampling period, and the test signal is almost linear around the zero crossing, the sampling case can be approximated to be a straight line around the sampling point. If the gradient at zero crossing and the sampled value of the test signal can be known, the timing error can be estimated.

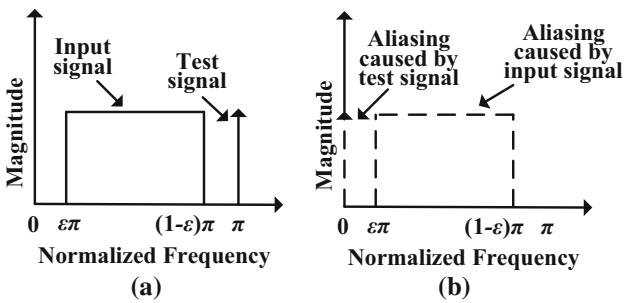

Fig. 3 The magnitude response **a** of the input signal combined with a test signal and **b** of aliasing caused by the input signal and test signal

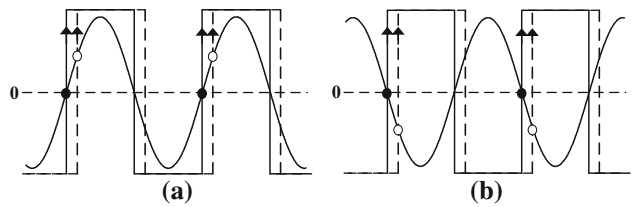

Fig. 4 The ideal sampling and the real sampling with timing error of the test signal for **a** ADC#0 and **b** ADC#1. Ideal clock *line*; clock with timing error *dashed line*; ideal sampling *filled circle*; sampling with timing error *open circle*

$$t_0 = \frac{s(n)}{G_0} \tag{9}$$

$$t_1 = \frac{s(n+1)}{G_1} \tag{10}$$

where t_0 and t_1 mean the absolute timing errors of ADC#0 and ADC#1, $s(n)$ and $s(n+1)$ represent the sampled values of ADC#0 and ADC#1 respectively, G_0 and G_1 are the gradients of the test signal at each zero crossings respectively. The approximated ideal sampling and the real sampling with timing error of the test signal of ADC#0 and ADC#1 is shown in Fig. 5.

According to Fig. 5, we can obtain the function representations of the sine wave for ADC#0 and ADC#1:

$$s(n) = A\sin(2\pi f_t t + 2n\pi) \tag{11}$$

$$s(n+1) = A\sin(2\pi f_t t + (2n+1)\pi) \tag{12}$$

where A and f_t are the amplitude and frequency of the sine wave respectively. The gradient at the zero crossing can be acquired by the derivative of the sine wave at the zero crossing:

$$\begin{aligned} G_0 = s(n)'\big|_{t=0} &= A\sin(2\pi f_t t + 2n\pi)'\big|_{t=0} \\ &= 2\pi f_t A\cos(2\pi f_t t + 2n\pi)\big|_{t=0} = 2\pi f_t A \end{aligned} \tag{13}$$

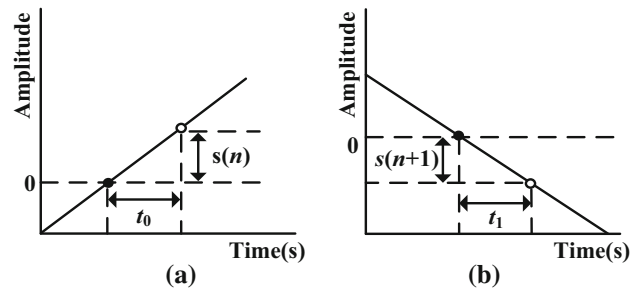

Fig. 5 The approximated ideal sampling and the real sampling with timing error of the test signal for **a** ADC#0 and **b** ADC#1. Ideal sampling *filled circle*; sampling with timing error *open circle*

$$G_1 = s(n+1)'\big|_{t=0} = A\sin(2\pi f_t t + (2n+1)\pi)'\big|_{t=0} = 2\pi f_t A\cos(2\pi f_t t + (2n+1)\pi)|_{t=0} = -2\pi f_t A \tag{14}$$

After substituting (13) into (9) and (14) into (10), we can get:

$$t_0 = \frac{s(n)}{2\pi f_t A} \tag{15}$$

$$t_1 = \frac{s(n+1)}{-2\pi f_t A} \tag{16}$$

The relative timing errors r_0 and r_1 are the results of t_0 and t_1 divided respectively by the overall sampling period T_s:

$$r_0 = \frac{t_0}{T_s} = t_0 f_s = \frac{s(n)}{2\pi f_t A} f_s = \frac{s(n)}{2\pi f_t A} 2f_t = \frac{s(n)}{\pi A} \tag{17}$$

$$r_1 = \frac{t_1}{T_s} = t_1 f_s = \frac{s(n+1)}{-2\pi f_t A} f_s = \frac{s(n+1)}{-2\pi f_t A} 2f_t = \frac{s(n+1)}{-\pi A} \tag{18}$$

According to (17) and (18), the coefficient to be estimated can be represented as:

$$\frac{1}{2}(r_0 - r_1) = \frac{1}{2}\left(\frac{s(n)}{\pi A} + \frac{s(n+1)}{\pi A}\right) = \frac{s(n) + s(n+1)}{2\pi A} \tag{19}$$

According to (19), the structure of the estimation module is shown in Fig. 6. In Fig. 6, ALP0 and ALP1 represent the low-pass filters for ADC#0 and ADC#1. The sampling value of the test signal is obtained by filtering the output of ADC#0 and ADC#1 through the low-pass filters. And the low-pass filters operate at the frequency of half the overall sampling frequency of TIADC. After filtering, $y_{L0}[n]$ and $y_{L1}[n]$ are the filtered outputs of ALP0 and ALP1 which represent the sampled values of the test signal for ADC#0 and ADC#1 respectively and we can get $(r_0 - r_1)/2$, which can be used to get the timing error $\hat{e}[n]$ [cf. Fig. 2 and Eq. (7)]. We know the values of the coefficients are associated with the sampled values of ADC#0 and ADC#1, i.e., $s(n)$ and $s(n+1)$. Whenever the timing mismatches are changed, which occur in practice due to temperature variations etc., the values of $s(n)$ and $s(n+1)$ are also changed, the new value of the coefficient can be computed according to (19).

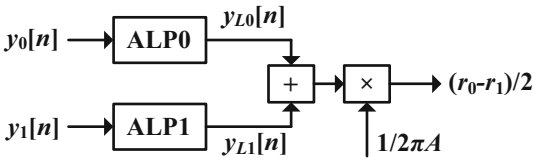

Fig. 6 The structure of the estimation module

To remove the test signal from the digital output, a preprocessing procedure can be conducted. We can first upsample the test signal obtained from both sub-ADC ADC#0 and ADC#1 by a factor two. Add the upsampled output from ADC#0 and the delayed upsampled output from ADC#1, we can get the digital sample of the test signal $x_t[n]$ for the TIADC system. The signal can then be subtracted from the uncalibrated output of TIADC $y[n] + x_t[n]$ so that the test signal can be removed from the digital output The block diagram of the preprocessing module is shown in Fig. 7, where D means the delay of the low-pass filter. Compared with the method in [8], a band-pass filter to remove the test signal from the calibrated output can be avoided.

4 Simulation results

To validate the proposed approach, a complete simulation model is constructed in MATLAB, as shown in Fig. 8. The TIADC system includes time mismatch estimation, preprocessing and compensation calibration. The estimation module operates at the frequency of half the overall sampling frequency of TIADC and the compensation module works at the same frequency with the overall sampling frequency of TIADC. An upsampler is used between estimation and compensation modules. The differentiator and the low-pass filters ALP0 and ALP1 were designed by the MATLAB function "fdatool." The order of the differentiator was 60 and of the low-pass filter was 50.

4.1 Preprocessing

In the simulation, a multi-tone input signal consisting of 5 sinusoids was employed and the bandwidth of the input signal can reach 0.85π. Two idealized ADC quantizers with 12 bits were used. Moreover, the test signal was a sine wave and its frequency was half the overall sampling frequency of TIADC. The relative timing errors for ADC#0 and ADC#1 were 0.02 and −0.01 respectively. We have taken 65,536 samples and the spectrum of the input signal combined with the test signal and of the output after preprocessing is shown in Fig. 9. In Fig. 9(a), the input signal

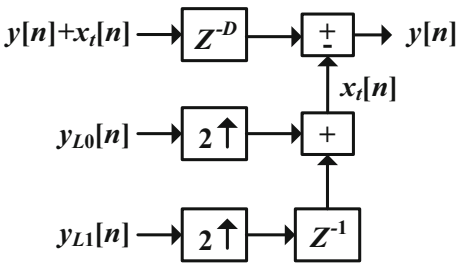

Fig. 7 The structure of the preprocessing module

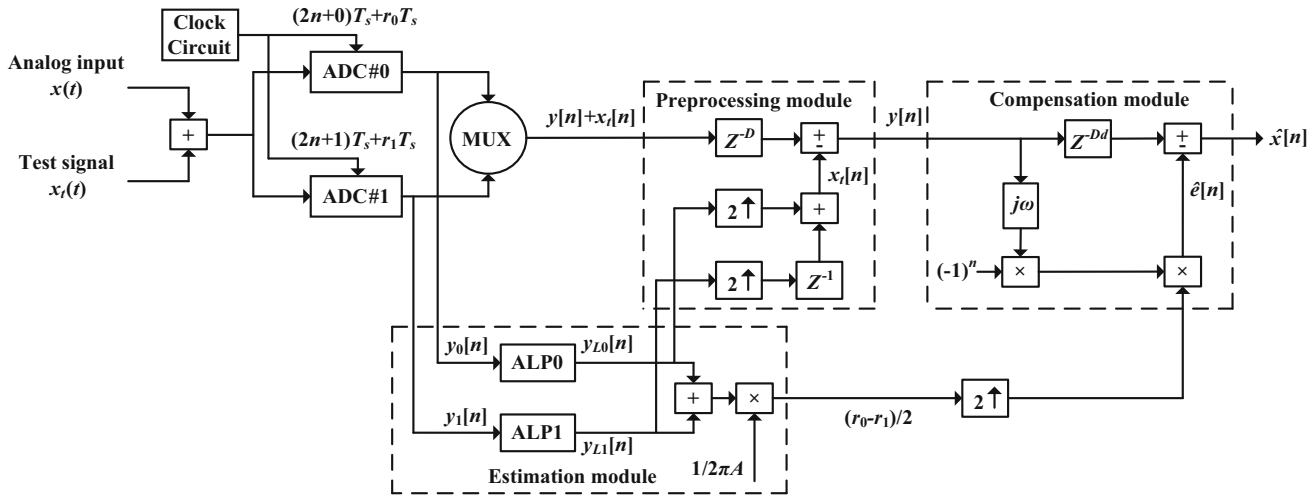

Fig. 8 The TIADC system with estimation, preprocessing and compensation calibration structure

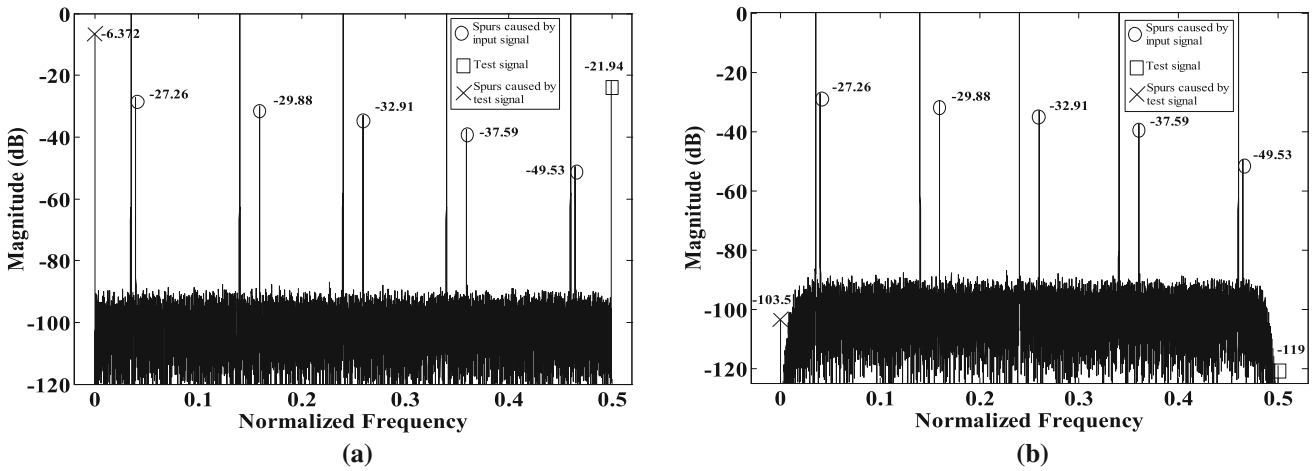

Fig. 9 The spectrum **a** of the input signal combined with the test signal and **b** of the output after preprocessing

combined with the test signal contains the power spectrum of the test signal and its spurious caused by timing error. In Fig. 9(b), after using the preprocessing module, the test signal and its spurious are removed from the uncalibrated output of TIADC. So the test signal and the spur caused by it will not bring any extra trouble to compensation and it does not interfere with the normal operation of TIADC.

4.2 Mismatch estimation

Figure 10 shows three results of estimated timing mismatches with different values of time parameters. There are $r_0 = -0.03$ $r_1 = 0.03$, $r_0 = 0.02$ $r_1 = -0.01$ and $r_0 = 0.05$ $r_1 = -0.05$. According to the given timing errors in ADC#0 and ADC#1, the coefficients $(r_0–r_1)/2$ should be -0.03, 0.015 and 0.05 respectively. From Fig. 10, the estimated coefficient is in well accordance with the given one. The time consumption of the estimation is

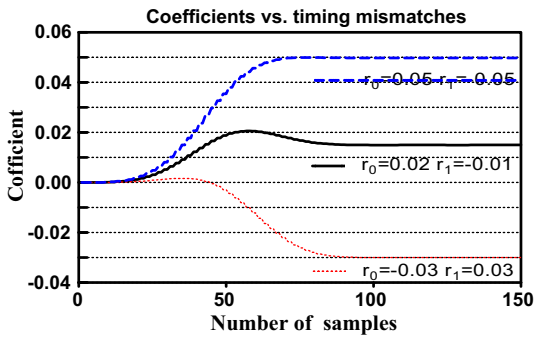

Fig. 10 The result of estimation

very small. It is the delay caused by the low-pass filter which is used after the sub-ADC. The low-pass filter's order was 50 and it operated at the frequency of half the overall sampling frequency of TIADC, so the number of delayed samples here was 100 samples.

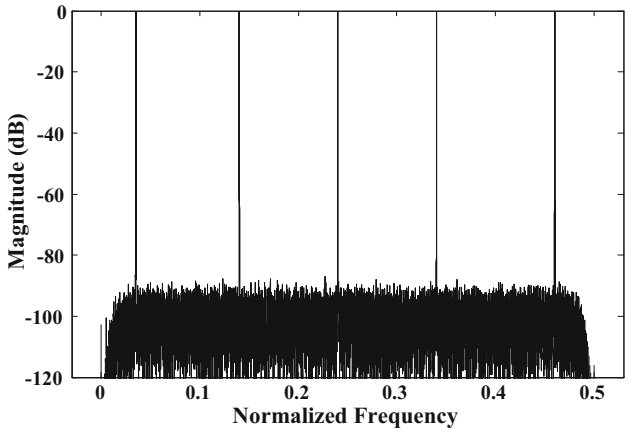

Fig. 11 The result of compensation

4.3 Compensation

The estimated coefficient is fed into the compensation module simultaneously to calibrate the input signal and the result of compensation is shown in Fig. 11. The uncalibrated result shown in Fig. 9(b) describes that the spectrum of the spurious from low to high frequency is [−27.26 dB, −29.88 dB, −32.91 dB, −37.59 dB, −49.53 dB]. The SFDR of uncalibrated is 27.26 dB. And in Fig. 11, we can clearly see that the spurious due to the timing errors have been effectively calibrated. The SFDR of calibrated is 85.44 dB and which is a significant improvement in SFDR.

In the previous method in [6], the high-pass filter which operates at the frequency same with the overall sampling frequency of TIADC is used and a significant error energy in the mismatch band is required. However the proposed method in this paper utilizes the low-pass filter which operates at the frequency of half the overall sampling frequency of TIADC and does not require a significant error energy in the mismatch band. Which can reduce the difficulty of implementation and the restriction on input signal. Moreover, for the method in this paper, the time consumption of the estimation is the delay caused by the low-pass filter and which is very small so that the proposed method can deal with variable timing errors which vary fast.

5 Conclusion

In this paper, we have presented an adaptive semiblind background calibration of timing mismatches in a two-channel TIADC based on injecting a sine wave test signal. We have demonstrated the calibration method by using a multi-tone input signal consisting of five sinusoids. The simulation results have confirmed that with this calibration method a considerable improvement in SFDR can be achieved. The simulation results also show that the proposed method can deal with the TIADC system with variable timing errors that can vary considerably fast and this kind of input signals have no power spectrum of error existing in the mismatch band. Furthermore, that the low-pass filter operates at the frequency of half the overall sampling frequency of TIADC can reduce the difficulty of implementation.

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