Area Efficient Concurrent Error Detection and Correction for Parallel Filters

P. Reviriego, S. Pontarelli, C.J. Bleakley and J.A. Maestro

In modern signal processing circuits, it is common to find several filters operating in parallel. In this letter, we propose an area efficient technique to detect and correct single errors occurring in pairs of parallel filters that have either the same input data or the same impulse response. The technique uses a primary implementation comprised of two independent filters and a redundant implementation that shares input data between both filters so as to detect and correct errors. Herein, the area cost of the proposed scheme is shown to be slightly more than double that of the unprotected filter, whereas the conventional Triple Modular Redundancy solution requires an area three times that of the unprotected filter.

Introduction: Reliability is a major issue for advanced electronic circuits. As technology scales, circuits become smaller and use lower supply voltages. This makes then more vulnerable to manufacturing defects, radiation and noise that can cause permanent faults and transient errors [1]. To mitigate these issues, a wide range of techniques has been proposed including changes to the manufacturing process, modified low level circuit designs and modular redundancy [2]. In Triple Modular Redundancy (TMR), three copies of the basic circuit operate in parallel on the same inputs. An error detection unit monitors the outputs and, if they differ, uses voting to select one of the two error-free outputs. Dual Modular Redundancy (DMR) only uses one redundant module and so, conventionally, DMR can detect errors but cannot correct them. Alternatively, the algorithmic or structural properties of certain circuits, such as signal processing circuits, can be used detect and correct errors [3].

In modern signal processing circuits, it is common to find several filters operating in parallel. This is the case, for example, in filter banks in which the same input signal is processed simultaneously by different filters [4]. In communications circuits, different signals are often processed simultaneously by parallel copies of the same filter [5].

In this letter, we propose a novel area efficient technique for detecting and correcting permanent and transient single errors occurring in pairs of parallel filters that share the same input data or have identical impulse responses. The proposed scheme uses a single redundant module. Thus, the area cost is similar to that of DMR. Error protection is achieved by exploiting the fact that the redundant module is functionally equivalent to the primary implementation but is structurally different. Previous work on design diverse DMR for Finite Impulse Response (FIR) filters [6], [7] focused on protecting single filters against transient errors and relied on recognition of temporal error patterns. In contrast, the proposal described herein only considers the current output sample. It has the advantages of protecting parallel filters against transient and permanent errors, and is valid for use with Finite Impulse Response and Infinite Impulse Response (IIR) filters.

Shared Signal DMR for parallel filters: A pair of parallel filters implements the following transformation:

$$y_i[n] = \sum_{k=0}^{N} h_i[k] x_i[n-k] \qquad i = 1, 2 \tag{1}$$

where $x_i[n]$ is the filter input, $y_i[n]$ is the filter output, $h_i[k]$ is the filter impulse response and i is the filter number.

In the case that the filters to be protected have the same impulse response, i.e. $h_1[k]=h_2[k]=h[k]$ for all k, protection is achieved as follows. The primary module implements Eq. (1) directly, whereas the redundant module implements the following:

$$\begin{aligned} s_1[n] &= \sum_{k=0}^{N} h[k](x_1[n-k] + x_2[n-k]) \\ d_1[n] &= \sum_{k=0}^{N} h[k](x_1[n-k] - x_2[n-k]) \\ y_1[n] &= \frac{1}{2}(s_1[n] + d_1[n]) \\ y_2[n] &= \frac{1}{2}(s_1[n] - d_1[n]) \end{aligned} \tag{2}$$

where $h[k]$ is the common impulse response and $s_1[n]$ and $d_1[n]$ are the filtered sum and the filtered difference of $x_1[n]$ and $x_2[n]$, respectively.

This arrangement is illustrated in Figure 1. The redundant module uses one filter to process the sum of the input signal and the other to process the difference. The sum and difference operations are undone in post-processing logic prior to the module output. The inherent scaling by a factor of two can be accounted for by a bit shift at the output, as in Eq. (1), or at the input, as shown in Figure 1.

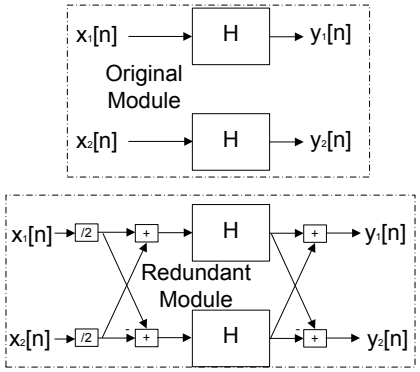

Fig. 1 *Shared Signal DMR for parallel filters with the same impulse response.*

Errors in the filters can be detected and corrected by noting that an error in the primary module propagates to only one output, whereas an error in the redundant module propagates to both outputs. However, errors in the post-processing logic of the redundant module only affect one filter output. Therefore, an error in the post-processing logic could be confused with an error in the primary implementation. To avoid this ambiguity, the post-processing logic must be duplicated. This allows an error in the post-processing logic to be identified.

The scheme can be used for both FIR and IIR filters, in fact in can be used for any transformation $F(.)$ for which the following property applies $F(A+B) = F(A)+F(B)$. This includes, for example, the Discrete Fourier Transform.

The complexity of the proposed technique is more than two times that of the primary module since, to avoid overflow, the redundant module requires an additional bit to represent the sum and difference signals. In relative terms, this has a small impact on area complexity when the filter bit-width is large. Six additional add/subtract operations are needed for pre- and post-processing and for error checking. For a typical filter, the relative increase in area due to these additional operations is small since additions and subtractions are much simpler than the multiplications required in the filters themselves. The scheme can be extended to the case where the filters to be protected have the same input data, i.e. $x_1[n]=x_2[n]]=x[n]$ for all n but different impulse responses. In this case, protection is achieved as follows:

$$\begin{aligned} s_2[n] &= \sum_{k=0}^{N} (h_1[k] + h_2[k]) x[n-k] \\ d_2[n] &= \sum_{k=0}^{N} (h_1[k] - h_2[k]) x[n-k] \\ y_1[n] &= \frac{1}{2}(s_2[n] + d_2[n]) \\ y_2[n] &= \frac{1}{2}(s_2[n] - d_2[n]) \end{aligned} \tag{3}$$

where $x[n]$ is the common input signal and $s_2[n]$ and $d_2[n]$ are the input signals filtered by the sum and difference of the impulse responses. In this case, the filter responses are combined and the combination is the undone at the filter output. This ensures that an error in the redundant module affects both outputs. As before, the post-processing operations are duplicated for error detection purposes. The complexity of the proposed technique depends on the complexity of the redundant sum and difference filters. For IIR filters, area complexity increases significantly as the combined responses are, in the general case, of a higher order. However, for FIR filters of the same order, the combined responses are of the same order and have similar complexity to the primary filters. Thus, the technique is effective for FIR filters. Four additional add/subtract operations are required for post-processing and error checking.

Evaluation: The proposed technique was implemented in Matlab for a pair of parallel FIR filters with identical impulse responses of order twelve. The filter coefficients correspond to a low pass filter and the inputs were generated randomly and quantized to sixteen bits. Filtering was performed without truncation or rounding. One thousand single errors, both transient and permanent, were randomly inserted into the primary and redundant modules. The final error protected output was compared with that obtained using an error-free implementation. It was found that in all cases the inserted errors were corrected.
In the case of truncation or rounding, the outputs of the primary and redundant modules may be different even in the absence of errors. To allow for this, a small error tolerance has to be added to the comparisons such that an error is only detected when the tolerance has been exceeded.
To evaluate the area cost of the proposed technique, two example circuits were implemented. The first consisted of two parallel filters with identical FIR filters: both 12^{th} order low-pass with cut-off frequency at 0.5. The second consisted of two different filters applied to the same input signal. The filters were 12^{th} order FIR filters, one low-pass and the other high-pass with cut-off frequencies at 0.2 and 0.8, respectively. The filters were implemented using a Hardware Description Language (HDL) for various coefficient and data word bit-widths. The area estimates after synthesis for a 45nm target library are presented in Table 1. The results show that the proposed technique requires a much smaller overhead than that of TMR. In fact, for the cases considered, the overhead is only slightly greater than that of conventional DMR, which only provides error detection.

Table 1: Area estimates for the example circuits (NAND2 Gate Equivalents).

	Unprotected	Shared Signal DMR	Overhead
Example 1			
8 bits	5,511	12,907	134%
16 bits	18,776	40,236	114%
Example 2			
8 bits	5,426	11,323	109%
16 bits	17,920	37,941	112%

Conclusion: This letter describes a novel technique for error protection of pairs of parallel filters that either share the same input signal or have identical impulse responses. The method can detect and correct transient and permanent errors at a significantly lower area cost than the conventional TMR approach. The proposed approach was evaluated in simulation and found to detect and correct all single errors. The area cost of the approach was assessed by means of HDL implementation and synthesis of two example circuits. The area overhead was found to be close to that of conventional DMR.

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